OKI

'96 Data Book for SPEECH LSI DEVICES (DIGEST)

FIRST EDITION
ISSUE DATE: MAY, 1996

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the imformation being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit and assembly designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. OKI assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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2 RECORDING AND PLAYBACK ICs

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Q&A

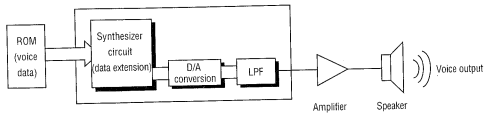
Note: Please refer to " '96 SPEECH LSI DEVICES DATA BOOK (DETAILS)" for details of each device.

1 INTRODUCTION

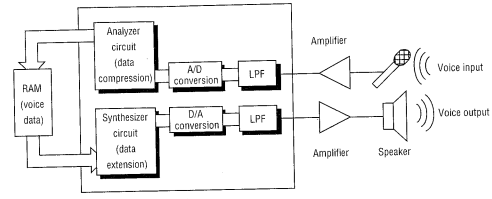
♦ PRODUCT LINE-UP

OKI's voice synthesizers use the Oki ADPCM and Oki SBC methods featuring high quality sound real voice.
Mainly lined up are voice synthesis ICs, recording and playback ICs, dedicated memories, and interface ICs. In addition, a developing environment including development tools, dedicated writers, demonstration boards, and a user support system is fully supported.

■ BASIC CONFIGURATION OF VOICE SYNTHESIS IC



■ BASIC CONFIGURATION OF RECORDING AND PLAYBACK IC



Built-in mask ROM voice synthesis ICs

MSM6650 family
- MSM6652A (288 Kbits)
- MSM6653A (544 Kbits)
- MSM6654A (1 Mbit)
- MSM6655A (1.5 Mbits)
- MSM6656A (2 Mbits)
- MSM6658A (4 Mbits)
- MSM66P54 (1 Mbit OTP)
- MSM66P56* (2 Mbits OTP)
- MSM6650 (External ROM)

External memory drive voice synthesis ICs

MSM6295 (4-channel mixing)
MSM9810 (8-channel mixing)*

Tone Controller IC

MSM6722

Prototype Voice Synthesis IC

MSM6585

Built-in mask ROM voice synthesis ICs

MSM9800 family
- MSM9802 (512 Kbits)
- MSM9803 (1 Mbits)
- MSM9805 (2 Mbits)*
- MSM98P05 (2 Mbits OTP)*

Development Support Tools

AR203 (for IBM PC/AT English)
PARAWRITER
BACKUP
ANAWRITER MK6
ANAWRITER MK8
PARAWRITER P74
PARAWRITER P54
Demonstration boards

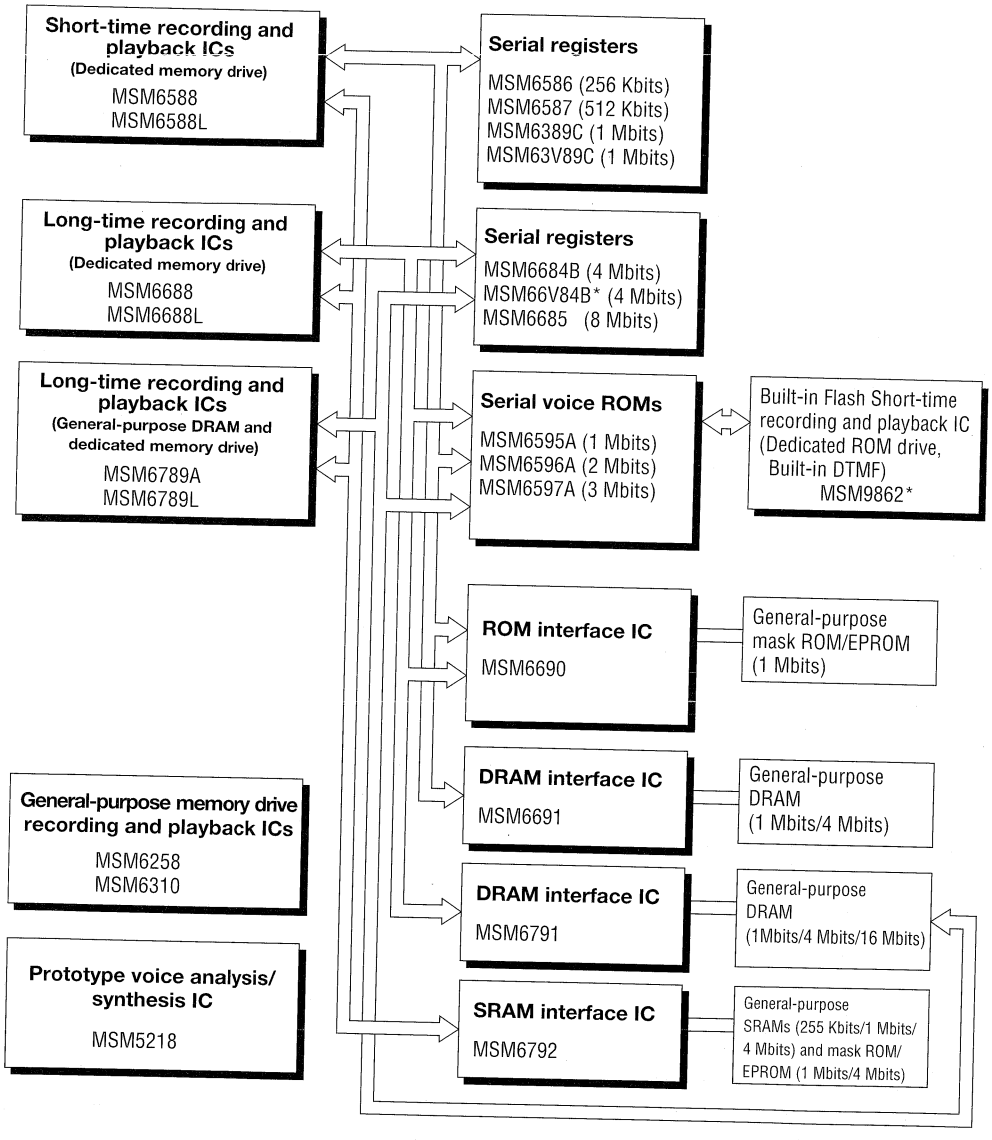
Speaker Drive Amplifiers

MSC1157
MSA180

Built-in OTP ROM voice synthesis ICs

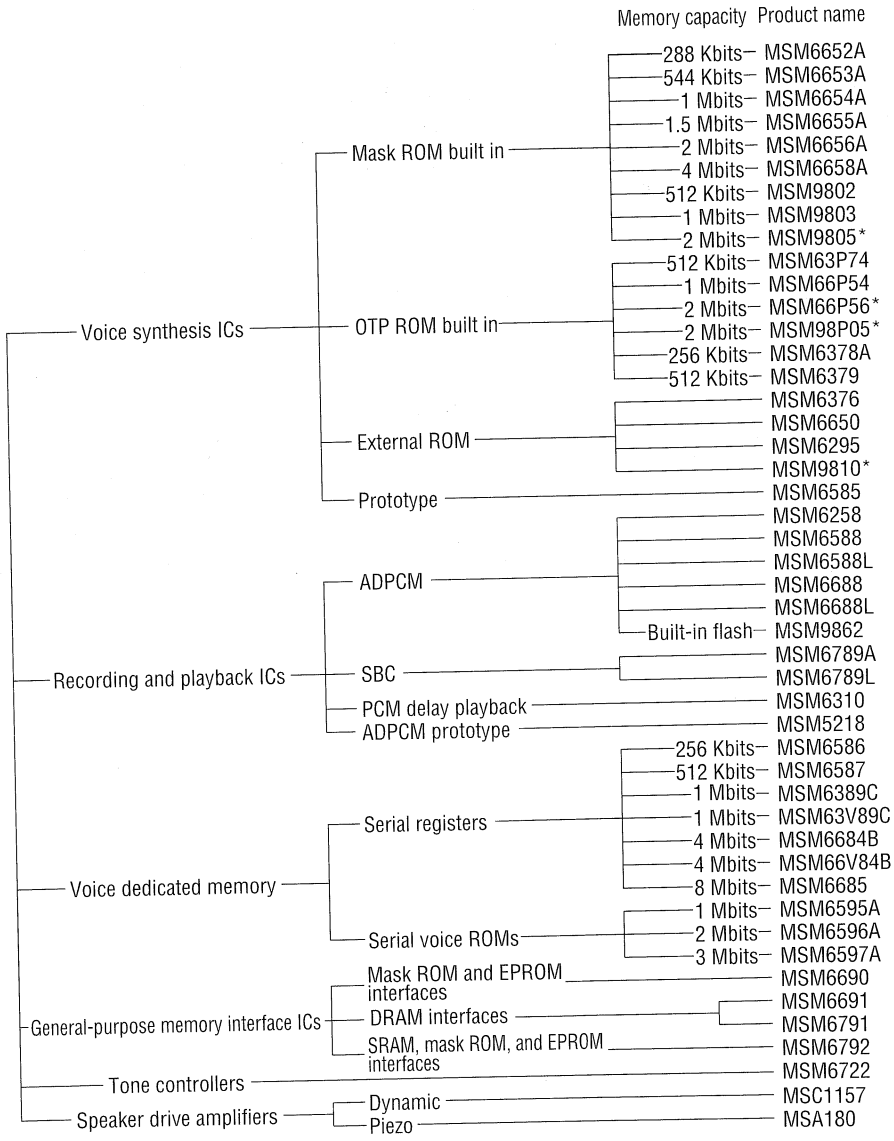
MSM63P74 (512 Kbits)
MSM6378A (256 Kbits)
MSM6379 (512 Kbits)

* Under development



* Under development

■ VOICE SYNTHESIZER PRODUCTS



* Under development

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■ DEVELOPMENT SUPPORT TOOLS

	Function overview	Applicable device	Operating environment	Japanese/ English
AR76-202 (Discontinued)	Voice analysis and edit; data write to ROM	All ROM-playback-type products	IBM-compatible machines	English
AR203	Voice analysis and edit; data write to ROM	All ROM-playback-type products	IBM-compatible machines	English
ANAWRITER MARK VI	Voice analysis and data write for MSM6378A/79	MSM6378A, MSM6379	Standalone	—
BACKUP	Writing to original EPROM	MSM6378A	Standalone	—
PARAWRITER	Writing to up to ten MSM6378A devices	MSM6378A	Standalone	—
PARAWRITER P74	Writing to up to ten MSM63P74 devices	MSM63P74	Standalone	—
PARAWRITER P54	Writing to up to ten MSM66P54 devices	MSM66P54	Standalone	—

Note: Full compatibility with IBM-PC (IBM-PC is a registered trademark of IBM Corporation) is required for "IBM-equivalent machines" denoted here when the AR76-202 or AR203 is used.

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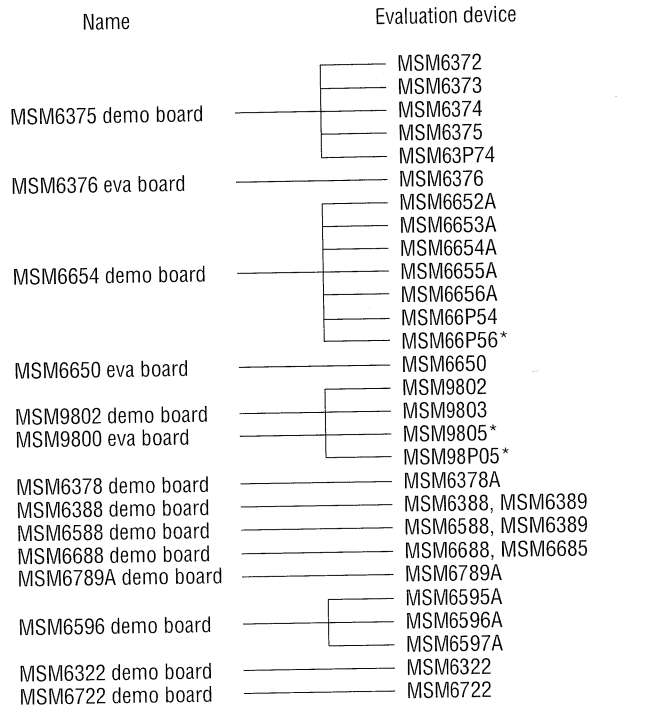
■ DEMONSTRATION BOARDS



* Under development

♦ PRODUCTS AND TYPICAL SPECIFICATIONS (Voice Synthesis ICs)

Product name	MSM6652A/53A/54A /55A/56A/58A	MSM6650	MSM66P54 /P56*	MSM9802/03 /05*	MSM98P05*	MSM63P74	MSM6378A /79	MSM6295	MSM9810*	MSM6585
Coding	4-bit ADPCM 8-bit PCM			8-bit PCM		4-bit ADPCM		4-bit ADPCM	4-bit ADPCM/ ADPCM2 8-bit PCM	4-bit ADPCM
ROM type	Built-in Mask ROM	External	Built-in OTP	Built-in Mask ROM	Built-in OTP			External		—
ROM capacity	288K/544K/1M/ 1.5M/2M/4Mbits	Up to 64Mbits	1Mbits 2Mbits	512K/1M /2Mbits	2Mbits	512Kbits	256K/512Kbits	Up to 2Mbits	Up to 128Mbits	—
Synthesis time (Sampling frequency)	16sec/33sec/63sec/94sec/ 126sec/252sec (4kHz) 10sec/20sec/39sec/58sec/ 78sec/156sec (6.4kHz) 4sec/8sec/15sec/23sec/ 31sec/62sec (16kHz)	67min (4kHz) 42min (6.4kHz) 16min (16kHz)	MSM66P54 63sec (4.0kHz) 39sec (6.4kHz) 15sec (16kHz) MSM66P56 126sec (4kHz) 78sec (6.4kHz) 31sec (16kHz)	8sec/16sec/32sec (8kHz)	32sec (8kHz)	32sec (4kHz) 20sec (6.4kHz) 8sec (16kHz)	16sec/32sec (4kHz) 10sec/20sec (6.4kHz) 8sec (16kHz)	80sec (6.4kHz) 16sec (32kHz)	134min (4kHz) 84min (6.4kHz) 32min (16kHz)	Determined by external circuit
Sampling frequency	4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16.0, 32.0kHz(Ceramic oscillation) 4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16.0kHz (RC oscillation)			4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16.0kHz (Ceramic oscillation)		4.0, 6.4, 8.0kHz (f_{OSC}=64kHz)	4.0kHz to 16.0kHz	6.4kHz to 32.0kHz	4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16.0, 21.3, 25.6, 32.0kHz	4.0, 8.0, 16.0 32.0kHz
Clock frequency	4.096MHz (Crystal oscillation) 256kHz (RC oscillation)					64kHz to 256kHz (RC/crystal oscillaiton)		1MHz to 4MHz	4.096MHz	640kHz
D/A converter	12 bits			10 bits		12 bits			14 bits	12 bits
Low-pass filter	–40dB/oct			Built-in		–24dB/oct		—	Built-in	–40dB/oct
Supply voltage	2.7V to 5.5V 3.5V to 5.5V (MSM6658A)	3.5V to 5.5V	2.0V to 5.5V	3.5V to 5.5V		2.7V to 5.5V		4.5V to 5.5V	2.7V to 5.5V	4.5V to 5.5V
Operating current	10mA	20mA	10mA	20mA		20mA		10mA	15mA	10mA
Standby current	10µA	100µA	10µA	100µA		100µA	10µA	—	10µA	—
Package	Chip 18-pin DIP 24-pin SOP MSM6658A : 24-pin SOP only	64-pin QFP 64-pin SDIP	20-pin DIP 24-pin SOP MSM66P56 : 20-pin DIP only	Chip 18-pin DIP 24-pin SOP 30-pin SSOP	20-pin DIP 24-pin SOP	20-pin DIP	Chip 16-pin DIP	44-pin QFP 42-pin DIP	64-pin QFP	18-pin DIP 24-pin SOP
Voice analysis tool	AR203						ANA writer/MK6 ANA writer/MK8 AR203	AR203		
Other characteristics	Edit ROM, melody, fade-out 2-channel maxing, random playback			Edit ROM random playback	2-channel mixing echo playback, beep tones.	Power on start	4-channel mixing, echo playback	Edit ROM 8-channel mixing, stereo output		Prototype

* Under development

♦ PRODUCTS AND TYPICAL SPECIFICATIONS (Recording and Playback ICs)

Product name	Short time recording and playback type			Long time recording and playback type				Prototype		
	MSM6588	MSM6588L	MSM9862*	MSM6688	MSM6688L	MSM6789A	MSM6789L	MSM6258	MSM6310	MSM5218
Coding	3-bit/4-bit ADPCM*1			3-bit/4-bit ADPCM		SBC 8-bit PCM*5		3-bit/4-bit ADPCM	8-bit PCM	3-bit/4-bit ADPCM
Memory type to be connected (max. capacity)	Serial register (4Mbits) Serial voice ROM (3Mbits)*3		Built-in FLASH (512Kbits)	Serial register (32Mbits)*6		Serial register (32Mbit)*7 general DRAM (32Mbits)*8		DRAM (16Mbits) SRAM (4Mbits) Mask ROM/EPROM (4Mbits)	DRAM (512Kbits)	—
			Serial register (4Mbits) serial voice ROM (3Mbits)	Serial voice (4Mbits)						
Maximum recording time (sampling frequency bit rate)	262sec (5.3kHz) 174sec (8kHz) in 3-bit ADPCM		294sec (5.3kHz)*9 196sec (8.0kHz) in 3-bit ADPCM	34min (4kHz 4-bit) 17min (8kHz 4-bit)		73min (7.5kbps) 34min (16kbps)		DRAM 17min (4kHz) SRAM 256sec (4kHz) Mask ROM/EPROM	16sec (4kHz) 8sec (8kHz)	Determined by external circuit
Number of words/ phrases	8 words *4		8 words *4	63 words (variable message) 255 words (fixed message)*2				7 words*3	1 word (Delay playback)	Determined by external circuit
Sampling frequency	4.0kHz to 16.0kHz		4.0kHz to 8kHz	4.0kHz to 16.0kHz		6kHz/8kHz		4.0kHz to 15.6kHz	4.0kHz to 16.0kHz	4.0kHz to 16.0kHz
Clock frequency	4.0MHz to 8.192MHz		4.096MHz	4.0MHz to 8.192MHz		6.0MHz to 8.192MHz		4.0MHz to 8MHz	4.0MHz to 8.2MHz	384kHz to 768kHz
Microphone/line amplifier	Built-in							—	Builtin line amplifier	—
A/D converter	12bits							8 bits		—
D/A converter	12bits							10 bits	8 bits	10 bits
Low-pass filter	–40dB/oct		–40dB/oct	–40dB/oct		–40dB/oct		—	–24dB/oct	—
Supply voltage	3.5V to 5.5V	2.7V to 3.6V	4.5V to 5.5V	3.5V to 5.5V	2.7V to 3.6V	4.5V to 5.5V	3.0V to 3.6V	3.5V to 6.0V	4.5V to 5.5V	3.0V to 6.0V
Operating current	15mA		—	30mA		35mA		4mA	10mA	6mA
Standby current	10µA	15µA	—	10µA	15µA	10µA (connected serial resistor)		10µA	—	—
Package	44-pin QFP 44-pin TQFP		80-pin QFP	56-pin QFP 64-pin TQFP		100-pin QFP		40-pin DIP*2 44-pin QFP*2 60-pin QFP	44-pin QFP	24-pin DIP

* Under development

*1. When stand-alone mode is selected, 3-bit ADPCM operates only.
*2. When microcomputer interface is selected.
*3. Serial voice ROM is special purpose mask ROM for the MSM6588 and 6588L/6688/6688L/6789A/6789L/9862. The MSM6588 can perform fixed message playback by using serial voice ROM and serial register. The M6688/6688L/6789A/6789L/9862 can directly drive serial voice ROM.
*4. When microcomputer interface mode is used, the number of recording words depends on external control.
*5. ROM playback only.
*6. *7. The maximum memory capacities cnnected to the MSM6688L and MSM6789L are 4Mbits and 16Mbits respectively.
*8. General DRAM can not be connected to the MSM6789L.
*9. When built-in Flash memory and serial resister (4-Mbit) are used.

1

■ TONE CONTROLLER

GENERAL DESCRIPTION

The MSM6722 are ICs that convert in real-time the pitch of the voice signal in a range of one octave upward or downward. For voice pitch control, two pitch control methods can be selected. One is to change the pitch in 17 steps by two switch inputs, and the other is to select one of 16 steps by four binary input lines. Since a microphone amplifier and a low-pass filter are built in, the pitch conversion set can easily be configured by connecting a microphone, amplifier, and speaker in the peripheral circuit.

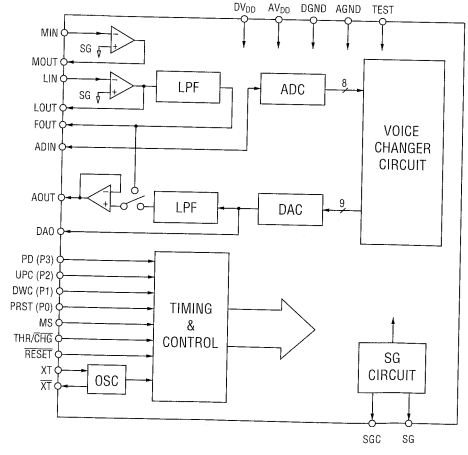
FEATURES

- Built-in microphone amplifier
- Built-in low-pass filters
- Built-in 8-bit A/D converter
- Built-in 9-bit D/A converter
- Voice pitch alterable in 17 steps (including the no pitch change step)
- Master clock frequency at 4 MHz
- 5 V single power supply
- Package : 24-pin plastic SOP (SOP24-P-430-VK)

VOICE PITCH CONTROLLER CHARACTERISTICS

Product name	MSM6722
Function	17-step voice pitch conversion
Coding method	8-bit PCM method
Clock frequency	4 MHz
Built-in analog circuit	8-bit A/D converter, 9-bit D/A converter, microphone amplifier, line amplifier
Supply voltage	+4.5 to +5.5V
Operating current	12mA
Power down current	10μA
Package	24-pin SOP

MSM6722 BLOCK DIAGRAM



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■ SPEAKER DRIVE AMPLIFIER

GENERAL DESCRIPTION

With low current consumption and the standby function, the speaker drive amplifiers are best suited to battery-driven portable equipment. Since speaker output is differential output, a high output amplitude can be produced even if supply voltage is low. Furthermore, a speaker can be connected directly to output and, thus, no coupling capacity connected directly to output and, thus, no coupling capacity is needed. A circuit is incorporated which prevents pop noise from being generated at power-ON and standby release. This enables configuration by a less number of components.

FEATURES

- Built-in pop noise prevention circuit (excluding MSA180)
- Low current consumption
- High coupling capacity not required
- High output
- Standby function

APPLICATIONS

MSC1157

- Portable telephone sets, cordless phone sets, and PHS (Personal Handphone System)
- Toys

MSA180

- Greeting cards
- Toys

SPEAKER DRIVE AMPLIFIER CHARACTERISTICS

Product name	MSC1157	MSA180
Applied speaker	Dynamic speaker	Piezo-speaker
Supply voltage	2.0 to 6.0V	
Maximum output	480 mW*2	9.8 V_{P-P}
Voltage gain	Up to ten	Up to ten
Operating current	1.6 mA	4.2 mA
Standby current	1 μA or less	
Package	Chip, 8-pin DIP, or 8-pin SOP	
Other features	—	Provided with an external power supply control pin

*1, *2 V_{CC} = 4.5V, R_L = 8Ω
*3 V_{CC} = 5.0V, I_{OUT} = 10mA

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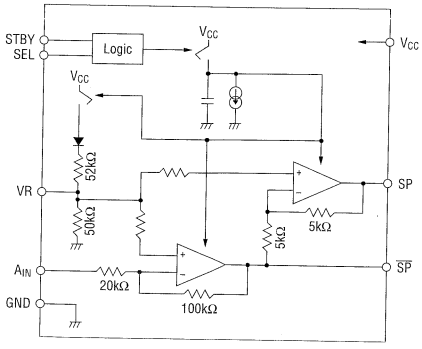
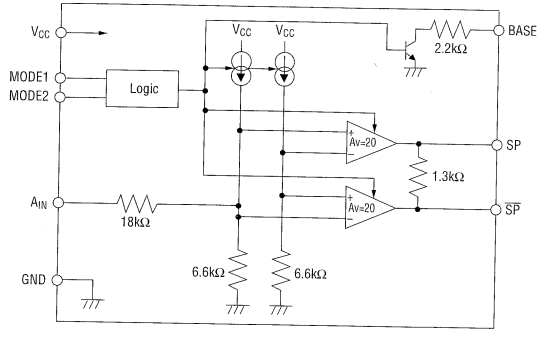
MSC1157 BLOCK DIAGRAM



MSA180 BLOCK DIAGRAM



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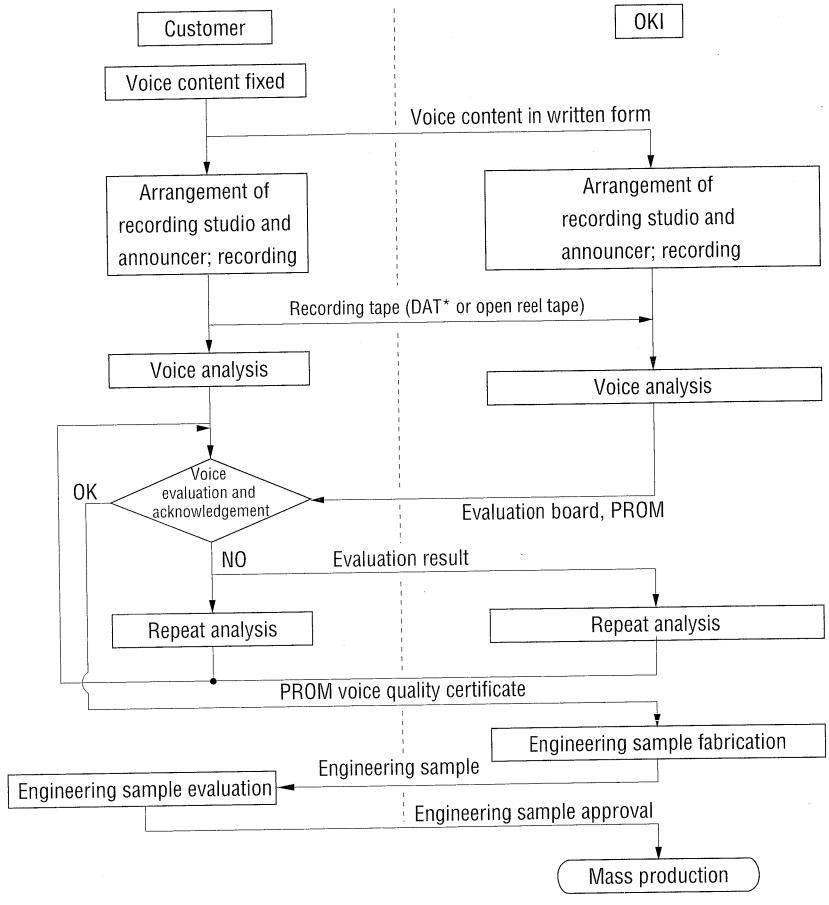
♦ BUILT-IN MASK ROM VOICE SYNTHESIS IC DEVELOPMENT



* DAT (Digital Audio Tape)

Note: The period of voice analysis varies with message contents and voice specifications. For details, contact OKI sales department.

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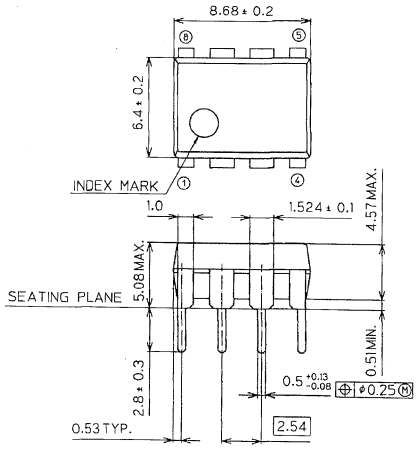
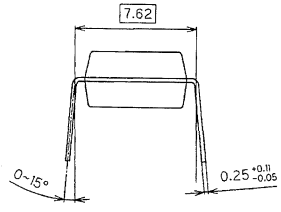
♦ PACKAGE OUTLINES AND DIMENSIONS

(Unit : mm)

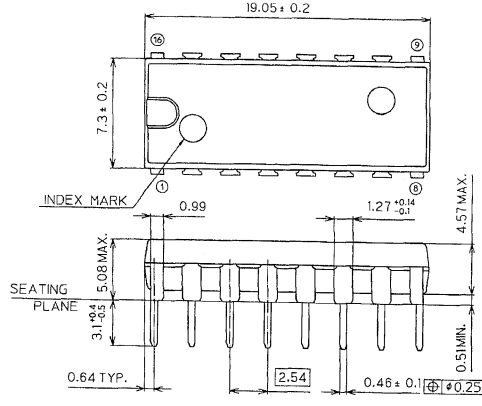
8-PIN PLASTIC	DIP8-P-300

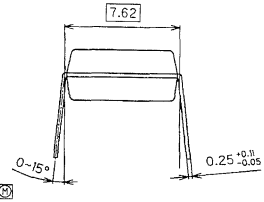




Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	0.46 TYP.

16-PIN PLASTIC	DIP16-P-300-W1

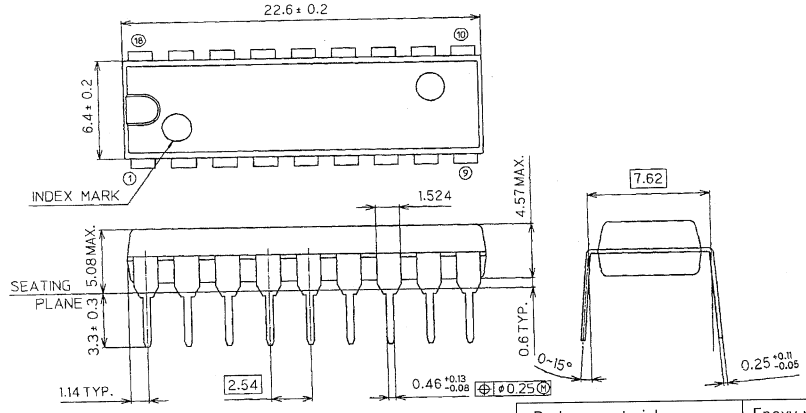




Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	1.00 TYP.

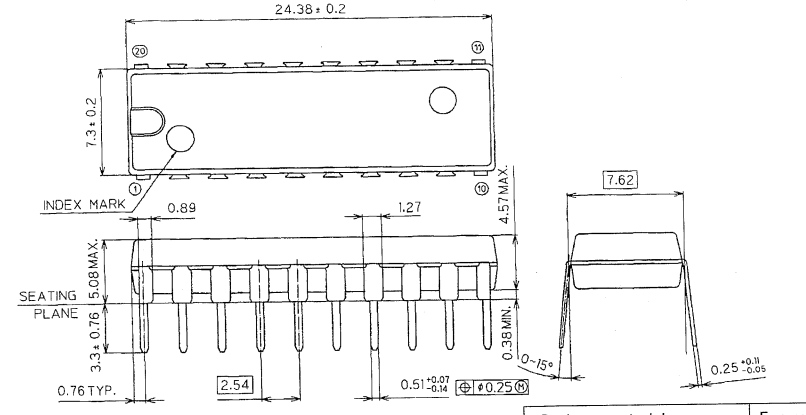
(Unit: mm)

18-PIN PLASTIC DIP	DIP18-P-300



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	1.30 TYP.

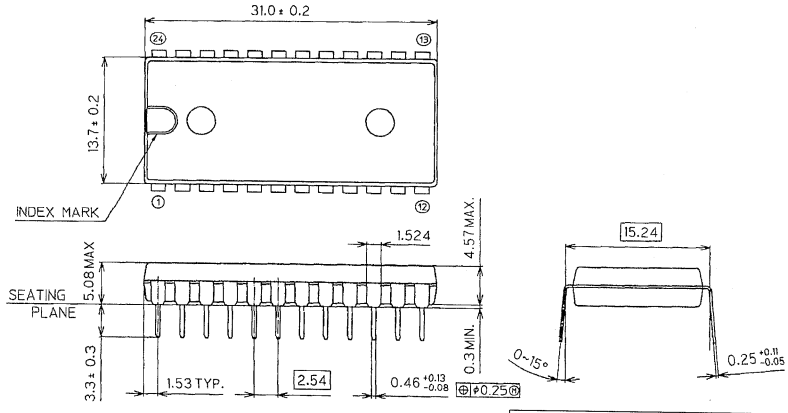
20-PIN PLASTIC DIP	DIP20-P-300-W1



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	1.50 TYP.

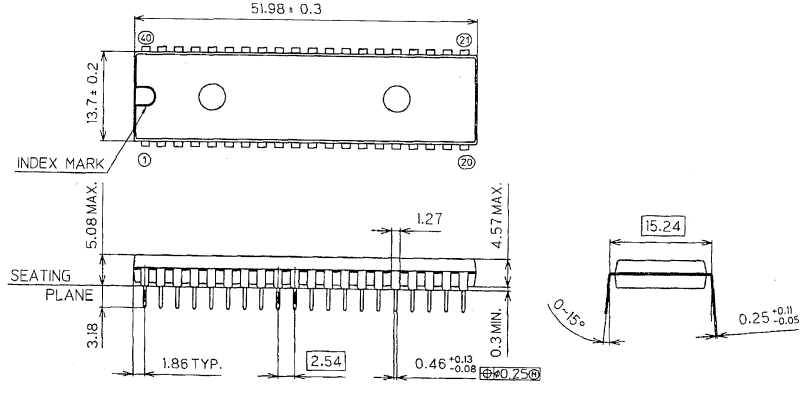
(Unit: mm)

24-PIN PLASTIC DIP	DIP24-P-600



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	3.55 TYP.

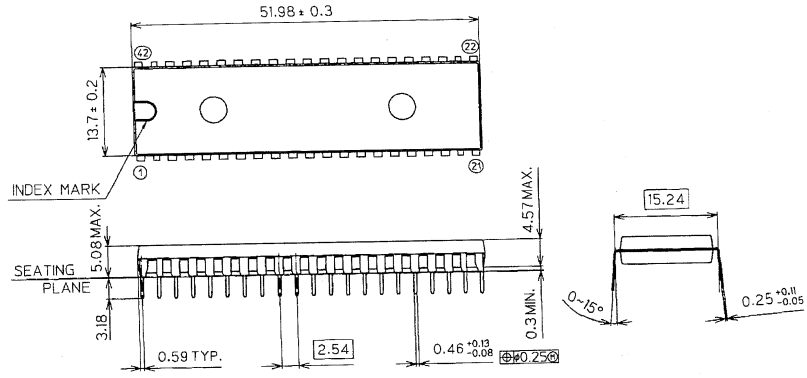
40-PIN PLASTIC DIP	DIP40-P-600



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	6.10 TYP.

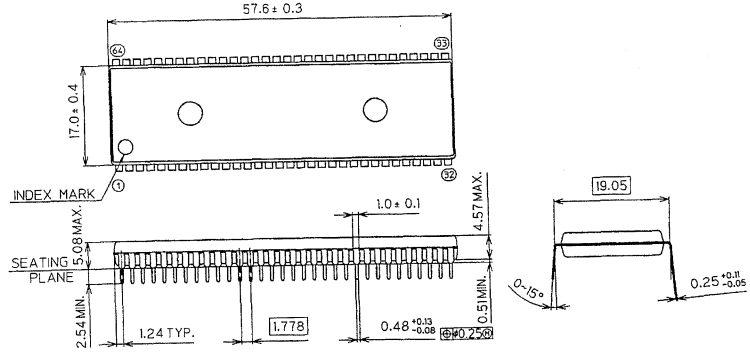
(Unit: mm)

42-PIN PLASTIC DIP	DIP42-P-600



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	6.20 TYP.

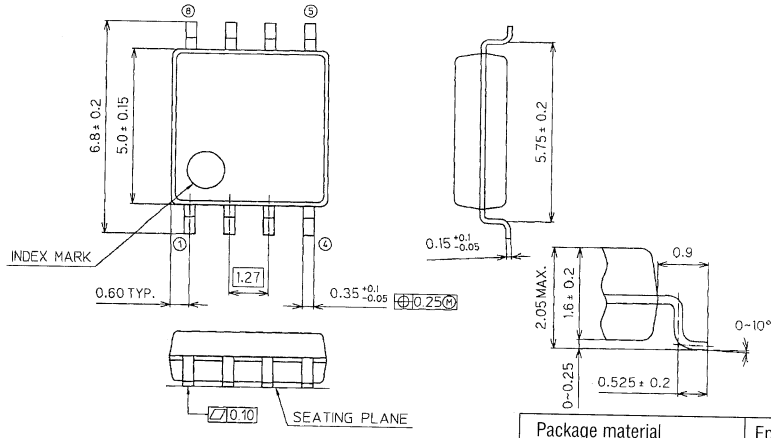
64-PIN PLASTIC SHRINK	SDIP64-P-750



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	8.70 TYP.

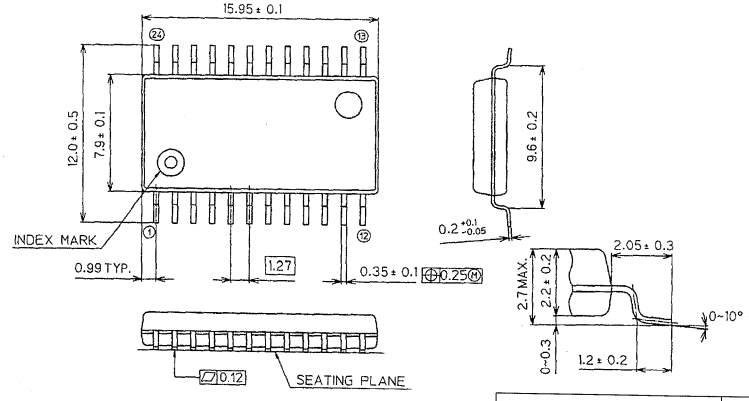
(Unit: mm)

8-PIN PLASTIC SOP | SOP8-P-250-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.10 TYP.

24-PIN PLASTIC SOP | SOP24-P-430-K



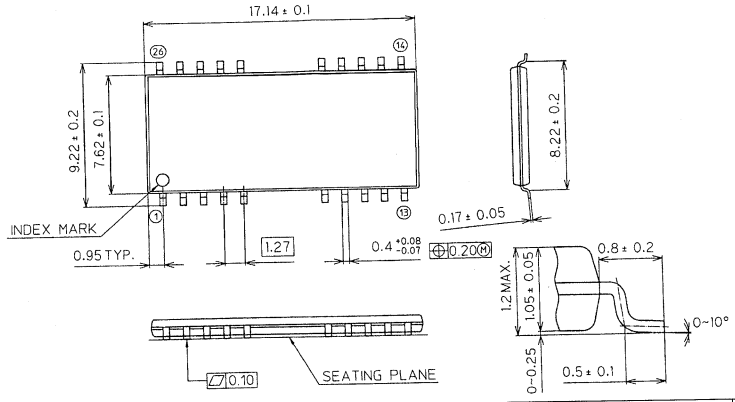
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

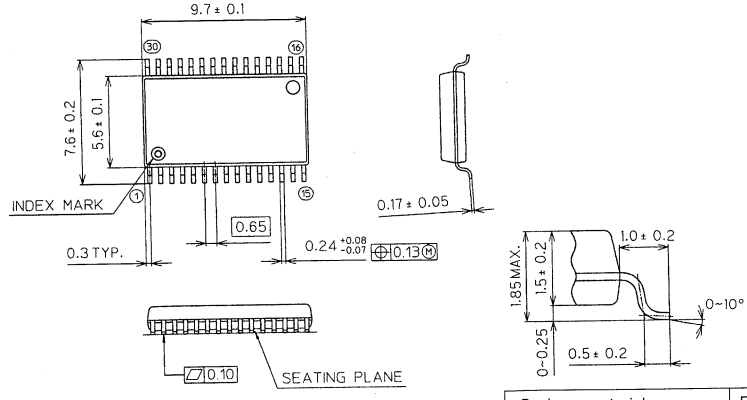
(Unit: mm)

26-PIN PLASTIC TSOP	TSOP26/20-P-300-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.38 TYP.

30-PIN PLASTIC SSOP	SSOP30-P-56/0.65-K



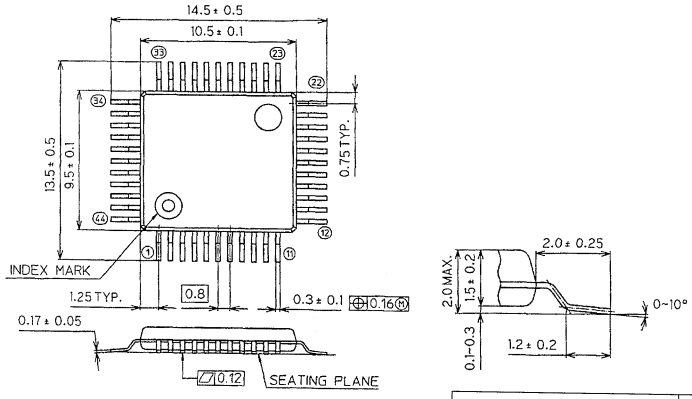
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

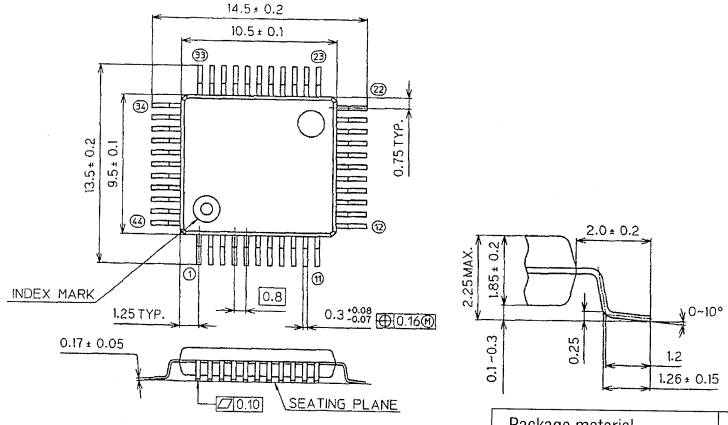
(Unit: mm)

44-PIN PLASTIC QFP	QFP44-P-910-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.35 TYP.

44-PIN PLASTIC QFP	QFP44-P-910-2K



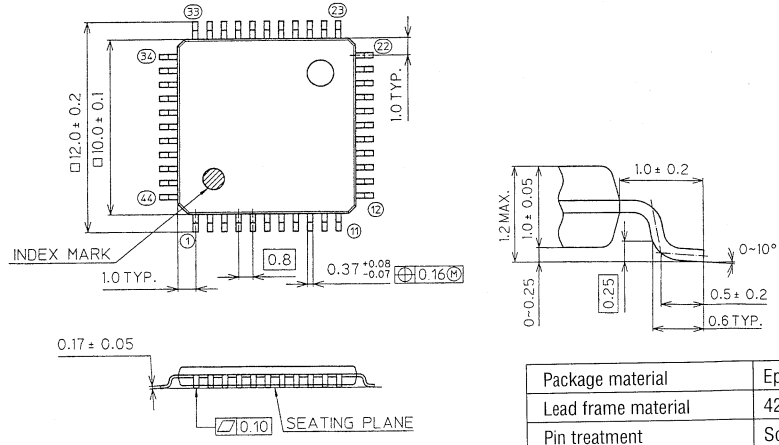
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

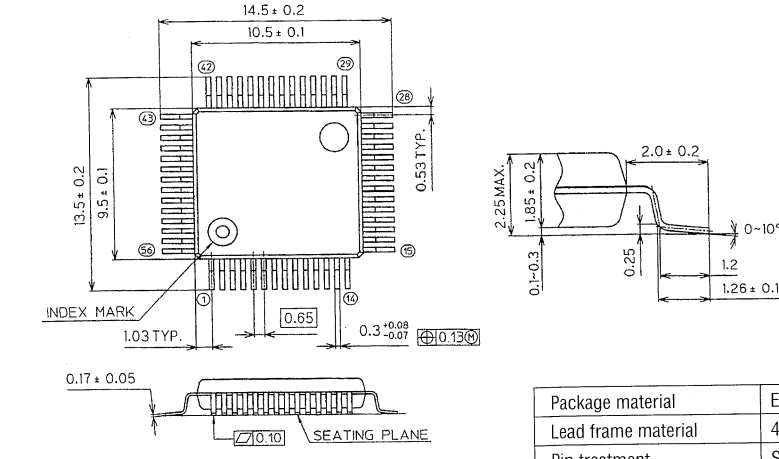
(Unit: mm)

44-PIN PLASTIC TQFP	TQFP44-P-1010/0.8-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	0.28 TYP.

56-PIN PLASTIC QFP	QFP56-P-910-2K



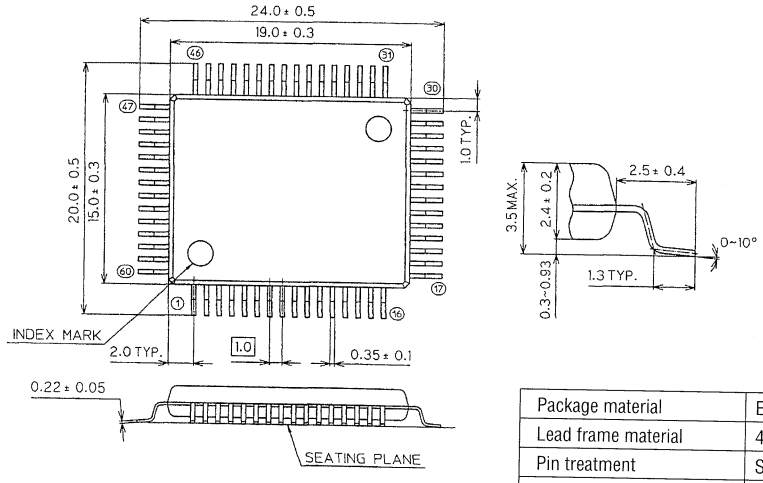
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

60-PIN PLASTIC QFP	QFP60-P-1519-K



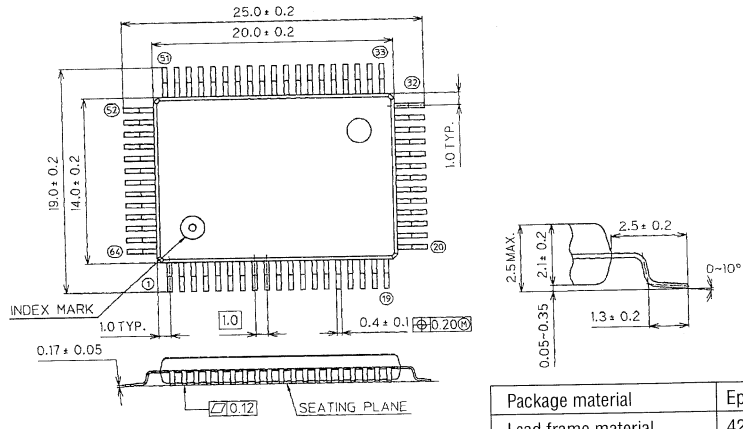
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	1.50 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

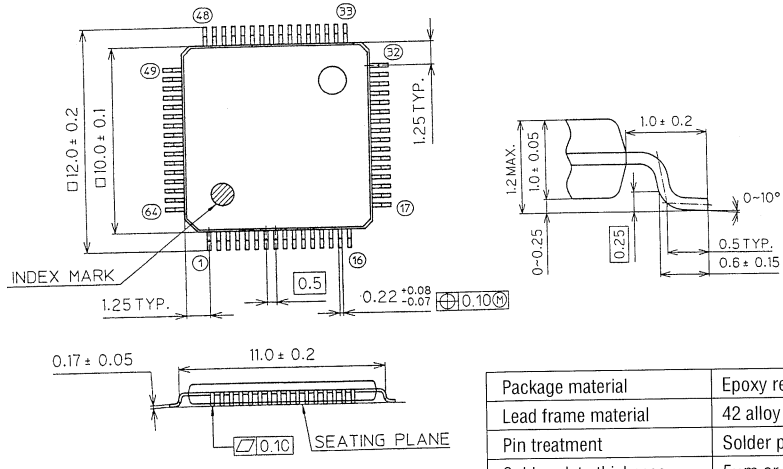
(Unit: mm)

64-PIN PLASTIC QFP	QFP64-P-1420-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	1.25 TYP.

64-PIN PLASTIC TQFP	TQFP64-P-1010/0.5-K



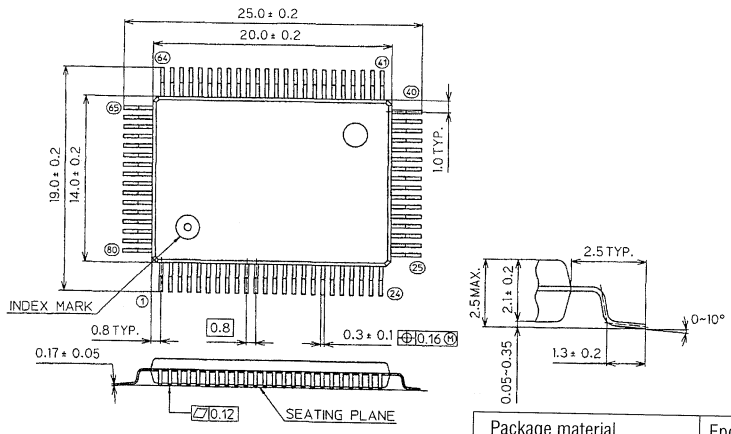
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.26 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

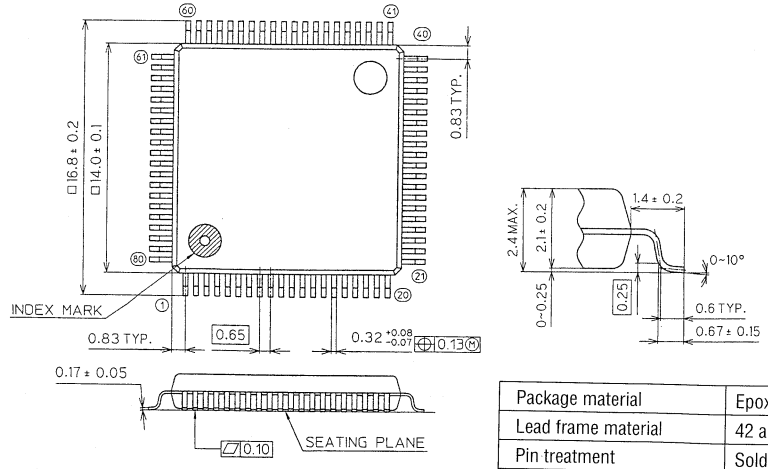
(Unit: mm)

80-PIN PLASTIC QFP | QFP80-P-1420-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	1.27 TYP.

80-PIN PLASTIC QFP | TQFP80-P-1414/0.65-K



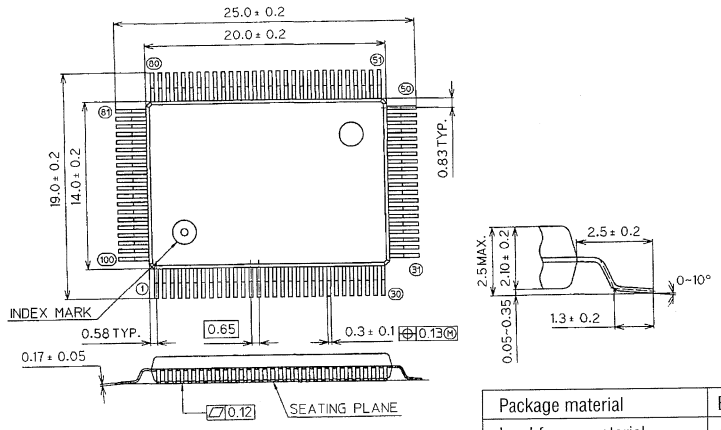
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.85 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

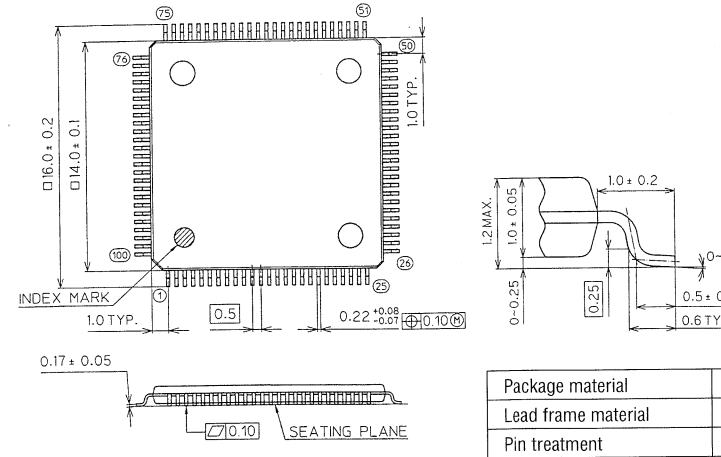
(Unit: mm)

100-PIN PLASTIC QFP	QFP100-P-1420-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	1.29 TYP.

100-PIN PLASTIC TQFP	TQFP100-P-1414/0.5-K



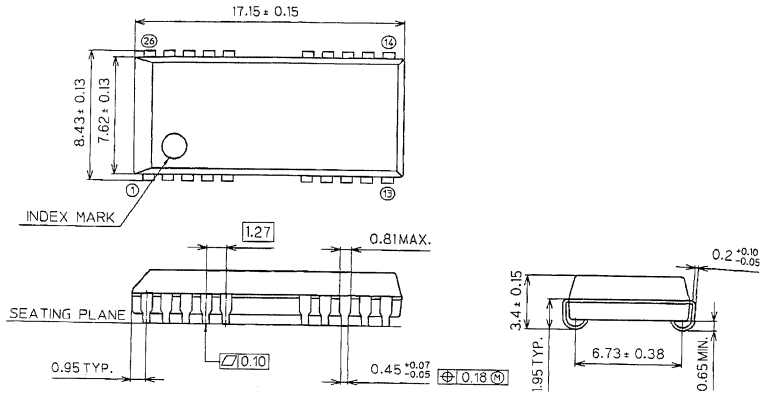
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

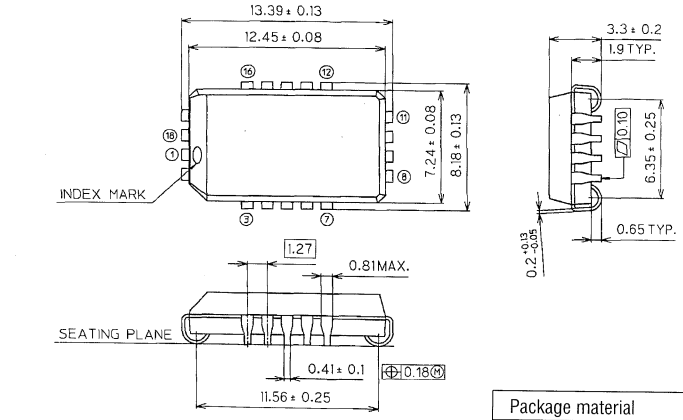
(Unit: mm)

26-PIN PLASTIC SOJ	SOJ26/20-P-300



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.80 TYP.

18-PIN PLASTIC QFJ	QFJ18-P-R290



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.50 TYP.

Notes for Mounting the Surface Mounting Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ and QFJ (PLCC) packages are very susceptible to heat in reflow mounting and to humidity absorbed in storage. Therefore, before performing reflow mounting, contact your OKI representative with the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

♦ RELIABILITY INFORMATION

Introduction

The application of semiconductor integrated circuits is rapidly expanding, from aerospace, automobiles and the public sector. Environments of IC use vary according to the application. The market demand for quality and reliability of IC products is diversifying along with demands for higher quality and reliability.

To meet diverse and advancing market demands for quality and reliability, OKI feels that it is important to maintain and improve quality and reliability in terms of product application and work environment. OKI's systematic quality and assurance activities are based on this concept. Not only in all activities that secure product quality and reliability for mass production and shipment steps, but for all steps, from product planning to after-sale service. All departments operate under a consistent quality assurance system.

The following sections explain the quality and assurance activities that OKI is engaging in.

For further information, please refer to "Quality/Reliability Hand Book" we issue.

1. Outline of Quality Assurance

OKI is engaging in product quality assurance activities under a consistent quality assurance system in all steps from product planning to development, designing, trial production, mass production, shipping, and after-sale service.

For product planning steps, we set appropriate quality and reliability levels according to the application and work environment of each product, after understanding the quality and reliability demanded by the market based on sales research. At the same time, we focus on research and development of reliable technologies, which is reflected when setting quality and reliability levels.

For product design, we followed the product specifications demanded by the customer, and designed in order to assure quality and reliability. To assure product quality and reliability, OKI has been performing two design reviews before starting mass production. (Product qualification system)

After entering the mass production process, all quality assurance activities are carried out according to OKI standards documents through the quality system based on Internaltional Organization for Standardization (ISO) 9002.

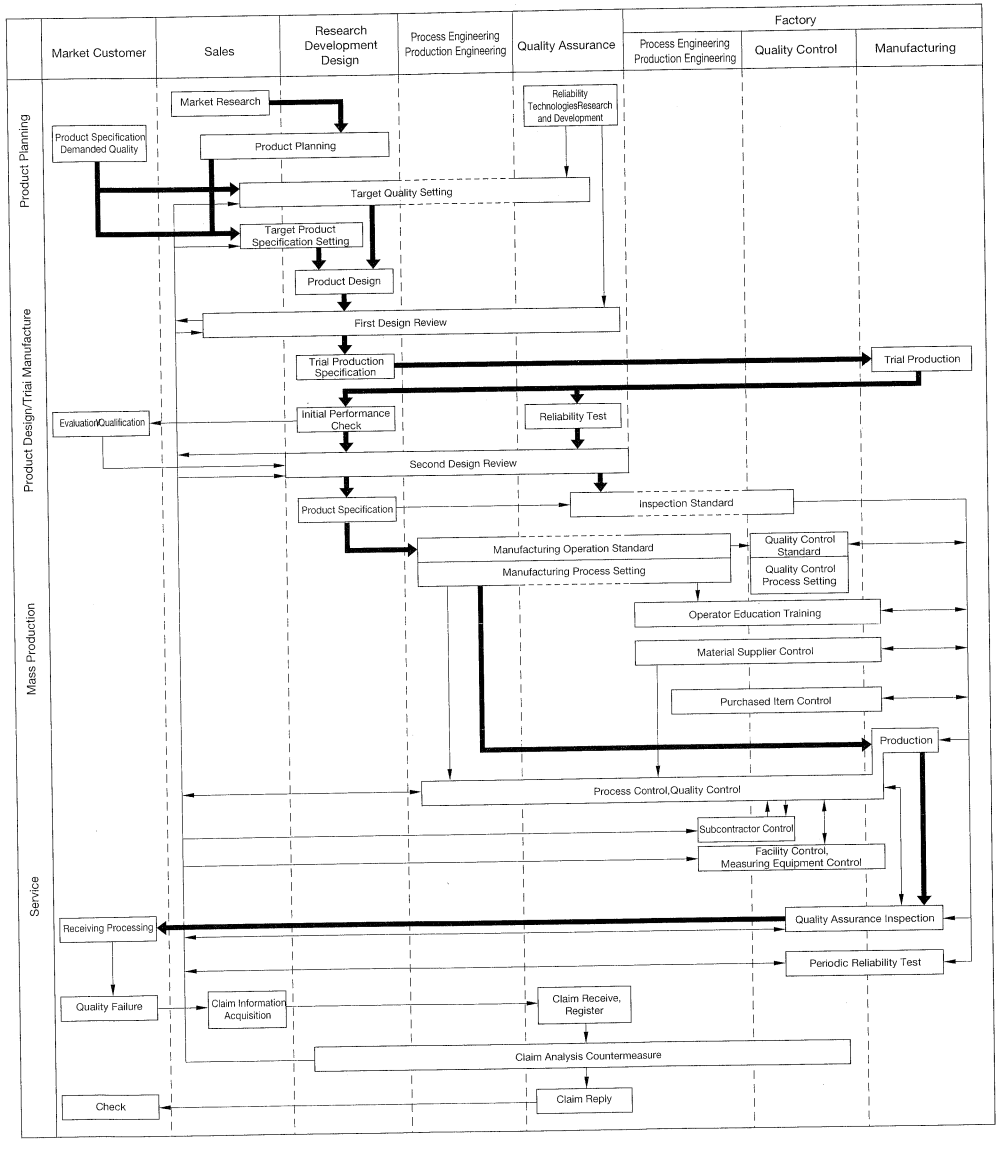
In the mass production process, product quality and reliability is assured for each process by process quality controls. OKI also regards raw materials, manufacturing equipment, sub-contractors and manufacturing environments as important factors to assure quality and reliability for mass production steps, controlling these variables very carefully.

In this way, product quality and reliability is completely assured for each design and mass production step. We also perform quality assurance inspection before shipping products to customers. This is the final quality and reliability assurance check of each process. Initial characteristics, environment durability, etc. are checked by a sampling test. Since this inspection also aims toward understanding the stability of a process, reliability is evaluated periodically.

After-sale service, available to customers after a product is shipped, is a matter which receives special attention from OKI. It is necessary to establish a system that quickly deals with customer problems all the time. OKI has established a system in which each department, including sales, design, technology and factory departments, can systematically deal with problems along with the quality assurance department.

In the quality assurance department, we are trying to maintain and improve quality by totalizing and analyzing the achievements in quality in the market of OKI products and then feeding back the result to related departments. The quality assurance system outlined above is shown in Figure 1, and contents of the system are explained in the subsequent sections.

Figure1: Quality Assurance System



2. Quality Assurance and Design Steps

2.1 Product Authorization

OKI establishes the product authorization system for newly developed and designed products. Before determining mass production for a designed product, OKI checks performance ratings and quality reliability studies by having two design review stages.
When the basic design that includes circuit, process and package is completed, the first design review meeting is held. At this meeting the basic specifications of a product, customer demanded specifications, target quality, costs, and a development/mass production schedule are examined. If a product passes this first design review, an initial performance check and reliability test are performed on a prototype. A second design review meeting studies various data acquired by these tests. At that meeting, product specifications, initial performance check results, reliability test results, trial manufacture achievements, customer evaluation results, and the preparation status of various standard documents are examined. Only products that pass this design review are qualified for mass production.

2.2 Reliability Testing

OKI uses methods specified in "JIS C 7022", "MIL-STD-883, and "IEC pub. 749" for reliability testing.
Also, target reliability ranks are established according to the use and use environment of OKI products.
The reliability tests are conducted according to individual ranks.

3. Statistical Process Control (SPC) in Manufacturing

3.1 Purchased Item Control

When purchasing parts, material and partially finished goods, OKI basically purchases items with quality assured by suppliers and subcontractors. For this, it is indispensable to maintain and improve the quality control levels of suppliers and subcontractors. OKI maintains and improves quality by holding periodic meetings and factory audits for sources. SPC information from suppliers and subcontractors is understood in conjunction with OKI's SPC activities. In this way, continuous quality improvement activities are developed.
Purchased parts and materials are delivered and stored based on individually specified delivery specifications and storage conditions. When using parts and materials, first-in-first-out control is maintained, and a history of materials used for products is recorded at each process to ensure trace-ability.

3.2 Process Quality Control

In the manufacturing process, quality is maintained and improved by checking the process conditions based on the feedback from results. OKI also performs process setting and process control according to customer demanded quality to assure precise quality. Critical quality characteristics, check control items, and control procedures are re-examined periodically.
OKI also pays attention to the environment as a factor that influences quality in a process. Deionized water control, particle control, temperature and humidity control, ESD (electrostatic discharge) control, and storage conditions at each process are standardized to assure quality.
For critical quality characteristics that strongly influence initial quality and reliability, OKI uses control charts to maintain a stable process status and process capability. Abnormalities detected by control charts are managed based on abnormality processing rules. Appropriate countermeasures are performed.

4. Quality Assurance Inspection, Periodic Reliability Test

Quality assurance inspection (Group A inspection) is carried out before shipment to check initial quality.
OKI sets quality assurance inspection standards according to the quality level demanded by customers. The quality at shipment is checked by these standards.
Inspection results are stored and managed for the period specified by company standard.
Products that passed inspection are stored in a temperature and humidity controlled area as a finished lot by lot units, under a first-in-first-out control system.
A periodic reliability test is performed aiming at continuously improving mass-produced products, including Group B test which evaluates the environmental durability by applying thermal and mechanical stress and Group C test which evaluates the durability of products by applying thermal stress for a long term.
OKI sets the test items and contents according to the demanded reliability level by wafer process and by package type.

5. Abnormality Processing

The process shown in Figure 2 is performed promptly when an abnormality is discovered at an in-process inspection and at a quality assurance inspection.

6. Claim Processing

OKI is taking all possible measures to maintain and improve quality and reliability as mentioned above. However, if a failure occurs after shipment, OKI quickly processes it as shown in Figure 3.

Figure 2: In-Process Quality Failure Processing Flow

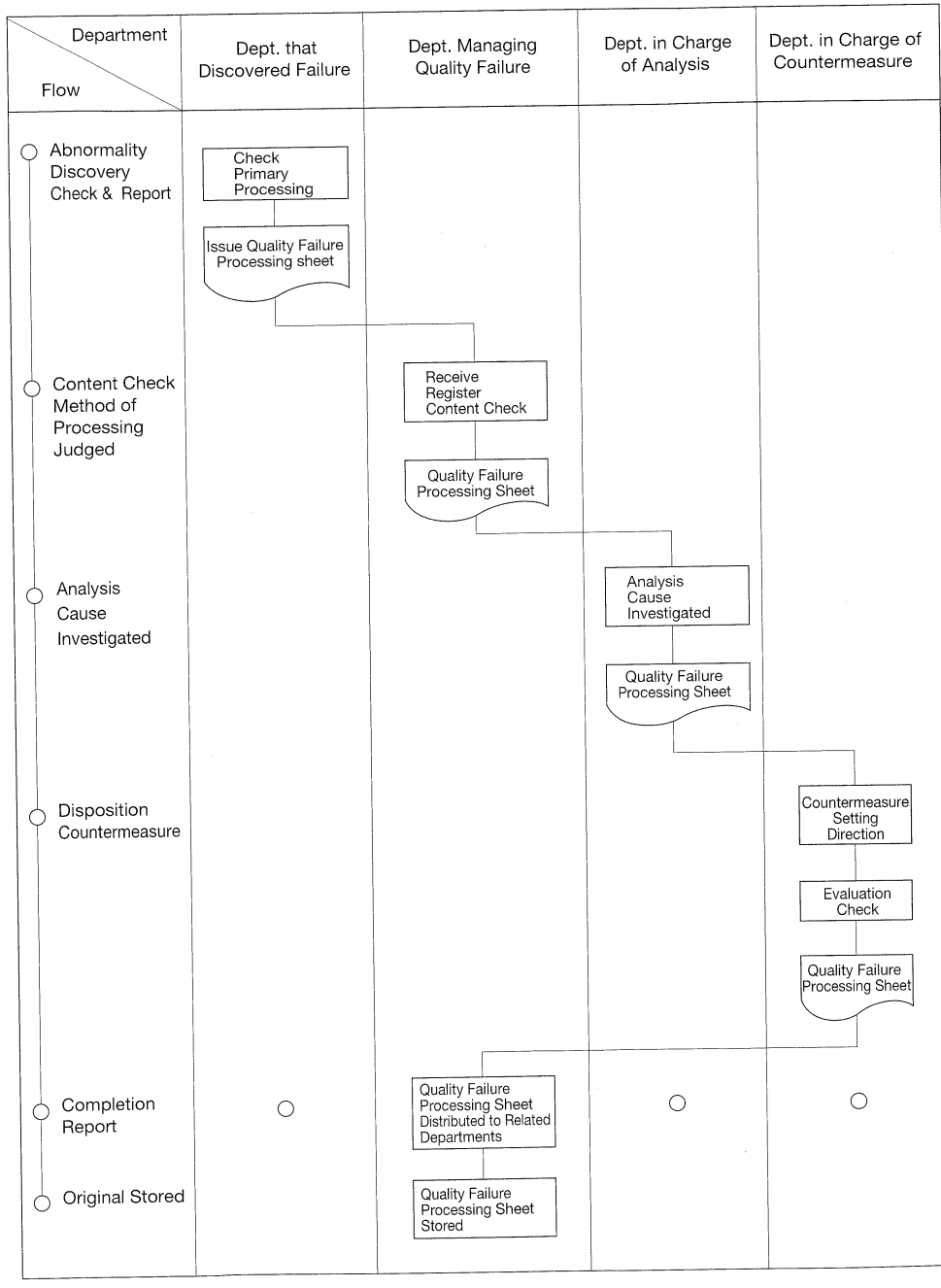
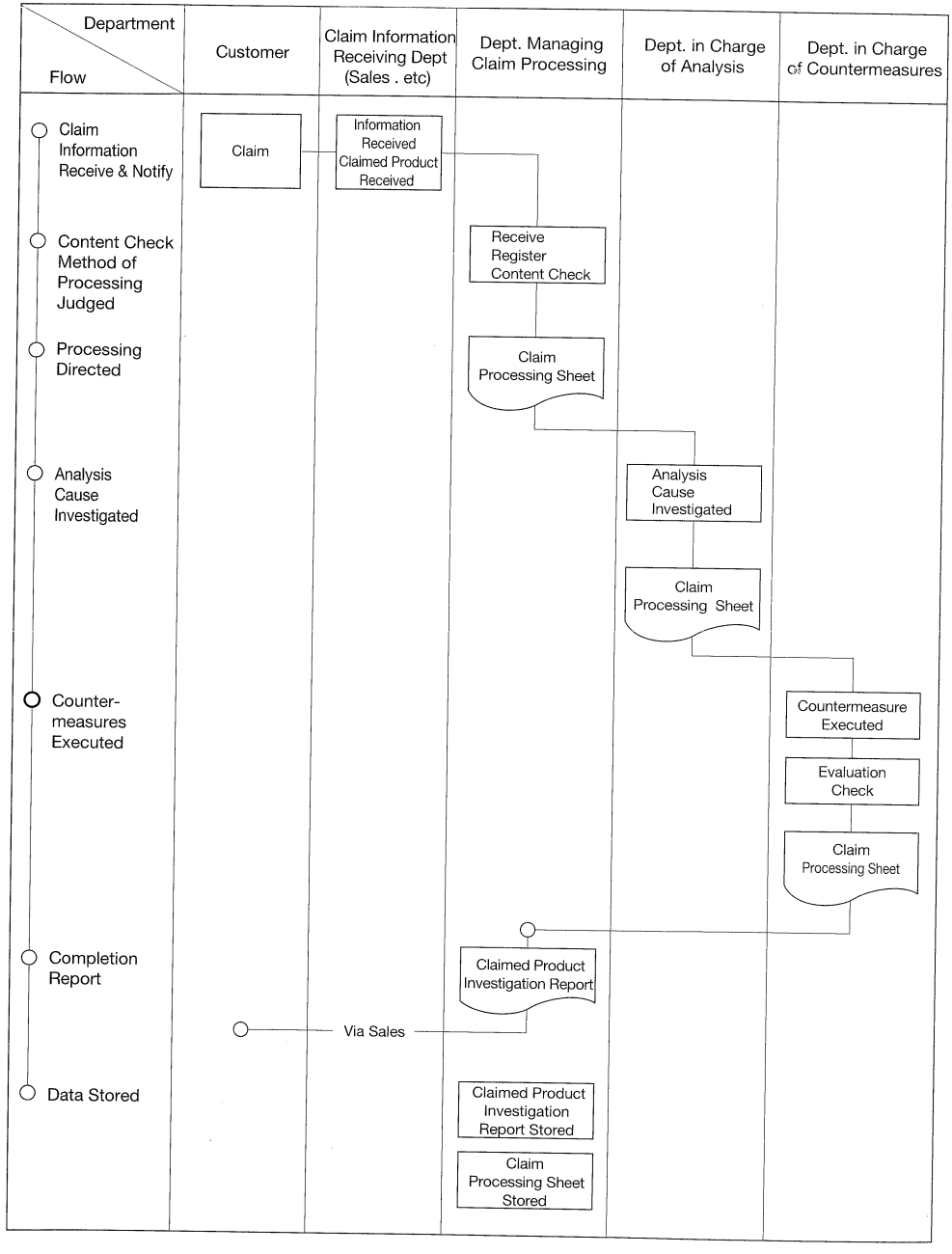


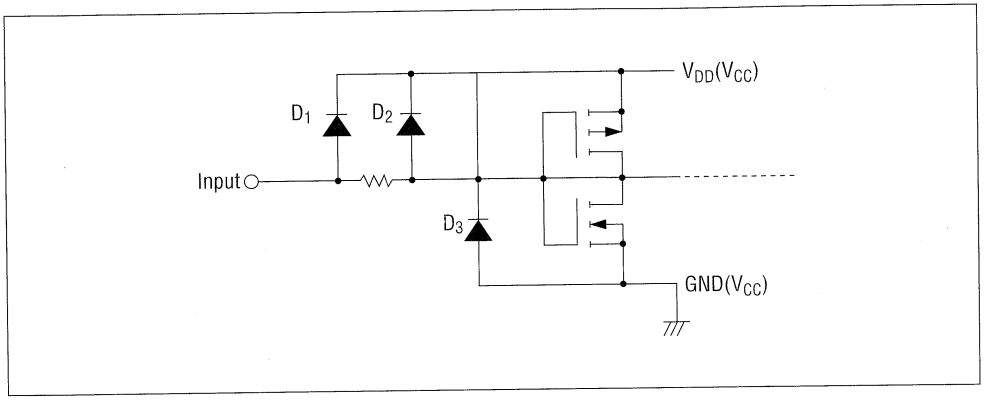
Figure 3: Claim Processing Flow



♦ NOTES ON USAGE

1. INTRODUCTION

CMOS IC chips are widely used in digital equipment due to their low power dissipation, high degree of margin for noise and wide operating power supply range. However, CMOS IC chips need to be handled carefully because of the latch-up, presence of input pins not in use, and other characteristics specific to them. Carefully read notes on use of Oki's CMOS IC chips described below before using them.



When the input voltage drops below the GND level, forward current flows in protection diode D_3, preventing a high negative voltage from being applied to the gates. When the input becomes higher than V_{DD}, forward current flows in D_1 and D_2, preventing a high positive voltage from being applied to the gates.
The input protection diode is designed so that current flows through it when necessary. Take care so that current does not flow through it during normal operation. Since the protection circuit is not enough for protection against all static electricity inputs, observe the notes described below.

2. COUNTERMEASURE AGAINST STATIC ELECTRICITY

2.1 Input Protection Circuit

The internal gate electrode of a CMOS IC chip, connected to input pins, are insulated from the substrate by thin oxide films. This assures high input impedance characteristics with low leak current. When a high voltage such as static electricity is applied, however, a dielectric breakdown may occur at a gate. To prevent this, input protection circuits are incorporated in Oki's CMOS IC chips. (Note that these input protection circuits are not provided for some special input pins.)

2.2 Transportation and Storage

Before Oki's CMOS IC chips are delivered, they are inserted in a special case such as an antistatic magazine, conductive magazine, antistatic pallet, or conductive pallet so that high voltage due to static electricity is not applied to input pins. When storing or transporting CMOS IC chips after delivery, be sure to place them in the magazine or pallet.

2.3 Board Mounting

It is necessary, therefore, to observe the following precautionary measures.

(1) Countermeasure for static electricity discharge from the body.
- Use a write-strap to ground the body.
- Place a conductive mat (10^6 Ωcm) on the work table where devices are handled.
- Put a conductive sheet on the floor and wear conductive shoes.
- Wear antistatic clothes.

The conductive mat and floor sheet should be grounded to the static electricity earth.

(2) Countermeasure for static electricity discharge from devices.
- Avoid processes which may cause friction to devices.
- Make sure insulators to charge static electricity should not be placed near devices.
- Avoid touching the leads of devices with metal parts.
- When using a soldering iron, use the soldering iron of JIS A class (insulation resistance 10 MΩ or more) whose the leakage current is little and ground it.

Refer to Oki's Package Information Data Book for detail.

3. BOARD MOUNTING PRECAUTIONS

3.1 Package Mounting

Take care of the following points when mounting a board.

(1) Reflow and wave soldering (flow soldering)
- There are products which require or do not require the damp proofed package.
- The allowable reflow condition differs depending on product.

When using the standard infrared reflow, the typical condition is: reflow twice within 10 seconds at the package surface temperature of 240°C.
When wave soldering is used, the condition is: twice within 10 seconds at the package surface temperature of 260°C.
The recommended handling conditions for each product should be strictly observed.

(2) Soldering iron
Be sure to complete lead soldering within 10 seconds at 260°C or 3 seconds at 350°C and to keep the package surface temperature within 150°C.
Refer to Oki's Package Information Data Book for detail.

4. CLEANING AFTER MOUNTING A BOARD

Recommended conditions in cleaning after mounting are shown below.

- Storage period from soldering to cleaning. It is recommended within 3 hours.
- Clearness degree control of cleaning solvent. The surface contaminated degree for the board after cleaning is recommended as less than 2.2 μg/cm^2 converted by NaCl (Omega meter).
- Recommended ultrasonic cleaning conditions
  - ★ Frequency : 28 kHz or less
  - ★ Output : 15 w/□ or less
  - ★ Time : 3 min. or less

However, hollow structure products such as ceramic packages are not recommended for ultrasonic cleaning.

- Cleaning solvent
  The following cleaning solvents are recommended as a replacement for Freon 113, because Freon 113 destroys the ozone layer.

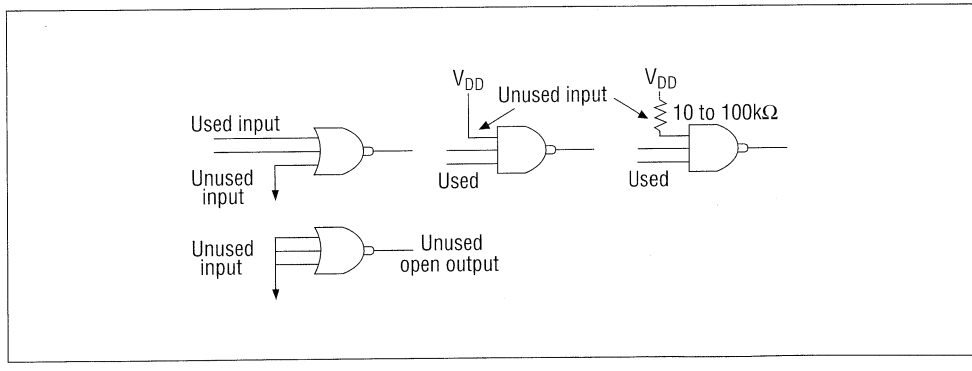
Cleaning Solvent	Type of Solvent	Company
Techno Care FRW-17	Silicone	Toshiba Corp.
Cleanthrough 750H	Water	Kao Corp.
BIOACT EC-7	Terpene	Alphametals Inc.

- No cleaning
  The insulation failure and characteristic deterioration may be caused by flux residues and solder balls.
  Therefore, select proper mounting condition such as the choice of solder parts.
  Refer to Oki's Package Information Data Book for detail.

5. CIRCUIT DESIGN AND CONNECTION TO EXTERNAL CIRCUITS

5.1 Treatment of Input Pins

CMOS IC chip inputs are voltage-driven and impedances are very high. Therefore, if input pins not in use are left open, charged voltages become unstable, making the corresponding output levels unstable. This may result in malfunction. In addition, I_{DD} (I_{CC}) at the corresponding circuit may be increased. To prevent this, be sure to connect the unused input pins to GND(V_{SS}) or V_{DD}(V_{CC}) so that an invalid logic state is obtained. When a pull-up or pull-down resistor is connected to an input pin, it can be used in the open state.



Leave the unused output pins open.

5.2 Output Shorting

A protection circuit to limit output current is not incorporated. So, do not directly connect output to V_{DD}(V_{CC}) or GND(V_{SS}). Otherwise, a high current flows, generating heat in the chip and deteriorating internal wiring. This may destroy the chip or lower the reliability.

5.3 Output Load Capacity

A capacitor may be connected to an output pin of a CMOS IC chip to remove noise by making the output waveform obtuse. In this case, take care so that the capacitance of the external capacitor does not exceed 500 pF. Otherwise, a high charging or discharging current flows in the chip. This may destroy the chip or lower the reliability.

5.4 Surge Voltage

To prevent CMOS IC chips from being destroyed by a high voltage, do not insert or pull out the active PC board on which CMOS IC chips are mounted. Check whether voltage surge occurs or not when the power supply or relays are turned on or off. If any, remove surge voltage so that the maximum IC chip rating is not exceeded or IC chips are not affected.

5.5 Power On/Off Sequence

In a CMOS circuit to which an external circuit is connected, if the power on sequences of the external power supply and CMOS power supply are not correct, the CMOS may malfunction or be destroyed. When the external power supply is turned on but the CMOS power supply is turned off, overcurrent flows into CMOS input pins connected to the external circuit. This may cause the CMOS to malfunction or be destroyed. In usual cases including transition states, set a power on/off sequence so that the CMOS power supply is first turned on and the external power supply is first turned off.

5.6 Optimum Load Capacitance of Oscillator

Values of optimum load capacitance to be connected to both pins of the oscillator are specified for each IC in the respective data sheets. However, those values are the ones when the oscillator is directly connected to the pins of IC. Therefore, care must be taken that, if a long wiring is formed on a circuit board, the optimum load capacitance will vary owing to the stray capacitance and leakage capacitance. For details, ask the manufacturer of the oscillator used.

DATA SHEET 1 VOICE SYNTHESIS ICs

MSM6585

ADPCM Voice Synthesis IC

GENERAL DESCRIPTION

The MSM6585 is an version-up product of the MSM5205 voice synthesis IC. Mainly improved points are improvement for the precision of an internal DA converter, a built-in low-pass filter, and expansion on the sampling frequency. The MSM6585 does not include a control circuit to drive an external memory similar to the MSM5205. Therefore, the MSM6585 can be connected with not only semiconductor memories, but other memory media (CD-ROM, etc.) by the control of CPU.

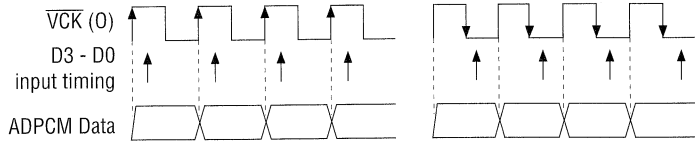
FEATURES

- 4-bit ADPCM method
- Built-in 12-bit DA converter
- Built-in low-pass filter (LPF) (–40dB/oct)
- Sampling frequencies: 4k/8k/16k/32kHz
- Master clock frequency (ceramic oscillator) : 640kHz
- Voice data synthesis : Supported by voice analysis editing tools AR76-202 and AR203
- Package options : 18-pin plastic DIP (DIP18-P-300) (Product name : MSM6585RS)
  24-pin plastic SOP (SOP24-P-430-K) (Product name : MSM6585 GS-K)

DIFFERENCES BETWEEN MSM6585 AND MSM5205

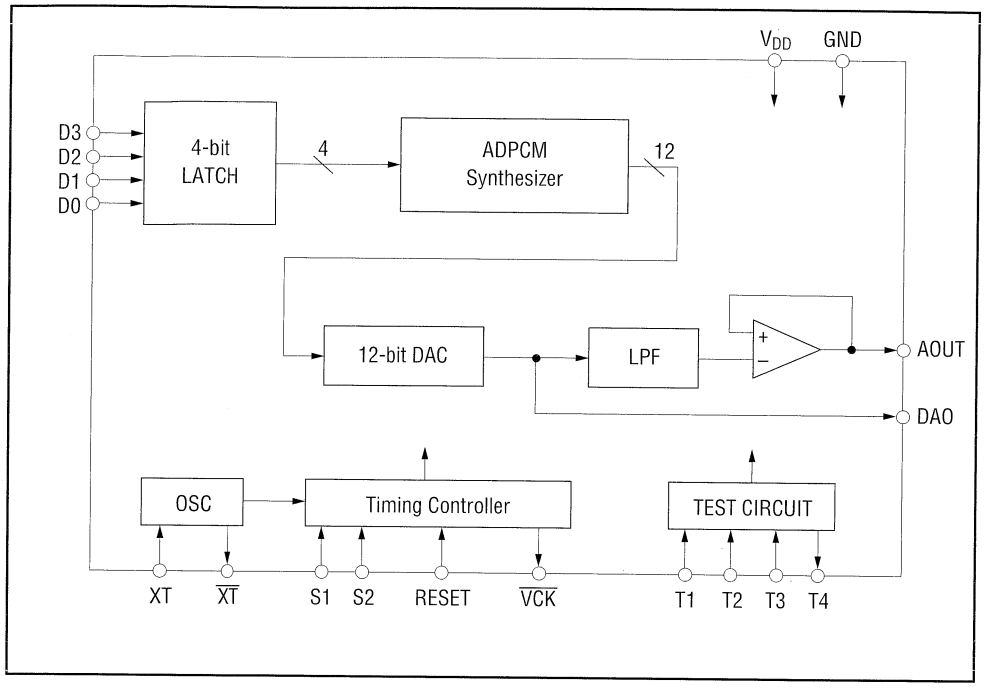
	MSM6585	MSM5205
• Master clock frequency:	640kHz	384kHz
• Sampling frequency:	4k/8k/16k/32kHz	4k/6k/8kHz
• ADPCM bit length:	4-bit	3-bit/4-bit
• DA Converter:	12-bit	10-bit
• Low-pass filter:	Included (–40dB/oct)	Not included
• Overflow preventing circuit:	Included	Not included
• Power supply voltage:	4.5 to 5.5V	3.0 to 6.0V
• Operating current consumption:	10mA	4mA
• Operating temperature:	–40 to +85°C	–30 to +70°C

• D3 to D0 input timing

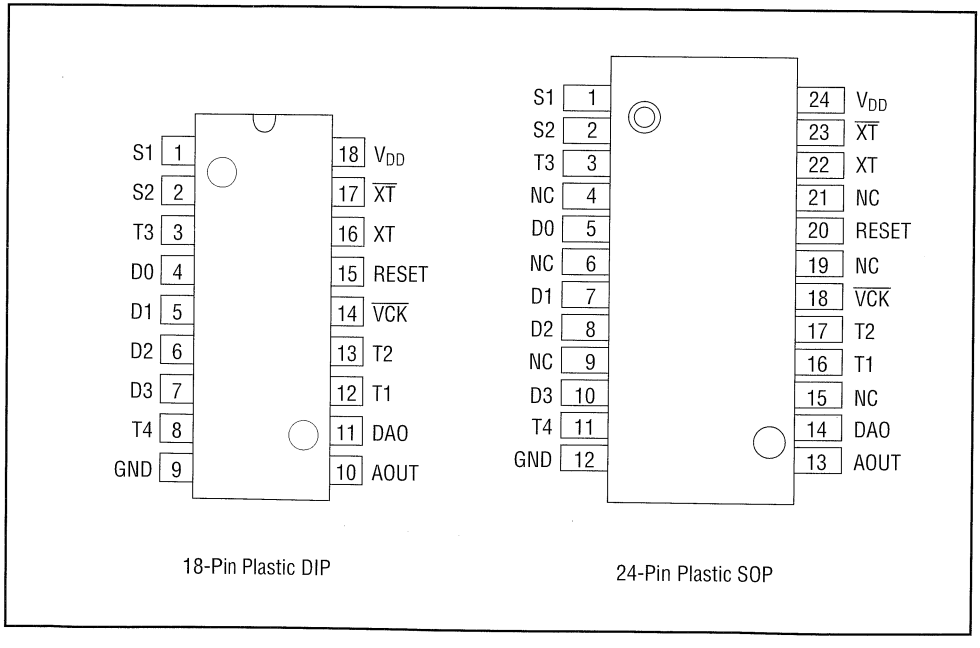


2

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Symbol	Type	Description
S1, S2	I	Pins to determine the sampling frequency. The sampling frequencies of 32k, 16k, 8k, and 4kHz can be selected by combinations. (See the sampling frequencies in FUNCTIONAL DESCRIPTION on the selection of combinations.)
T3	I	Pin to test the internal circuit. Set this pin to a high level or make it open because it has a built-in pull-up resistor.
D0~D3	I	Input pins for ADPCM data.
T4	O	Pin to test the internal circuit. Make this pin open.
GND	—	Ground pin
AOUT	O	Pin to output the analog voice from the low-pass filter. Connect a 0.01 μF capacitor to this pin. (See the AOUT connecting circuit in FUNCTIONAL DESCRIPTION on the connecting circuit.)
DA0	O	Pin to output the analog voice from the DA converter.
T1, T2	I	Pins to test the internal circuit. Set these pins to a low level or make them open because pull-down resistors are included.
$\overline{VCK}$	O	This pin outputs the sampling frequency selected by the combinations of S1 and S2. The voice synthesis starts or stops by synchronizing with $\overline{VCK}$.
RESET	I	Reset pin. The voice synthesis circuit is initialized by synchronizing with $\overline{VCK}$. If this pin is set to a high level, the D0 to D3 data inputs are disabled by synchronizing with $\overline{VCK}$. The AOUT and DA0 pins output 1/2 V_{DD} and become the state of no voice.
XT	I	Pin to connect an oscillator. When the external clock is used, input it from this pin.
$\overline{XT}$	O	Pin to connect an oscillator. When the external clock is used, make this pin open.
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and the GND pin.

2

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0V)

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	—	+4.5 to +5.5	V
Operating Temperature	T_{op}	—	−40 to +85	°C
Master Clock Frequency	f_{OSC}	oscillator connection	640	kHz

ELECTRICAL CHARACTERISTICS

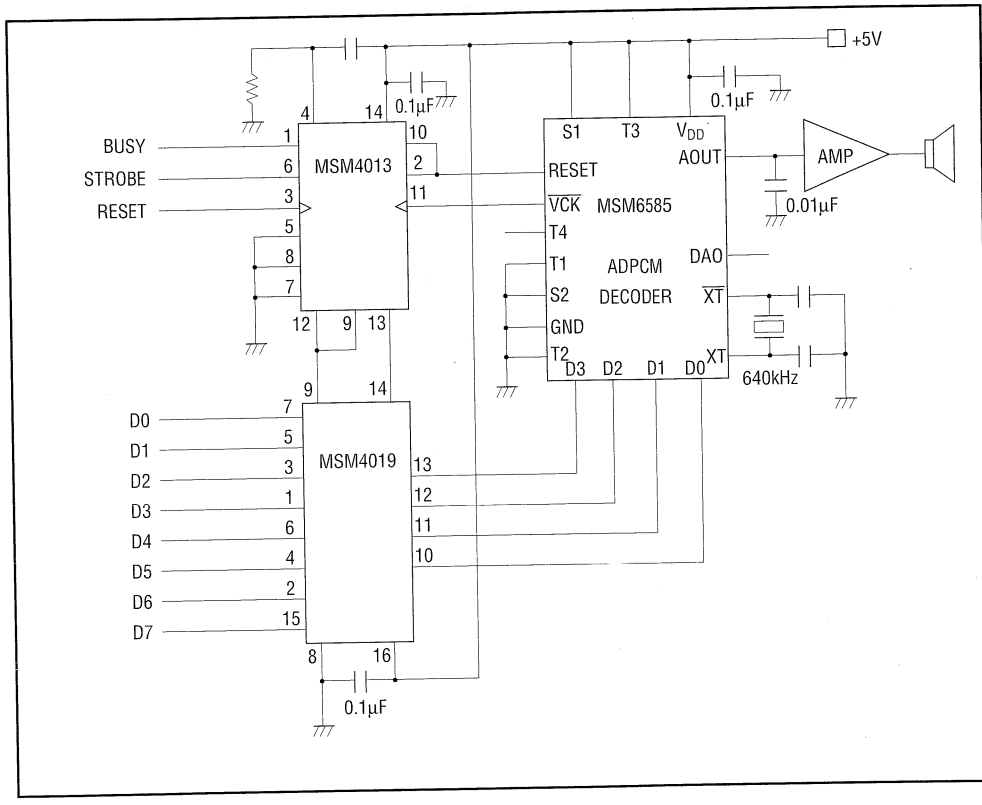
DC Characteristics

(V_{DD}=4.5 to 5.5V, GND=0V, Ta=−40 to +85°C)

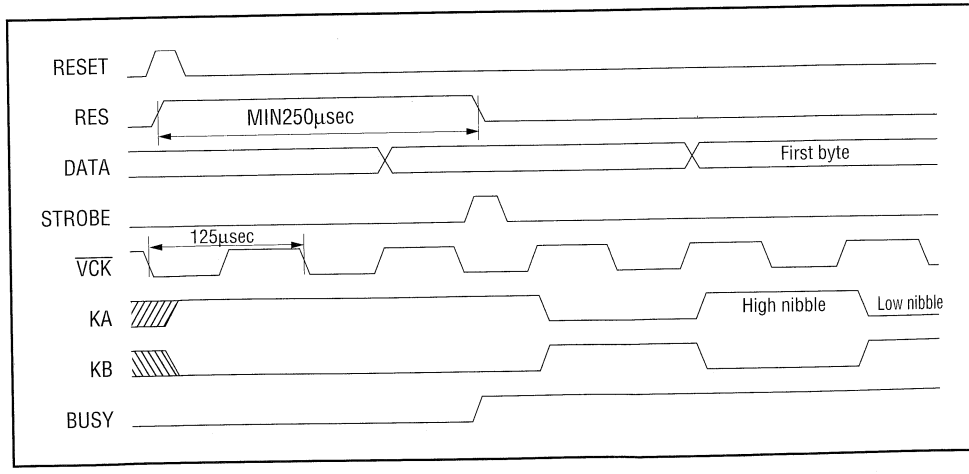
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	0.8×V_{DD}	—	V_{DD}+0.1	V
"L" Input Voltage	V_{IL}	—	−0.1	—	0.2×V_{DD}	V
"H" Output Voltage	V_{OH}	VCK: I_{OH} = −40μA	V_{DD}−0.4	—	—	V
"L" Output Voltage	V_{OL}	VCK: I_{OL} = 40μA	—	—	0.4	V
"H" Input Current	I_{IH1}	T1, T2, RESET: V_{IH} = V_{DD}	20	150	400	μA
"H" Input Current	I_{IH2}	S1, S2, D0 ~ D3, T3: V_{IH} = V_{DD}	—	—	10	μA
"H" Input Current	I_{IH3}	XT: V_{IH} = V_{DD}	—	—	20	μA
"L" Input Current	I_{IL1}	T3: V_{IL} = 0V	−400	−120	−20	μA
"L" Input Current	I_{IL2}	S1, S2, D0 ~ D3, T1, T2, RESET: V_{IL}=0V	−10	—	—	μA
"L" Input Current	I_{IL3}	XT=V_{IL}=0V	−20	—	—	μA
Current Consumption	I_{DD}	f_{OSC}=640kHz, No load	—	5	10	mA
DA Output Relative Error	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
DA Output Impedance	R_{DAO}	—	10	—	40	kΩ
LPF Load Resistance	R_{AOUT}	—	50	—	—	kΩ

APPLICATION CIRCUITS

Centronics Interface Circuit (sampling frequency : 8kHz)



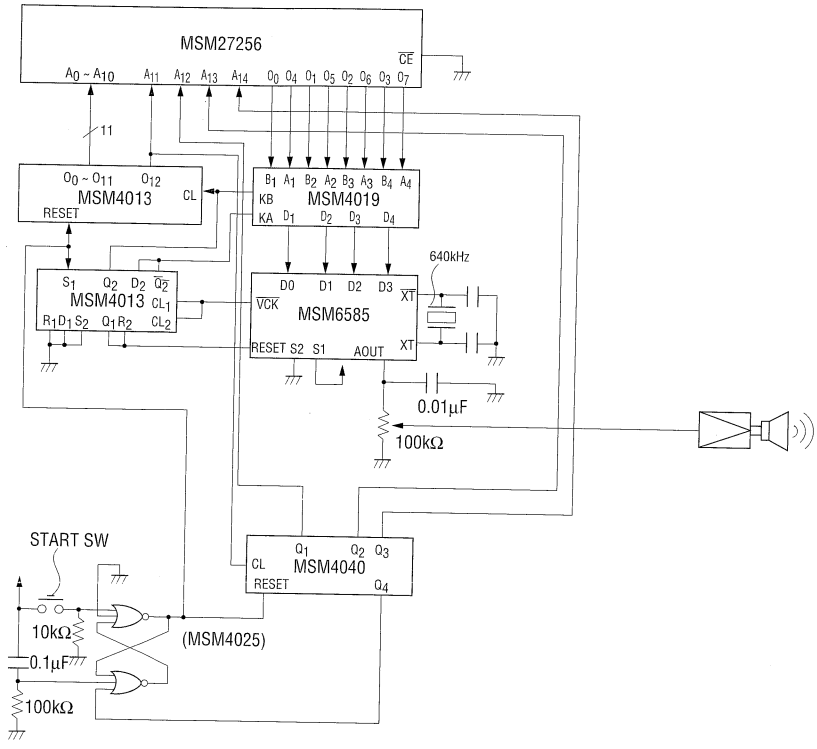
Centronics Timing Chart



Example of Interface Circuit with 256K-bit EPROM

The circuit example and timing diagram that used the 256K-bit EPROM are shown below.

2



MSM6295

4-Channel Mixing ADPCM Voice Synthesis IC

GENERAL DESCRIPTION

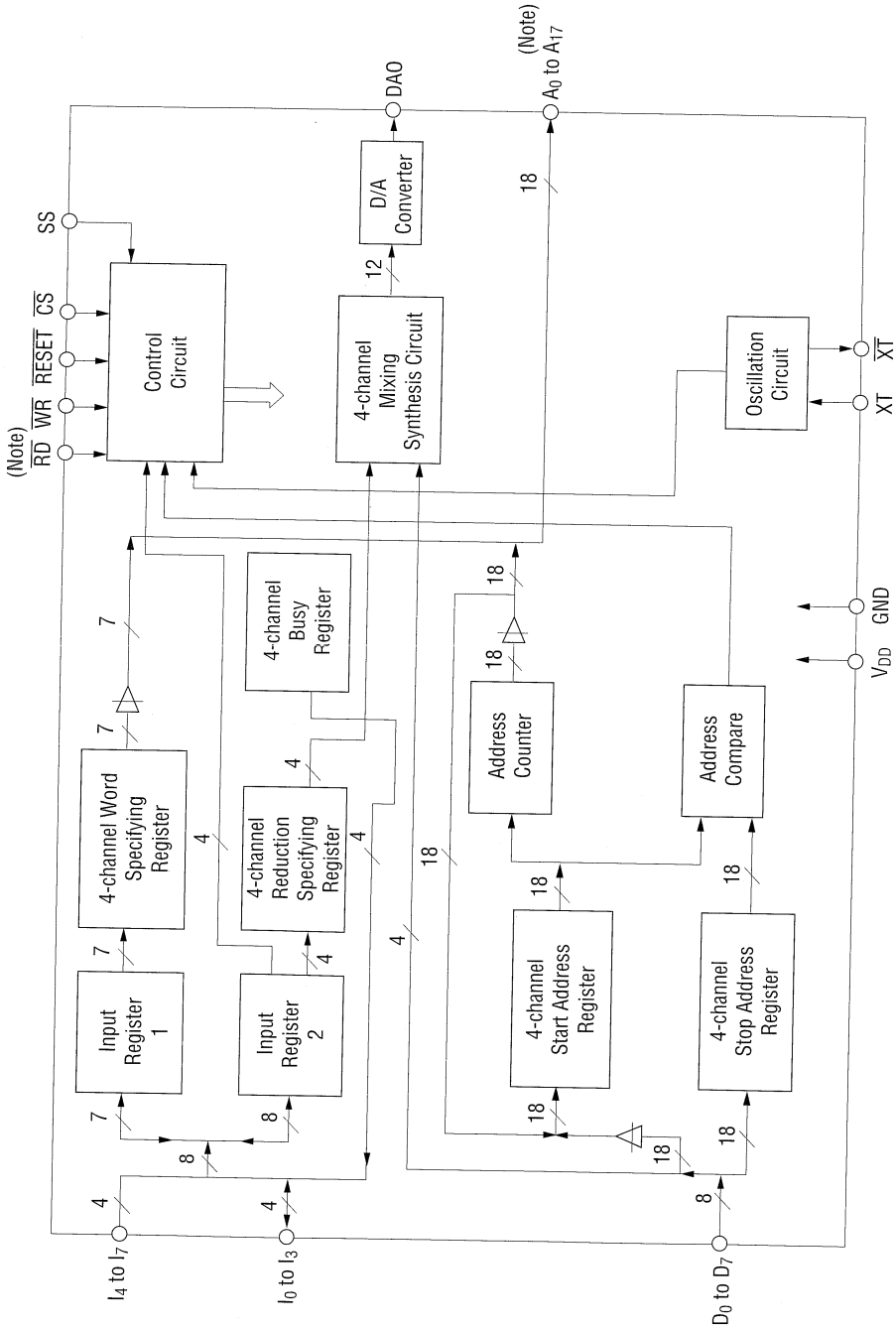
The MSM6295 can access an external ROM, where voice or sound effects data is stored. The maximum external ROM size is 256 Kbytes.
The MSM6295 has a 4-channel synthesis stage which allows the simultaneous playback of four different channels. It is used to have a voice with BGM (background music) effect, instrumental sound, echo, etc.

FEATURES

- 4-bit ADPCM method
- External ROM capacity: MSM6295GS-K/-2K: 2 Mbits (Max.)
  MSM6295VRS: 1 Mbit (Max.)
- Interface with common CPU and MPU
- Sampling frequency: 6.4 kHz and 8 kHz (@1.056 MHz clock)
  25.6 kHz and 32 kHz (@4.224 MHz clock)
- Voice level attenuation: 0dB to -24dB (9 steps)
  Attenuation on each channel: -3dB/step
- Low power CMOS process
- 5 V single power supply
- Number of mixing channels: 4 (Max.)
- Package options:
  44-pin plastic QFP (QFP44-P-910-K) (Product name: MSM6295GS-K)
  44-pin plastic QFP (QFP44-P-910-2K) (Product name: MSM6295GS-2K)
  42-pin plastic DIP (DIP42-P-600) (Product name: MSM6295VRS) (Note)

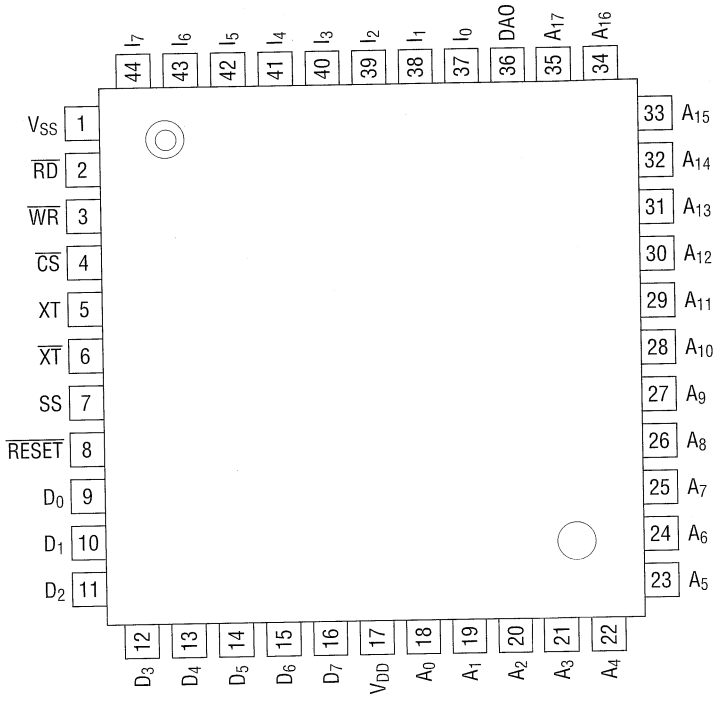
Note: Since the 42-pin DIP type MSM6295VRS does not have Pin A17, the external ROM capacity is limited to up to 1 Mbit. Moreover, since the IC does not have the $\overline{RD}$ pin either, the busy status cannot be read.

BLOCK DIAGRAM



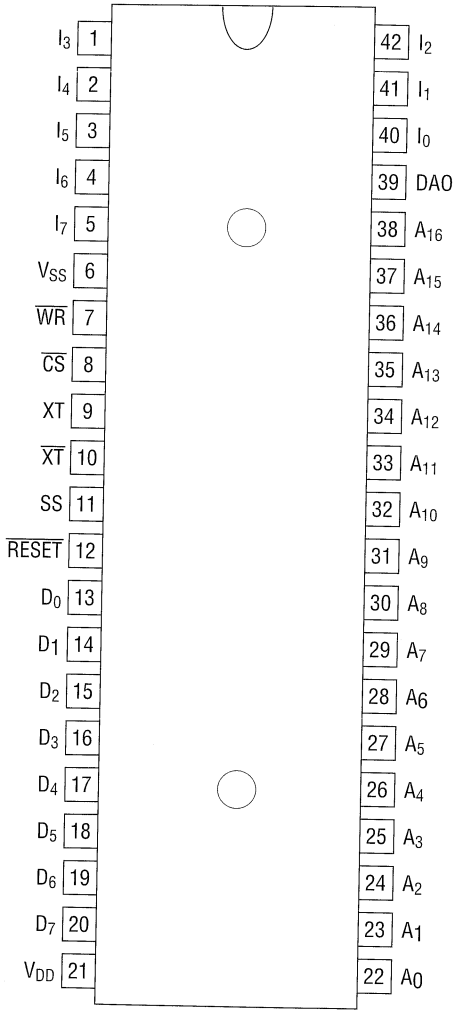
Note: The MSM6295VRS does not have pins $\overline{RD}$ and A17.

PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

2



42-Pin Plastic DIP

PIN DESCRIPTION

Pin	Symbol	Type	Description
37 38 39 40 41 42 43 44	I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7	I/O I/O I/O I/O I I I I	Instruction bus and condition outputs These pins are inputs for phrase specification. Maximum number of phrases is 127. I_0 to I_3 pins are also outputs of the operating state, busy state, for channels 1 to 4 and are further used to select the channel attenuation rate.
3	$\overline{WR}$	I	Write enable input Data is written on the data bus of I_0 to I_7. The data is written when $\overline{WR}$ goes low.
2	$\overline{RD}$ (Note)	I	Read enable input The output busy state of channels 1 to 4 on the data bus of I_0 to I_3, can be read using this input. A high level indicates busy.
4	$\overline{CS}$	I	Chip select input Input "L" level either when $\overline{WR}$ signal is input or when $\overline{RD}$ signal is input.
8	$\overline{RESET}$	I	Reset input Reset condition is available by inputting "L" level. All functions are suspended during reset.
18 to 35	A_0 to A_{17} (Note)	I to I	Address outputs These pins are to address the external ROM in which voice data is stored.
9 to 16	D_0 to D_7	I to I	Voice data inputs
7	SS	I	Sampling frequency select input When oscillation frequency is 1.056 MHz or 4.224 MHz, the following choices are available by inputting "H" level or "L" level to SS.

	SS = "H"	SS = "L"
Oscillation frequency 1.056 MHz	8 kHz	6.4 kHz
Oscillation frequency 4.224 MHz	32 kHz	25.6 kHz

36	DAO	O	Voice synthesis output Voice synthesized analog signal is output from this pin.
5	XT	I	Crystal oscillator pin
6	$\overline{XT}$	O	Crystal oscillator pin
17	V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 µF or more between this pin and the V_{SS} pin.
1	V_{SS}	—	Ground

Note: The MSM6295VRS does not have the $\overline{RD}$ and A17 pins.

2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	V_{SS} = 0 V	4.5 to +5.5	V
Operating Temperature	T_{op}	V_{SS} = 0 V	−40 to +85	°C
Oscillation Frequency	f_{OSC}	V_{SS} = 0 V	1 to 5	MHz

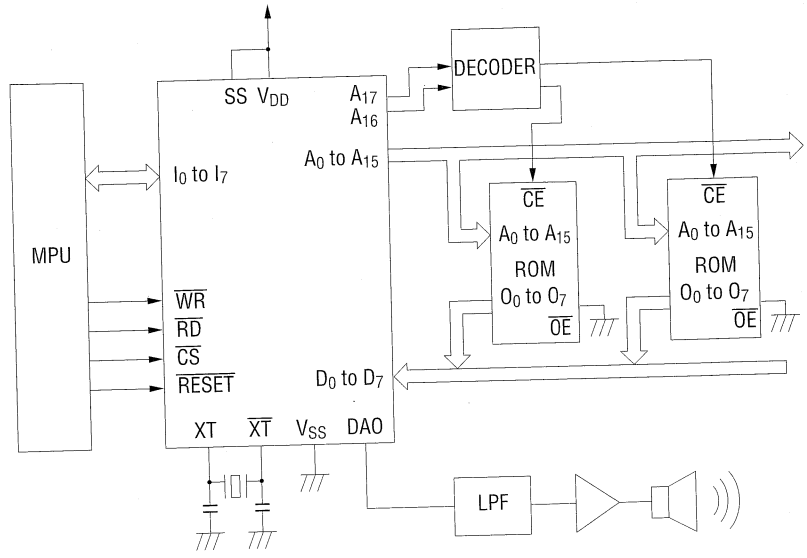
ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, Ta = −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"L" Input Current	I_{IL}	V_{IL} = V_{SS}	−10	—	—	μA
"H" Input Current	I_{IH}	V_{IH} = V_{DD}	—	—	10	
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Input Voltage	V_{IH}	—	2.4	—	—	
"L" Output Voltage	V_{OL}	I_{OL} = 0.8 mA	—	—	0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 μA	3.7	—	—	
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{OUT} \leqq V_{DD}$	−10	—	10	μA
Operating Current	I_{DD}	f_{OSC} = 5.0 MHz	—	5	10	mA
DA Output Relative error	$\|V_{DAE}\|$	No load	—	—	20	mV
DA Output Impedance	R_{DAOUT}	—	—	15	—	kΩ

APPLICATION CIRCUIT



OKI Semiconductor

MSM63P74-02/05/07/12

512-Kbit OTP BUILT-IN VOICE SYNTHESIZER

GENERAL DESCRIPTION

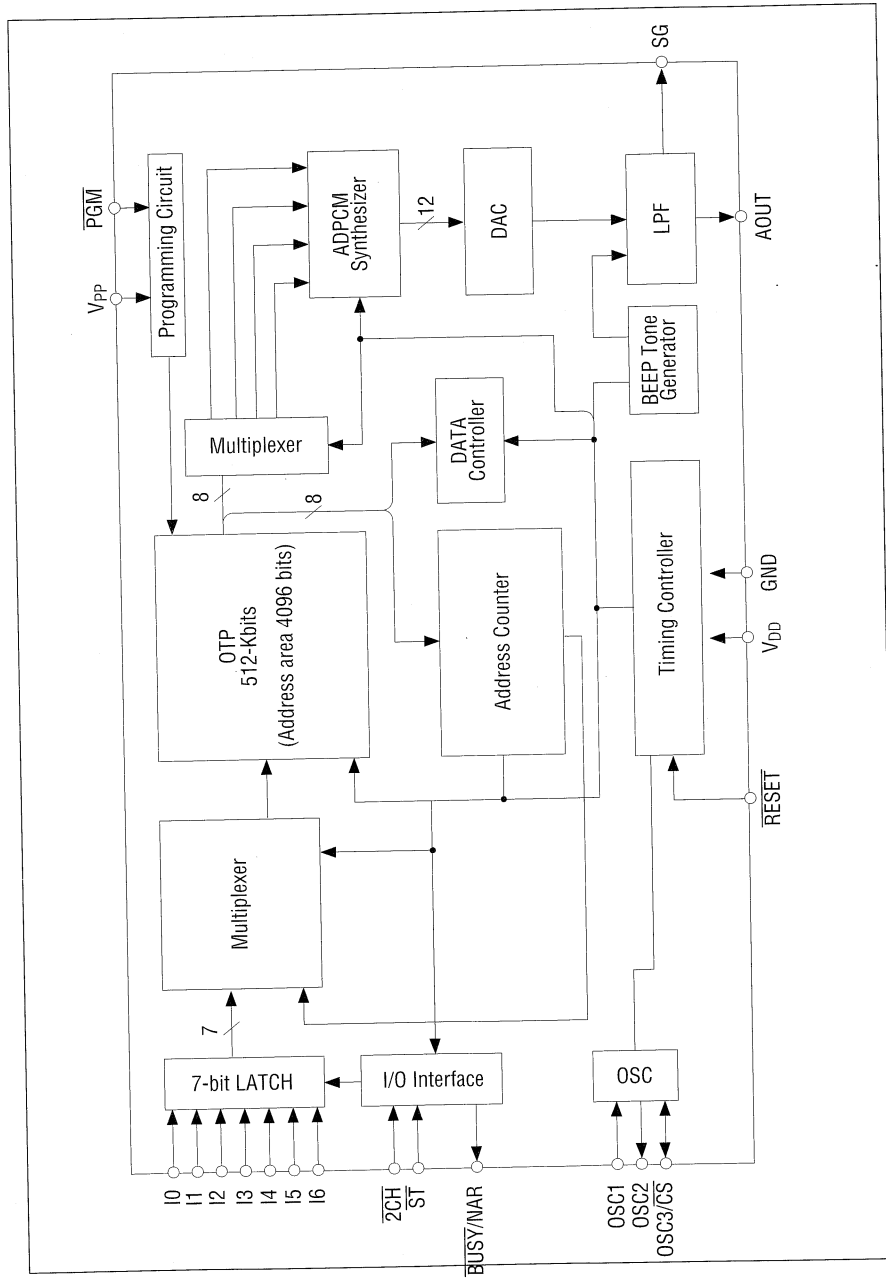
For a new circuit design, it is recommended to use the MSM66P54 described later. The MSM63P74 is a single-chip CMOS ADPCM voice synthesizer IC. It has a on-chip OTP (One time PROM) for voice data storage. This IC is compatible with the MSM6375 series. In addition to on-chip programmable ROM, it contains a 12-bit DA converter, a low-pass filter (LPF), a 2-channel mixing function, and beep tone generation. Voice analysis and voice data programming can be easily performed by the user with the OKI development tool, AR-761.

This IC is suitable for applications where programming flexibility is needed for multiple voice codes, further more for medium or small quantities and for minimum turn around times.

FEATURES

- Built-in 512K-bit OTP
- Single-chip CMOS
- 4-bit ADPCM algorithm
- Echo or 2-channel mixing functions
- Maximum number of words : 111
- Built-in 12-bit DA converter
- Built-in LPF
- Standby function
- Oscillation : RC or crystal
- Data write time (when using AR762 or AR203)
  Write and verify : approx. 55 seconds
  Verify only : approx. 15 seconds
- Data retention time : ten years min.
- Package: 20-pin DIP (DIP20-P-300-W1) (Product name : MSM63P74-××RS)
  : ×× indidates the code number

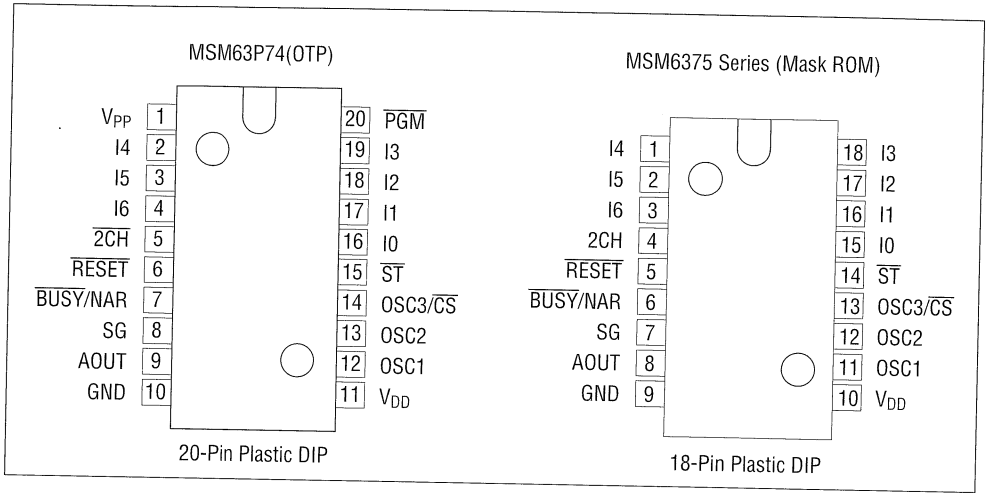
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

The pin layout of the MSM63P74 matches with that of the on-chip mask ROM series except that the MSM63P74 has two more pins than the MSM6375 series for the programming function.

These two pins (V_{PP}, $\overline{PGM}$) may be left open during playback after programming.



DIFFERENCES BETWEEN THE MSM63P74 AND THE MSM6375 SERIES

- Built-in memory (OTP)
- DC characteristics
- The values of external R and C for RC oscillation.
- Mask bonding options (02/05/07/12)
  Refer to CODE OPTION described later.
- Pin layout
- Maximum sampling frequency 16 kHz
- 20-pin Plastic DIP

PIN DESCRIPTIONS

Symbol	Type	Description
I0-I6	I	**Phrase Address Inputs**.A designed phrase can be selected for playback. The code at I0-I6 when the $\overline{ST}$ pulse goes "L" level is input and latched at the rising edge.
$\overline{2CH}$	I	**Echo Playback.** Use for simultaneous playback of two phrase/words. Input of only the $\overline{2CH}$ pulse in 1-channel operation starts the echo playback mode. The echo delay time can be changed by the timing of the $\overline{2CH}$ pulse input. Input of the $\overline{ST}$ pulse when $\overline{2CH}$ is "L" causes 2-channel playback.
SG	O	**Voltage Stabilizer.** Connect 1 µF capacitor between this pin and the GND pin to stabilize the voltage. Connecting the capacitor to this pin improves the SN ratio of the internal LPF.
AOUT	O	**Analog voice output pin that passed the LPF**
$\overline{BUSY}$/NAR	O	**Busy/Next Address Request**. Select either the NAR signal output or the $\overline{BUSY}$ signal output. When selecting $\overline{BUSY}$, this pin maintains a "L" level during playback. When selecting NAR, the $\overline{ST}$ input in channel 1 at the "H" level becomes valid.
$\overline{RESET}$	I	**Reset**. The IC enters the standby state upon a "L" input. At this time, the oscillation stops, the LPF output (AOUT) is set to GND level and the IC is reset. This IC has a built-in power-on-reset circuit but for normal operation with power-on-reset, apply the power within 1 ms up to V_{DD}. If the power cannot be applied within 1 ms, input the $\overline{RESET}$ pulse during power-on.
GND	—	**Ground pin**
V_{DD}	—	**Power supply pin.** Insert a bypass capacitor of 0.1 µF or more between this pin and the GND pin.
OSC1	I	**Crystal Oscillator.** Use when choosing crystal oscillation as an option. **RC Connection**. Use when choosing RC oscillation. Input from this pin if external clock is used.

Symbol	Type	Description
OSC2	O	**Crystal Oscillator.** Use when choosing crystal oscillation as an option. This pin becomes a RC connection pin when choosing RC oscillation. It outputs a "L" level in the standby mode. Leave it open when using an external clock.
OSC3/$\overline{CS}$	I/O	**Oscillator/Chip Select.** This pin becomes a RC connection pin when for RC oscillation and outputs the "H" level in the standby mode. It becomes a $\overline{CS}$(CHIP SELECT) pin when for the crystal oscillation and the ST input is fetched internally. Leave $\overline{CS}$ to "L" when not needed.
$\overline{ST}$	I	**Signal Tansmission**. Voice synthesis playback starts with the falling edge of $\overline{ST}$ and addresses I0-I6 are fetched when $\overline{ST}$ is "L" level. The addresses are latched internally at the rising edge of $\overline{ST}$. Input the address of channel 1 when NAR is "H". When playing back in channel 2, it is possible to change the sound volume of channel 2 by the number of $\overline{ST}$ pulses while $\overline{2CH}$ is "L". When selecting the SW input interface, perform repeated playback by fixing $\overline{ST}$ to the "L" level.
V_{PP}	—	**Programming Power Supply.** Use for the built-in OTP. When playing back, set V_{PP}=V_{DD} or leave this pin open.
$\overline{PGM}$	I	**Interface to the Dedicated Writer,** AR761 or AR762. Set this pin to "L" or leave the pin open when playing back. This pin has a built-in pull-down resistor.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input Voltage	V_I	Ta = 25°C	−0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition		Range	Unit
Power Supply Voltage	V_{DD}	LPF selection	40 kHz ≤ fosc ≤140 kHz	+4.5 to +5.5	V
			fosc ≤ 80 kHz	+2.7 to +5.5	V
Operating Temperature	Top	—		−40 to +85	°C
Master Oscillation Frequency (Note 1)	fosc	LPF output		40 to 140	kHz

Note 1: The precision of the oscillation frequency with the optional RC oscillator depends strongly on the precision of the external R and C.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5.0 V, GND = 0 V, Ta = −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Level Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Level Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Level Output Voltage	V_{OH}	I_{OH} = −40 µA	4.6	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL} = 40 µA	—	—	0.4	V
"H" Level Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" Level Input Current 2	I_{IH2}	$V_{IN} = V_{DD}$ (applied to $\overline{PGM}$ pin)	150	—	450	µA
"L" Level Input Current	I_{IL}	V_{IL} = 0 V	−10	—	—	µA
Operating Current Consumption	I_{DD}	—	—	6	20	mA
Standby Current Consumption	I_{DS}	—	—	0.1	100	µA
Relative Precision of DA	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
LPF Load Resistance	R_{AOUT}	—	50	—	—	kΩ

DC Characteristics

(V_{DD} = 3.1 V, GND = 0 V, Ta = −40 to 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Level Input Voltage	V_{IH}	—	2.6	—	—	V
"L" Level Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Level Output Voltage	V_{OH}	I_{OH} = 10 µA	2.7	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL} = 10 µA	—	—	0.4	V
"H" Level Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	1	µA
"H" Level Input Current 2	I_{IH2}	$V_{IN} = V_{DD}$ (Applied to $\overline{PGM}$ Pin)	100	—	300	µA
"L" Level Input Current	I_{IL}	V_{IL} = 0 V	−1	—	—	µA
Operating Current Consumption	I_{DD}	—	—	3	6	mA
Standby Current Consumption	I_{DS}	—	—	0.1	100	µA
Relative Precision of DA	$\lvert V_{DAE} \rvert$	No Load	—	—	20	mV
LPF Load Resistance	R_{AOUT}	—	50	—	—	kΩ

MSM6376

ADPCM Voice Synthesis IC with External ROM

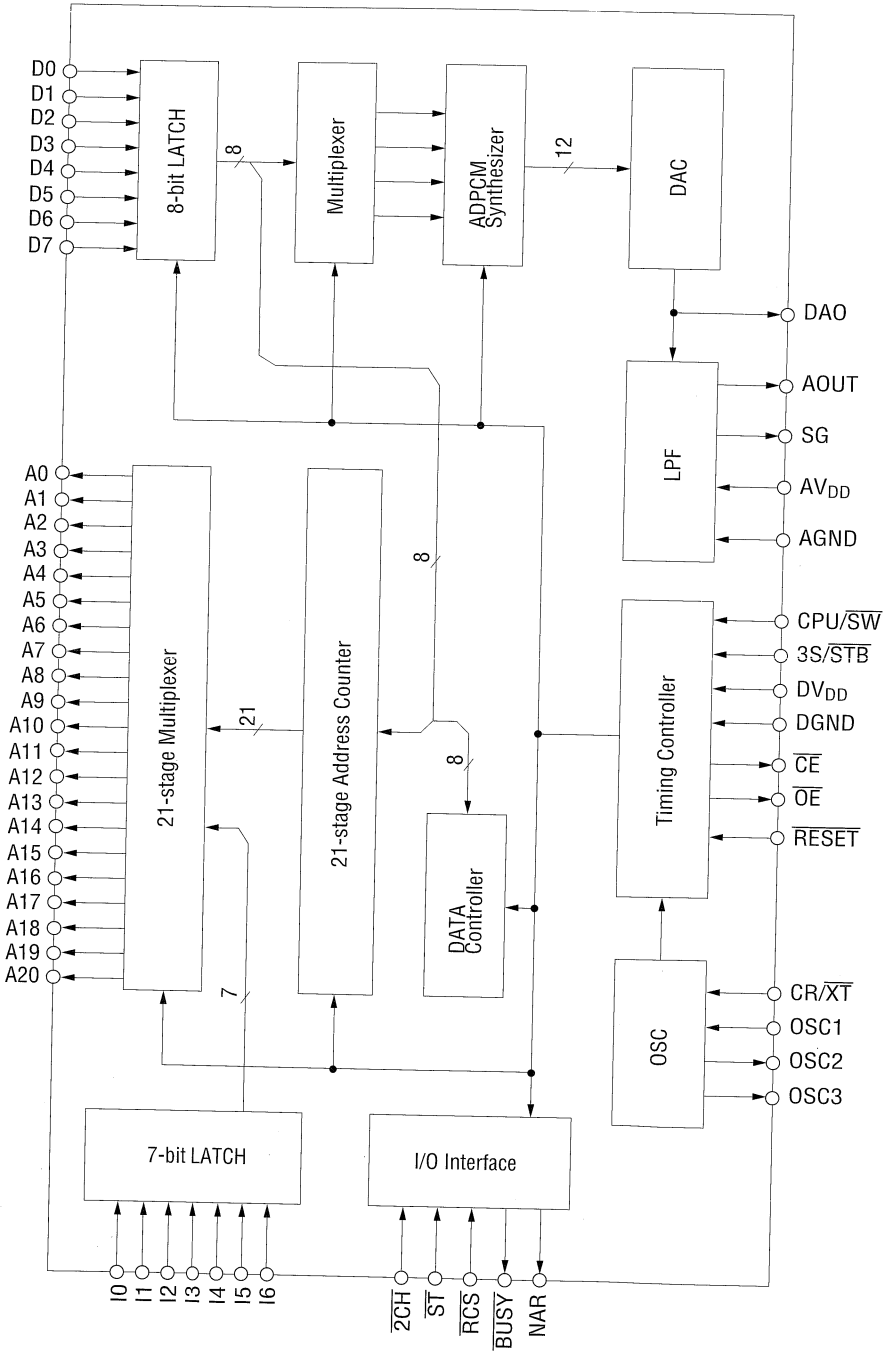
GENERAL DESCRIPTION

For a new circuit design, it is recommended to use the MSM6650 described later.
The MSM6376 is a two-channel mixing ADPCM voice synthesis IC using up to 16 Mbit external voice data storage, such as ROM and EPROM. Since it has a built-in 12-bit DA converter and low pass filter, a voice data output system can easily be configured by connecting an external power amplifier and speaker. The MSM6376 is best suited to the evaluation of MSM6375 series, which are used as voice synthesizers with built-in ROM, because the MSM6376 has the same circuit configuration as those ICs.

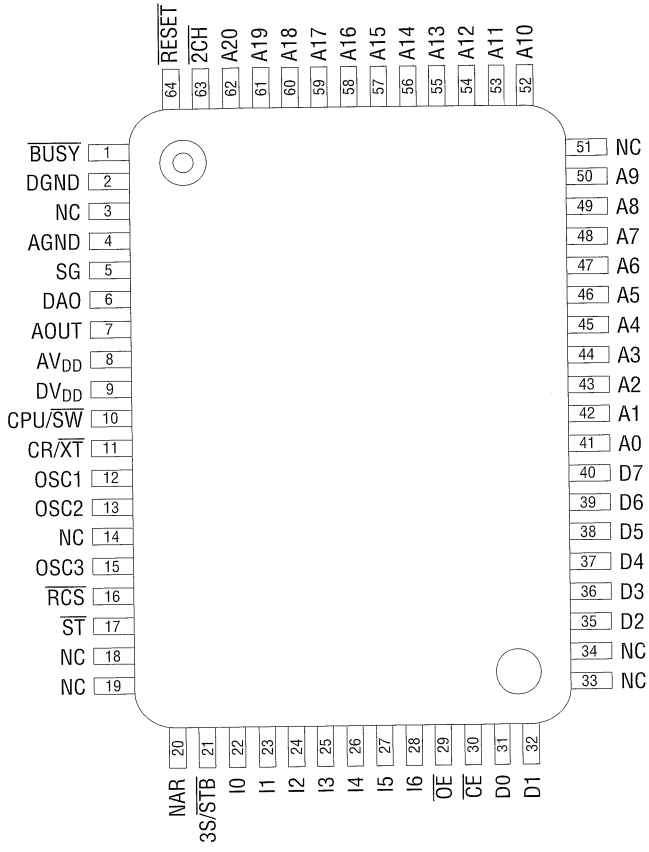
FEATURES

- External ROM capacity : Up to 16 Mbits
- 4-bit straight ADPCM method
- Echo playback and simultaneous output of two audible tones (sound volume variation for one tone in three stages)
- Output of either of two built-in BEEP tones (1 kHz and 2 kHz) by designation code (when oscillation is 64 kHz)
- Sampling frequency 4.0, 6.4 and 8.0 kHz (at oscillation of 64 kHz) up to 32 kHz is possible (at selected DA output).
- Maximum voice period of 10.9 minutes (at sampling frequency of 6.4 kHz) with 16 Mbit ROM
- Maximum number of words : 111-word
- Built-in 12-bit D/A converter of class A voltage type (with built-in pop noise suppression circuit)
- Built-in LPF with attenuation factor of –24 dB/oct
- Standby function to stop oscillation and all functions during the standby state
- Oscillation selectable between RC oscillation and crystal oscillation
- Master oscillation frequency : 40 to 140 kHz (LPF output)
  40 to 256 kHz (DAC output)
- Supply voltage : 4.5 to 5.5 V
- Package : 64-pin plastic QFP (QFP64-P-1420-BK)
  (Product name: MSM6376GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

Note: Leave the NC pin open.

PIN DESCRIPTIONS

Symbol	Type	Description
I6 to I0	I	User-specified word corresponding to the vocalized word. The code when the level of the $\overline{ST}$ pulse goes low is read, and latched as the level rises.
A20 to A0	O	Address pins for the external connection of memory. The data is output when $\overline{RCS}$ is "L".
D7 to D0	I	Input of data from external memory. The data is input when $\overline{RCS}$ is "L". Insert a pull-down resistor of about 100 kΩ to pins D7 to D0. If these pins are used at an open state, the leakage current of hundreds of microamperes may flow to a power supply pin at a standby state.
$\overline{2CH}$	I	Echo, or two different tones are played simultaneously. If $\overline{2CH}$ pulse is entered during operation in channel 1, echo is played back. Delay time for the echo can be changed according to the time of input of $\overline{2CH}$ pulse. If $\overline{ST}$ pulse is enterd when the level for CH2 is low, playback is performed in channel 2.
$\overline{ST}$	I	Data on I6 through I0 is read when their level is "L", and latched at the rise of $\overline{ST}$. Enter an address for channel 1 when the level of NAR is "H". For playback in channel 2, sound volume can be changed according to the number of $\overline{ST}$ pulses when the level of $\overline{2CH}$ is "L". In the case of SW input interface, synthesis is repeated while the level of $\overline{ST}$ is set to "L".
$\overline{RCS}$	I	Enables $\overline{ST}$ pulse to be input and the address from A20 to A0, $\overline{OE}$ and $\overline{CE}$ are output when the level is "L". When the level is "H", the address pins of A20 to A0, and $\overline{CE}$ and $\overline{OE}$ become high impedance.
$\overline{BUSY}$	O	During playback, "L" level is output.
NAR	O	When the level is "H", the next channel address can be input. This pin is a signal to indicate whether or not a 7-bit LATCH (refer to the Block Diagram) to latch addresses 16 to 10 is idle. A "H" level indicates that the 7-bit LATCH is idle.
CR/$\overline{XT}$	I	RC oscillation or crystal oscillation. If the level of CR/$\overline{XT}$ is set to "H", OSC1, OSC2, and OSC3 work as RC oscillation pins; if the level of CR/$\overline{XT}$ is set to "L", OSC1 and OSC2 serve as crystal oscillation pins, and a resistor with a resistance of about 2 MΩ is inserted between OSC1 and OSC2.

Symbol	Type	Description
OSC1	I	Crystal oscillation and RC oscillation.
OSC2	O	For crystal oscillation, leave the OSC3 pin open. If an external clock signal
OSC3	O	is to be used, it should be connected to the OSC1 pin with OSC2 and OSC3 left open.
CPU/$\overline{SW}$	I	Selection between CPU interface and SW input interface. "H" level = CPU interface. "L" level = switch interface Note: If SW input interface is selected, echo playback, and 2-channel mixing playback cannot be performed.
3S/$\overline{STB}$	I	Standby state is invoked three seconds after completion of voice synthesis if the level of the 3S pin is "H". If the level of the 3S pin is "L", the output from the DA converter remains at 1/2 V_{DD} after completion of voice synthesis.
$\overline{RESET}$	I	Reset . If the level of this pin is set to "L", the IC is put in standby state. Upon $\overline{RESET}$, oscillation is stopped, the output from the DA converter is grounded, and put to the intitial state. The M6376 has a built-in power-on reset circuit. To make the power-on resetting function reliably, raise the power supply within 1ms. If this is impossible to do, enter the $\overline{RESET}$ pulse when the power is turned on.
$\overline{CE}$	O	Timing output that controls chip enable of external memory. The signal is output when the level of $\overline{RCS}$ is "L".
$\overline{OE}$	O	Timing output that controls reading from external memory. The signal is output when the level of $\overline{RCS}$ is "L".
DAO	O	Outputs analog voice sent from the DA converter.
AOUT	O	Output of analog voice sent from the LPF.
SG	O	Improves SN ratio of LPF. To utilize the output from the LPF, connect a capacitor of about 1 µF. If the LPF is not used, make this pin open.
AV_{DD}	—	Analog power supply. Insert a bypass capacitor of 0.1 µF or more between this pin and the AGND pin.
AGND	—	Analog grounding.
DV_{DD}	—	Digital power supply. Insert a bypass capacitor of 0.1 µF or more between this pin and the DGND pin.
DGND	—	Digital grounding pin.

ABSOLUTE MAXIMUM RATINGS

(DGND = AGND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}		−0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = AGND = 0 V)

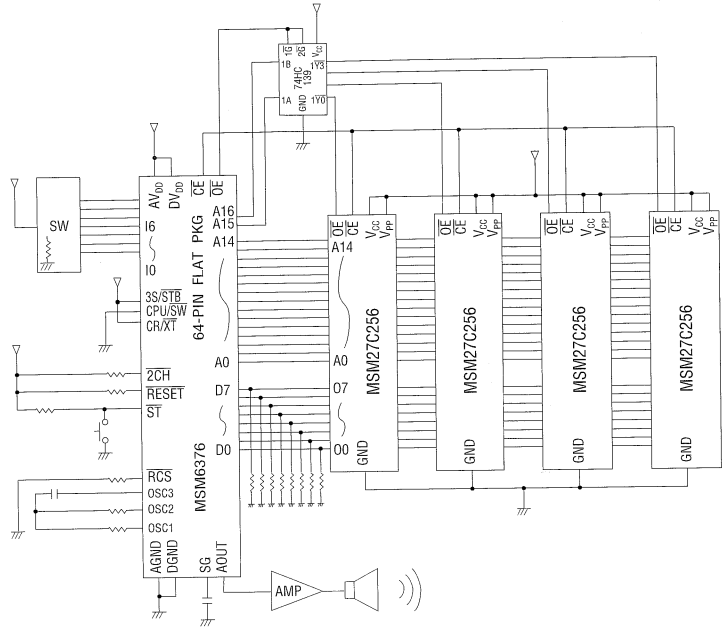
Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	—	+4.5 to +5.5	V
Operating Temperature	T_{op}	—	−40 to +85	°C
Master Oscillation Frequency	f_{OSC1}	LPF output	40 to 140	kHz
Master Oscillation Frequency	f_{OSC2}	DAC output	40 to 256	kHz
DAO Output Level	V_{OD}	No load	0 to V_{DD}	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

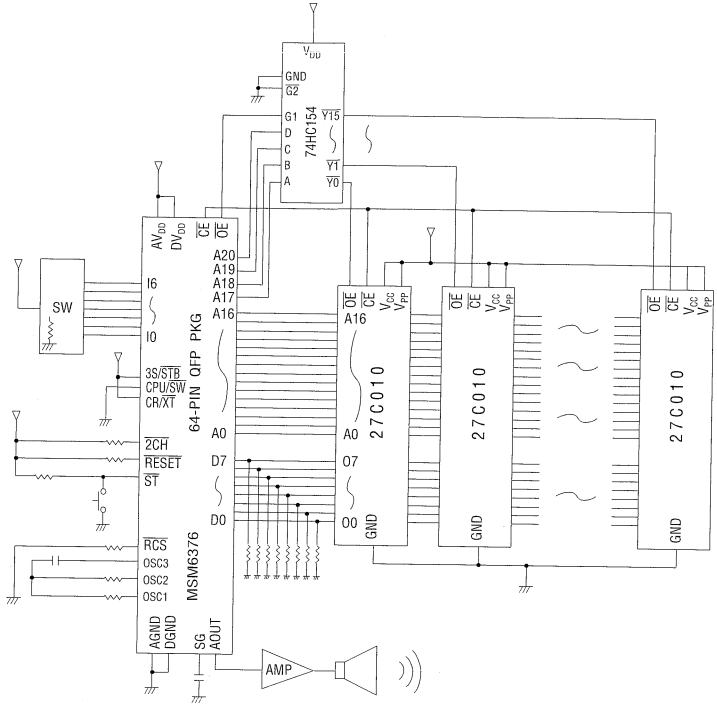
(DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta= −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	0.84 × V_{DD}	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.16 × V_{DD}	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 µA	V_{DD} − 0.4	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 40 µA	—	—	0.4	V
"H" Input Current	I_{IH}	V_{IH} = V_{DD}	—	—	10	µA
"L" Input Current	I_{IL}	V_{IL} = 0 V	−10	—	—	µA
Output Leakage Current	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}	−10	—	10	µA
Operating Current Consumption	I_{DD}	—	—	4	10	mA
Standby Current Consumption	I_{DS}	—	—	—	10	µA
Relative Precision of DA Output	$\|V_{DAE}\|$	no load	—	—	40	mV
DA Output Impedance	R_{DAO}	—	15	25	35	kΩ
LPF Load Impedance	R_{AOUT}	—	50	—	—	kΩ



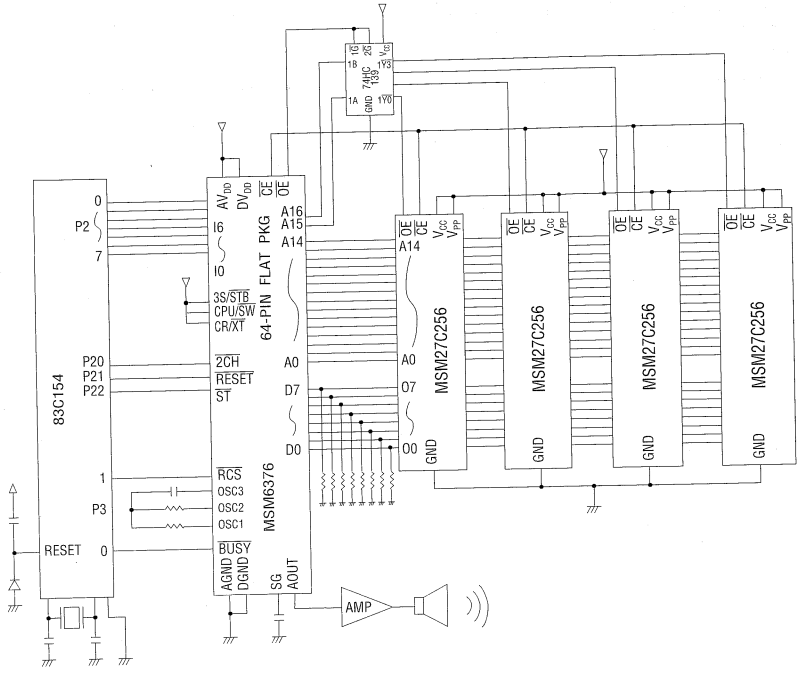
Note: Use a CMOS type 27C256 as an EPROM if possible. If an NMOS type 27256 is used, the power voltage variation of the EPROM may become a source to generate noise.

Figure 17 Example of Interface Using 4pcs. 256 Kbit EPROMs



Note: Use a CMOS type 27C010 as an EPROM if possible. If an NMOS type EPROM is used, the power voltage variation of the EPROM may become a source to generate noise.

Figure 18 Example of Interface Using 16pcs. 1 Mbit EPROMs



Note: Use a CMOS type 27C256 as an EPROM if possible. If an NMOS type 27256 is used, the power voltage variation of the EPROM may become a source to generate noise.

Figure 19 Example of Applied CPU Interface Circuit

OKI Semiconductor

MSM6378A/MSM6379

OTP ROM Built-in Voice Synthesis IC

GENERAL DESCRIPTION

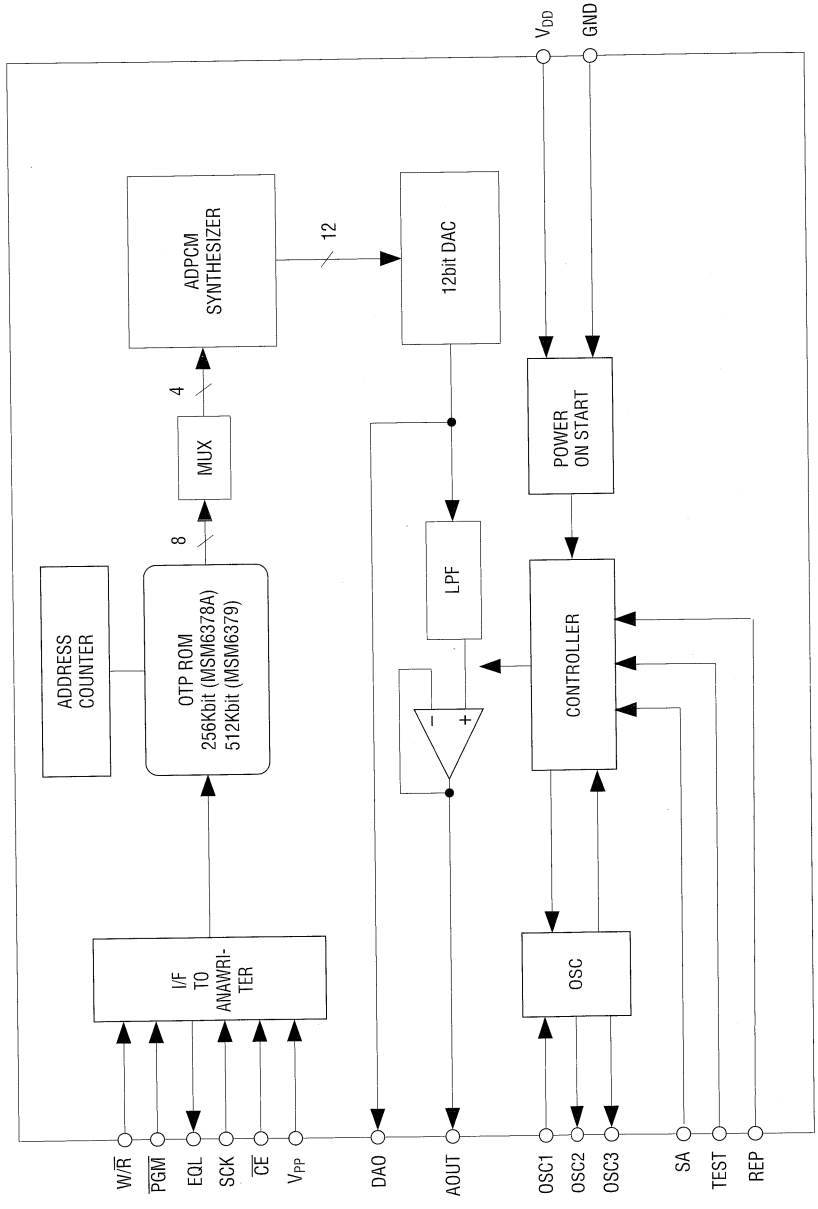
The MSM6378A/6379 is an ADPCM voice synthesis IC with a built-in one-time programmable (OTP) ROM. The MSM6378A/6379 reproduces the voice data, which the user has analyzed and recorded using the "ANAWRITER" for an exclusive use, through a speaker driving AMP and speaker. The MSM6378A/6379 can be used in voice cards, small-quantity multi-product toy line-ups, and personal use devices.

FEATURES

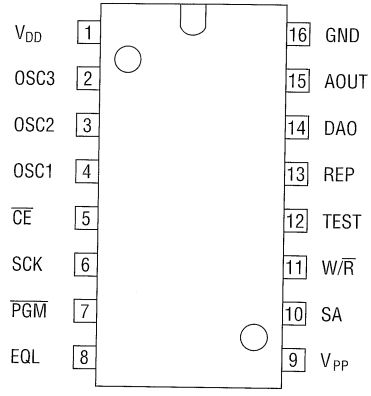
- MSM6379 : Built-in 512Kbit OTP ROM (500Kbits for recording)
- MSM6378A : Built-in 256Kbit OTP ROM (244Kbits for recording)
- 4-bit straight ADPCM method
- Built-in low pass filter
- Built-in 12-bit DA converter
- Data write time : MSM6379 16 sec
  MSM6378A 8 sec
- Oscillation system : R/C oscillation or external clock input
  (ceramic oscillation is available.)
- Oscillation frequency : 64 to 256kHz
- Sampling frequency : 4 to 16kHz (original oscillation frequency/16)
- Activation : Power on start or reactivation after one shot output
- Voice output : one-shot or repeat
- Low current consumption
- Largest voice time : MSM6379 32.0 sec (4kHz sampling)
  MSM6378A 15.6 sec (4kHz sampling)
- Number of phrases that can be output : One phrase only
- Power supply voltage : DAO pin 2.4 to 5.5V
  AOUT pin 2.7 to 5.5V ($f_{SAM} \leq 8$kHz)
  3.5 to 5.5V ($f_{SAM} \geq 10$kHz)
- Package : 16-pin plastic DIP (DIP16-P-300-W1)
  (Product name: MSM6378ARS/MSM6379RS)
  Chip

	M6378A	M6379
ANAWRITER MK2	○	×
ANAWRITER MK6	○	○
AR761/AR762	○	○
AR76-202/AR203	○	○

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



16-Pin Plastic DIP

PIN DESCRIPTION

Symbol	Type	Description
REP	I	Repeat/one-shot selection pin. In power-on or input to SA pin, one-shot is output when REP="L" and repeated voices are output when REP="H". The voice is not output so long as this pin is merely set to "H" level. This pin does not include a pull-down resistor.
SA	I	Pin to be reactivated after one-shot output. When a single pulse is applied to SA pin, the IC is reactivated on the falling edge. This pin includes a pull-down resistor.
W/$\overline{R}$	I	Interface pin for the ANAWRITER for exclusive use. Set to "L" or "open" in playback. This pin includes a pull-down resistor.
$\overline{PGM}$	I	Same as above (W/$\overline{R}$).
SCK	I	Same as above (W/$\overline{R}$).
$\overline{CE}$	I	Same as above (W/$\overline{R}$).
EQL	O	Interface pin for the ANAWRITER for exclusive use. Set to "open" in playback.
TEST	I	Internal circuit test pin. Set to "L" or "open" in playback. This pin includes a pull-down resistor.
OSC1	I	Oscillation RC connection pin or external clock input pin.
OSC2	O	Oscillation RC connection pin. Set to open to input external clock through the OSC1 pin.
OSC3	O	Same as above (OSC2).
DAO	O	DA converter output pin.
AOUT	O	LPF output pin.
V_{PP}	—	Power voltage pin for writing to the built-in OTP. Set to $V_{PP} = V_{DD}$ or "open" in playback.
V_{DD}	—	Power pin. Insert a bypass capacitor of 0.1µF or more between this pin and the GND pin.
GND	—	Ground pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	GND = 0V	DAO pin 2.4 to 5.5 AOUT pin 2.7 to 5.5 ($f_S \leqq 8$ kHz) 3.5 to 5.5 ($f_S \geqq 10$ kHz)	V
Operating Temperature	T_{op}	—	−10 to +70	°C
Oscillation Frequency	f_{OSC}	—	64 to 256	kHz

ELECTRICAL CHARACTERISTICS (V_{PP}=V_{DD} at playback)

DC Characteristics

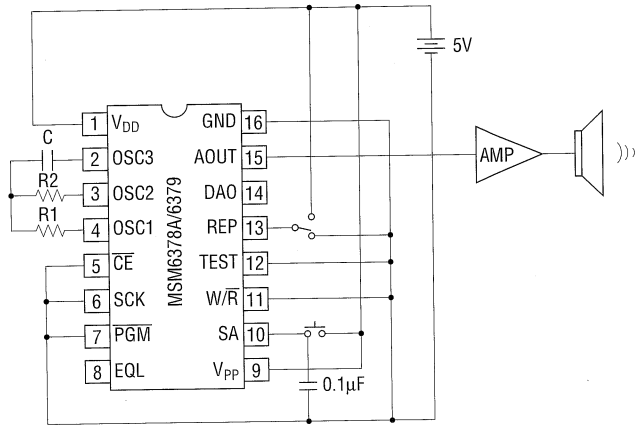
(V_{DD}=4.5 to 5.5V, GND=0V, Ta=0 to +70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
"H" Input Voltage	V_{IH}	—	0.8×V_{DD}	—	V_{DD}+0.1	V
"L" Input Voltage	V_{IL}	—	−0.1	—	0.2×V_{DD}	V
"H" Input Current 1	I_{IH1}	Applies to $\overline{CE}$, SCK, $\overline{PGM}$, SA,W/$\overline{R}$, and TEST pins	20	—	400	µA
"H" Input Current 2	I_{IH2}	Applies to OSC1 and REP pins	—	—	10	µA
"L" Input Current	I_{IL}	—	−10	—	—	µA
Operation Current Consumption	I_{DD}	—	—	7	20	mA
Standby Current Consumption	I_{DS}	—	—	0.1	10	µA
DA Output Relative Accuracy	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
DA Output Impedance	R_{DAO}	—	15	25	35	kΩ
LPF Minimum Driving Resistance	R_{AOUT}	—	50	—	—	kΩ

APPLICATION CIRCUITS

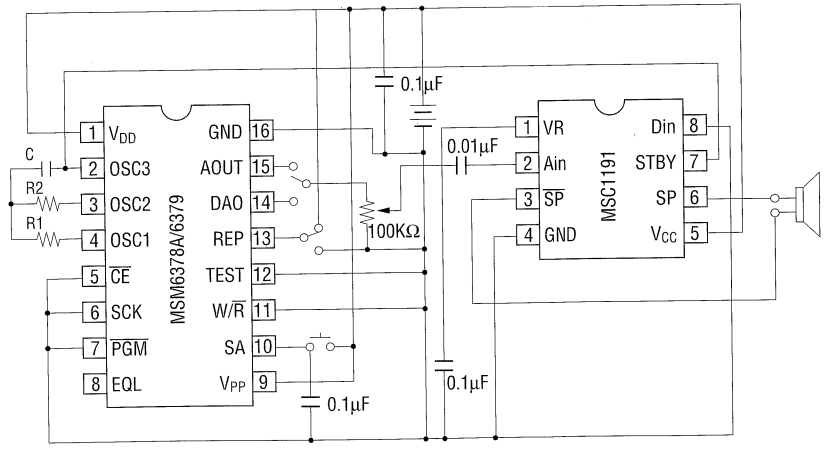
1. Playback

1.1 When Standard AMP is used



Note: The capacitor connected to the SA pin contributes to noise margin in the case of SA being "open".

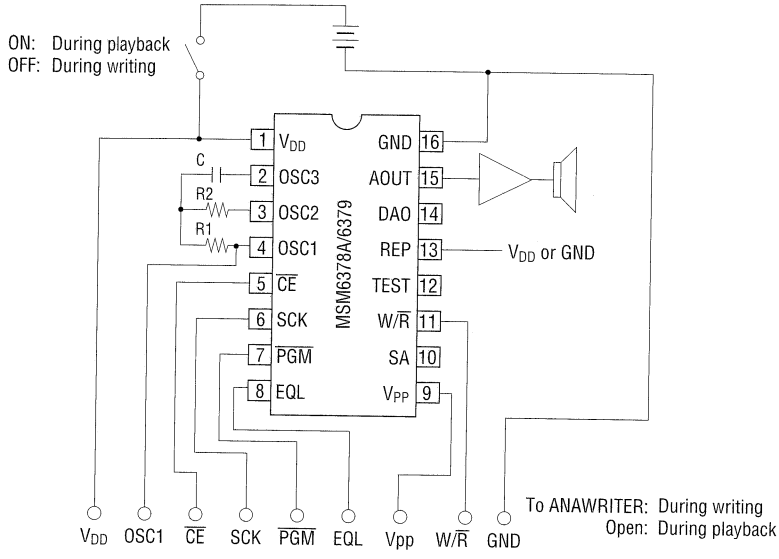
1.2 Use of MSC1191 as AMP



Note: The MSC1191 is the most suitable amplifier to drive a speaker for voice ICs. When the MSM6378A terminates the playback of voice data, the MSC1191 is also put into power save mode automatically.

2. Example of Write Circuit

(Equivalent to the playback circuit)



ANAWRITER interface pins

Note: Be careful about noise margin for input pins that are open during playback.

MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx, MSM6650

Internal Mask ROM Voice Synthesis IC, Internal 1-Mbit One-Time-Programmable (OTP) ROM Voice Synthesis IC, External ROM Drive Voice Synthesis IC

GENERAL DESCRIPTION

The MSM6650 family is the successor to OKI's MSM6375 family. To ensure high-quality voice synthesis, the MSM6650 family members offer adaptive differential pulse-code modulation (ADPCM) playback, pulse-code modulation (PCM) playback, 12-bit D/A conversion, and on-chip –40 dB/octave low-pass filter (LPF).

The conventional "beep" tones and 2-channel playback are now easier to use. OKI has added additional functions such as melody play, fade-out, and random playback. OKI has improved external control by adding an Edit ROM. The Edit ROM can be used to form sentences by linking phrases.

The MSM6650 family members can support a variety of applications as it can function in either Standalone Mode or Microcontroller Interface Mode. In Microcontroller Interface Mode, serial input control is available. Serial input control minimizes the number of microcontroller port pins required for voice synthesis control. The MSM6650 family includes an internal mask ROM version, internal one-time-programmable (OTP) ROM version, and external ROM version. The features of the MSM6650 family devices are as follows.

- MSM6652/53/54/55/56-xxx
  These devices are single-chip voice synthesizers with an on-chip mask ROM using the CMOS technology.
  Standalone Mode or Microcontroller Interface Mode can be selected by mask option.
- MSM6652A/53A/54A/55A/56A/58A-xxx
  The trial production period for these devices is shorter than those described above. These devices are suitable for developing prototype models and concept demonstration of new products.
- MSM66P54-xx
  The device is a single-chip CMOS voice synthesizer with one-time-programmable (OTP) ROM. Standalone and Microcontroller Interface Modes are selected by using a code (01-04).
  The user can easily write voice data using the development tool AR761 or AR762, or P54 adapter. Unlike the mask ROM version, the OTP version is suited to applications which requires a small lot production of different type devices or short delivery time.
- MSM6650
  The MSM6650 device can directly connect external ROM or EPROM of up to 64 Mbits, which stores voice data.
  This device is ideally suited to an evaluation IC for the MSM6650 family because its circuit configuration is identical to those of the mask ROM-based and OTP version devices.

• Option Table

	Pin Name	Microcontroller Interface Mode		Standalone Mode	
		Serial Input	Parallel Input	With Standby	No Standby
MSM6652/53/54/55/56 MSM6652A/53A/54A/55A/56A/58A	—	Mask Option			
MSM66P54	—	–01	–02	–03	–04
MSM6650	CPU	"H"	"H"	"L"	"L"
	SERIAL	"H"	"L"	"L"	"L"
	$\overline{\text{STBY}}$	"H"	"H"	"L"	"H"

Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

The table below shows the major differences between the MSM6650 family and the MSM6375 family.

	MSM6650 Family	MSM6375 Family
Interface	Standalone mode/Microcontroller interface mode	SW input/CPU input interface
Voice synthesis method	4-bit ADPCM or 8-bit PCM/Melody PCM	4-bit ADPCM
"Beep" tone frequecy (length)	0.5, 1.0, 1.3, 2.0 kHz Options (16 ms to 2100 ms)	1.0 or 2.0 kHz, (User-specified length, fixed at either 64, 128, 250, or 500 ms)
Sampling frequency (f_S)	Eight frequencies (4.0, 5.3, 6.4, 8.0, 10.6, 12.8, 16.0, or 32.0 kHz)	Three frequencies at two oscillator frequencies (4.0, 6.4, 8.0 kHz with f_{OSC}=64 kHz; 16.0, 25.6, 32.0 kHz with f_{OSC}=256 kHz)
Master clock frequency (f_{OSC})	256 kHz (RC)/4.096 MHz (ceramic/crystal)	40 kHz to 256 kHz
LPF attenuation factor	–40 dB/octave	–24 dB/octave
LPF cut-off frequency (f_{CUT}), kHz	f_{CUT}: 1.8 | 2.6 | 2.6 | 3.2 | 4.2 | 5.1 | 6.4 | 12.8 f_S: 4.0 | 5.3 | 6.4 | 8.0 | 10.6 | 12.8 | 16.0 | 32.0	f_{CUT}: 1.5 | 3.0 | 3.0 f_S: 4.0 | 6.4 | 8.0
Maximum phrase number	127	111
Pull-up/pull-down resistors	Built in	—
Standby conversion time	0.2 sec	3 sec
Mask options	4 options	14 options
Added function in edit ROM	Edit ROM Fade-out Random playback Melody playback PCM playback Serial input/port output	—

STANDALONE MODE

FEATURES

Device name	ROM size	Maximum playback time (sec)			
		f_S=4.0 kHz	f_S=6.4 kHz	f_S=8.0 kHz	f_{SAM}=16 kHz
MSM6652, 6652A	288 Kbits	16.9	10.5	8.4	4.2
MSM6653, 6653A	544 Kbits	31.2	19.5	15.6	7.8
MSM6654, 6654A	1 Mbit	63.8	39.9	31.9	15.9
MSM6655, 6655A	1.5 Mbits	96.5	60.3	48.2	24.1
MSM6656, 6656A	2 Mbits	129.1	80.7	64.5	32.2
MSM6658A	4 Mbits	259.7	162.9	129.8	64.9
MSM66P54	1 Mbit	63.8	39.9	31.9	15.9
MSM6650	64 Mbits (Max)	4194.3	2620.5	2096.4	1048.2

Note: Actual voice ROM area is smaller by 22 Kbits.

- 4-bit ADPCM or 8-bit PCM sound generation
- Melody function
- Edit ROM function
- Two-channel mixing function
- Built-in random playback function
- Fade-out function via four-step sound volume attenuation
- Built-in beep tone of 0.5 kHz, 1.0 kHz, 1.3 kHz, or 2.0 kHz selectable with a specific code
- Sampling frequency of 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, or 32.0 kHz (32 kHz sampling is not possible when using RC oscillation)
- Up to 120 phrases
- Built-in 12-bit D/A converter
- Built-in –40 dB/octave low-pass filter
- Standby function
- Selectable RC or ceramic oscillation
- Package options:

18-pin plastic DIP (DIP18-P-300) (Product name: MSM6652-xxxRS/MSM6653-xxxRS/ MSM6654-xxxRS/MSM6655-xxxRS/ MSM6656-xxxRS/MSM6652A-xxxRS/ MSM6653A-xxxRS/MSM6654-xxxRS/ MSM6655A-xxxRS/MSM6656-xxxRS/)

24-pin plastic DIP (SOP24-P-430-K) (Product name: MSM6652-xxxGS-K/MSM6653-xxxGS-K MSM6654-xxxGS-K/MSM6655-xxxGS-K/ MSM6656-xxxGS-K/MSM6652A-xxxGS-K/ MSM6653A-xxxGS-K/MSM6654A-xxxGS-K/ MSM6655A-xxxGS-K/MSM6656A-xxxGS-K/ MSM6658A-xxxGS-K/MSM66P54-03GS-K MSM66P54-04GS-K)

20-pin plastic DIP (DIP20-P-300-W1) (Product name: MSM66P54-03RS/MSM66P54-04RS)

64-pin plastic QFP (QFP64-P-1420-BK) (Product name: MSM6650GS-BK)

64-pin plastic SDIP (SDIP64-P-750) (Product name: MSM6650SS)

• Option Table

	Pin Name	Microcontroller Interface Mode		Standalone Mode		
		Serial Input	Parallel Input	With Standby	No Standby	
MSM6652/53/54/55/56 MSM6652A/53A/54A/55A/56A/58A	—	Mask Option (Note1)				
MSM66P54	—	–01	–02	–03	–04	(Note2)
MSM6650	CPU	"H"	"H"	"L"	"L"	
	SERIAL	"H"	"L"	"L"	"L"	
	$\overline{\text{STBY}}$	"H"	"H"	"L"	"H"	

Note: 1. The options for the mask ROM-based devices are mask options. The user should send OKI an option list before starting development.
A sample of option list is shown below.
2. A code of OTP version device corresponds to one of the options. The user should specify either MSM66P54-03 or MSM66P54-04. (In this case, no option list is required.)

Oki Electric Industry Co., Ltd.

Date:

Option List

You are requested to develop MSM665X-XXX on the following conditions.

1. Options
There are four options for the MSM6650 family.
Choose and circle the desired option.

Option	Interface mode	Input	Standby conversion
Option A	Microcontroller	Serial	—
Option B	Microcontroller	Parallel	—
Option C	Standalone	—	Yes
Option D	Standalone	—	No

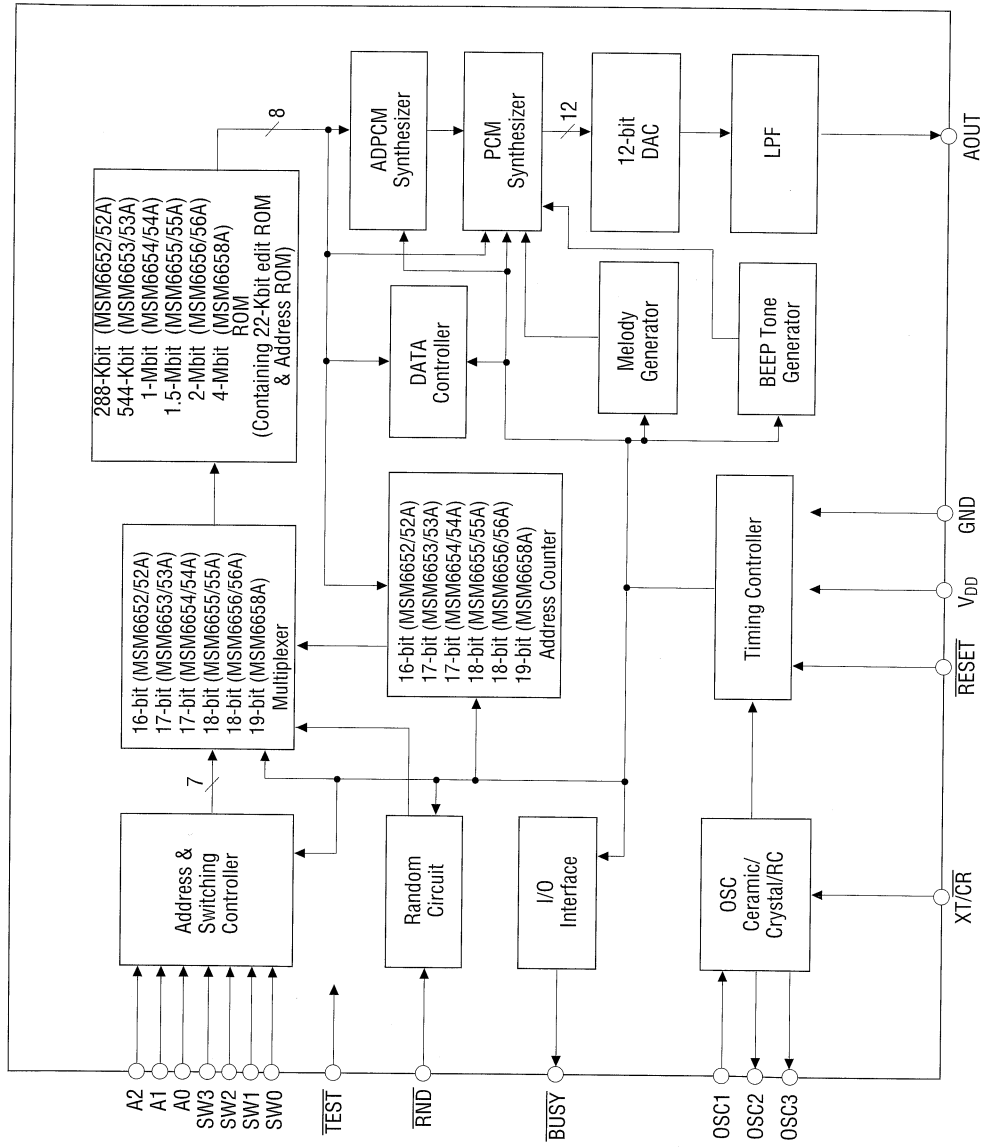
2. Package and quantity

Item	Package (circle the desired one)			Quantity	Note
Ceramic sample	18-pin DIP (ceramic)	24-pin SOP (ceramic)	chip	____pcs	Up to 10 samples. Operating temp. : 10 to 30°C
Mold sample	18-pin DIP (plastic)	24-pin SOP (plastic)	chip	____pcs	Up to 50 samples
Mass production	18-pin DIP (plastic)	24-pin SOP (plastic)	chip	____pcs per lot ____monthly	

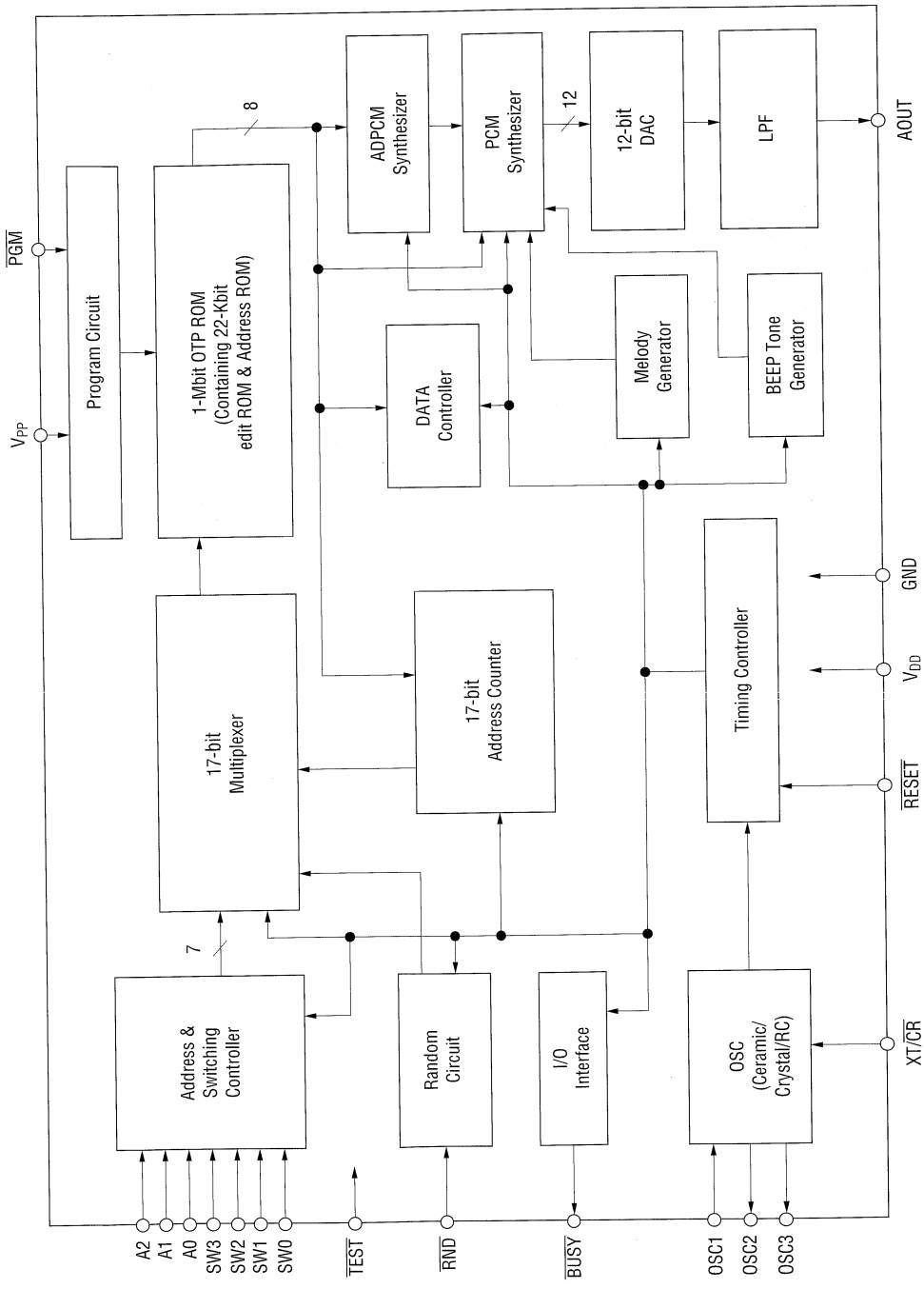
Signed by _____
Title :
Company name :

BLOCK DIAGRAMS

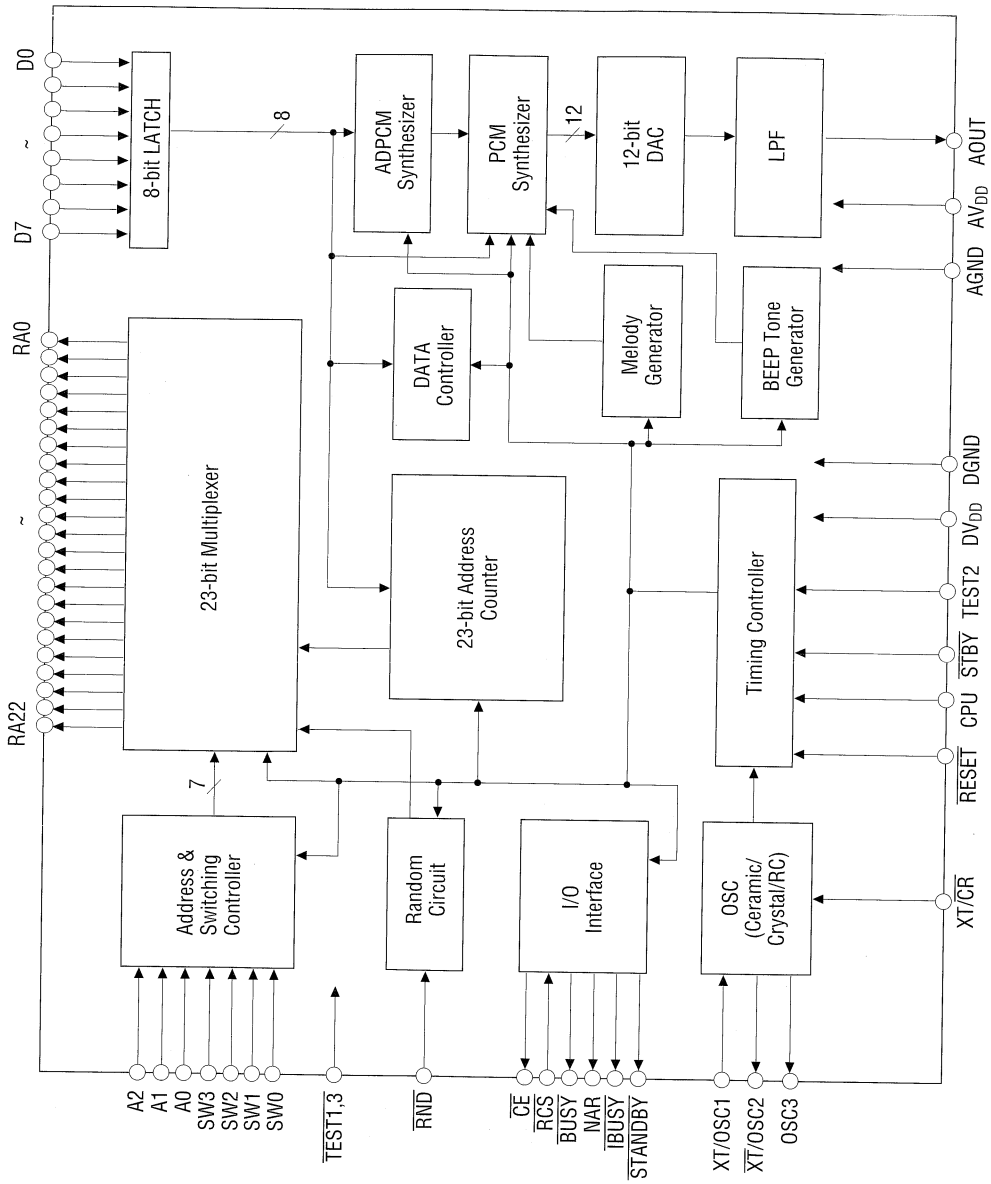
MSM6652/53/54/55/56-xxx
MSM6652A/53A/54A/55A/56A/58A-xxx



MSM66P54-xx


PGM
VPP
Program Circuit
1-Mbit OTP ROM
(Containing 22-Kbit
edit ROM & Address ROM)
8
ADPCM
Synthesizer
PCM
Synthesizer
12
12-bit
DAC
LPF
AOUT
DATA
Controller
Melody
Generator
BEEP Tone
Generator
17-bit
Multiplexer
17-bit
Address Counter
Timing Controller
GND
VDD
RESET
XT/CR
7
Address &
Switching
Controller
Random
Circuit
I/O
Interface
OSC
(Ceramic/
Crystal/RC)
A2
A1
A0
SW3
SW2
SW1
SW0
TEST
RND
BUSY
OSC1
OSC2
OSC3

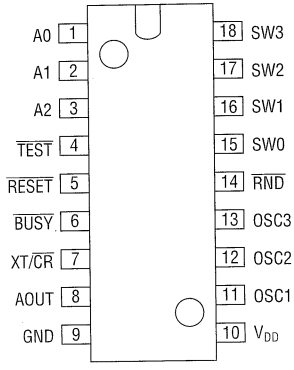
MSM6650


D0
~
D7
8-bit LATCH
8
ADPCM Synthesizer
PCM Synthesizer
12
12-bit DAC
LPF
AOUT
AVDD
AGND
RA0
~
RA22
23-bit Multiplexer
DATA Controller
Melody Generator
BEEP Tone Generator
23-bit Address Counter
Timing Controller
DGND
DVDD
TEST2
STBY
CPU
RESET
7
Address & Switching Controller
Random Circuit
I/O Interface
OSC (Ceramic/ Crystal/RC)
XT/CR
A2
A1
A0
SW3
SW2
SW1
SW0
TEST1,3
RND
CE
RCS
BUSY
NAR
IBUSY
STANDBY
XT/OSC1
XT/OSC2
OSC3

PIN CONFIGURATION (TOP VIEW)

The MSM66P54-xx has two more pins than the MSM6652-6658A while their pin configurations are identical.
The additional two pins (V_{PP}, $\overline{PGM}$) of the MSM66P54-xxX may be open at playback after completion of writing.

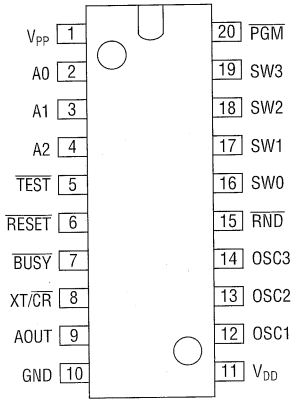
MSM6652-6656 (Mask ROM)



18-Pin Plastic DIP

MSM6652-xxxRS, MSM6653-xxxRS, MSM6654-xxxRS,
MSM6655-xxxRS, MSM6656-xxxRS, MSM6652A-xxxRS,
MSM6653A-xxxRS, MSM6654A-xxxRS,
MSM6655A-xxxRS, MSM6656A-xxxRS

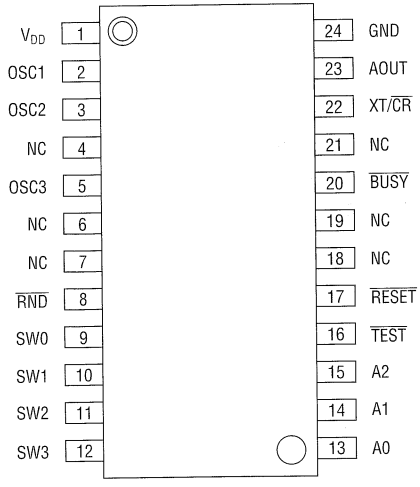
MSM66P54 (OTP)



20-Pin Plastic DIP

MSM66P54-03/-04RS

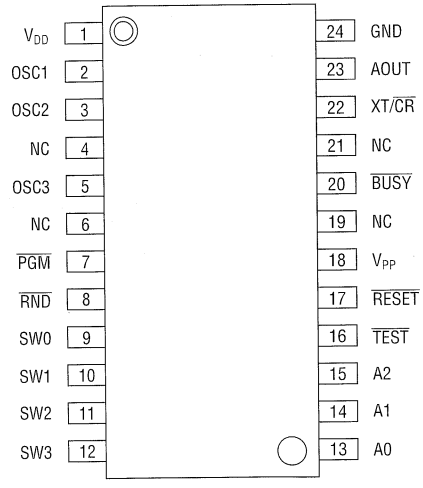
MSM6652-6658A (Mask ROM)



24-Pin Plastic SOP

MSM6652-xxxGS-K, MSM6653-xxxGS-K
MSM6654-xxxGS-K, MSM6655-xxxGS-K,
MSM6656-xxxGS-K, MSM6652A-xxxGS-K,
MSM6653A-xxxGS-K, MSM6654A-xxxGS-K,
MSM6655A-xxxGS-K, MSM6656A-xxxGS-K,
MSM6658A-xxxGS-K

MSM66P54 (OTP)

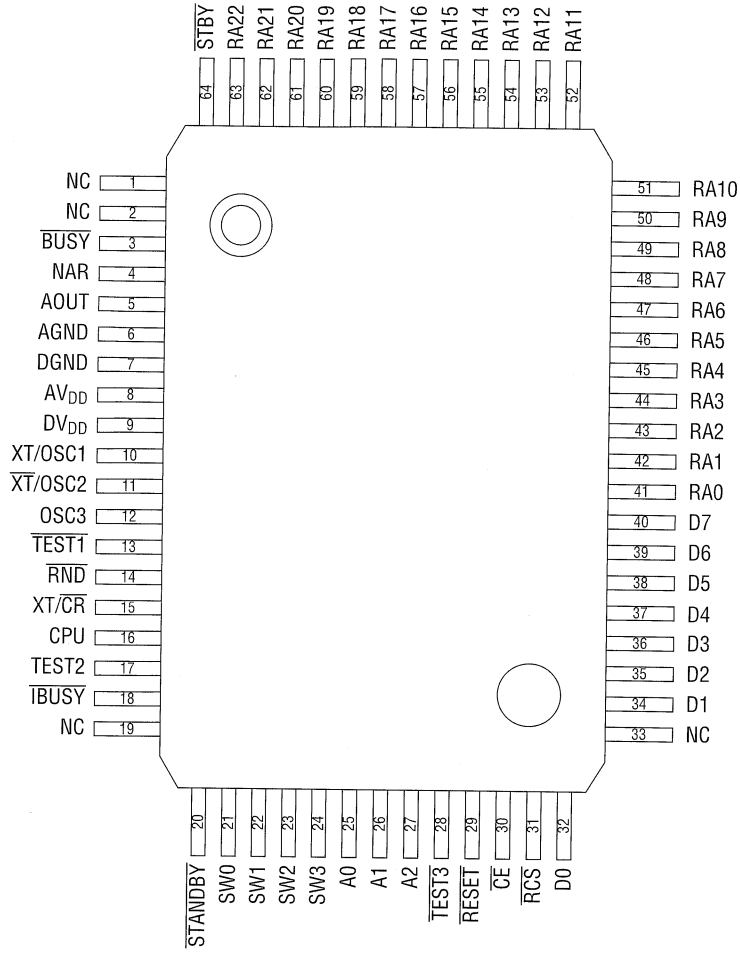


24-Pin Plastic SOP

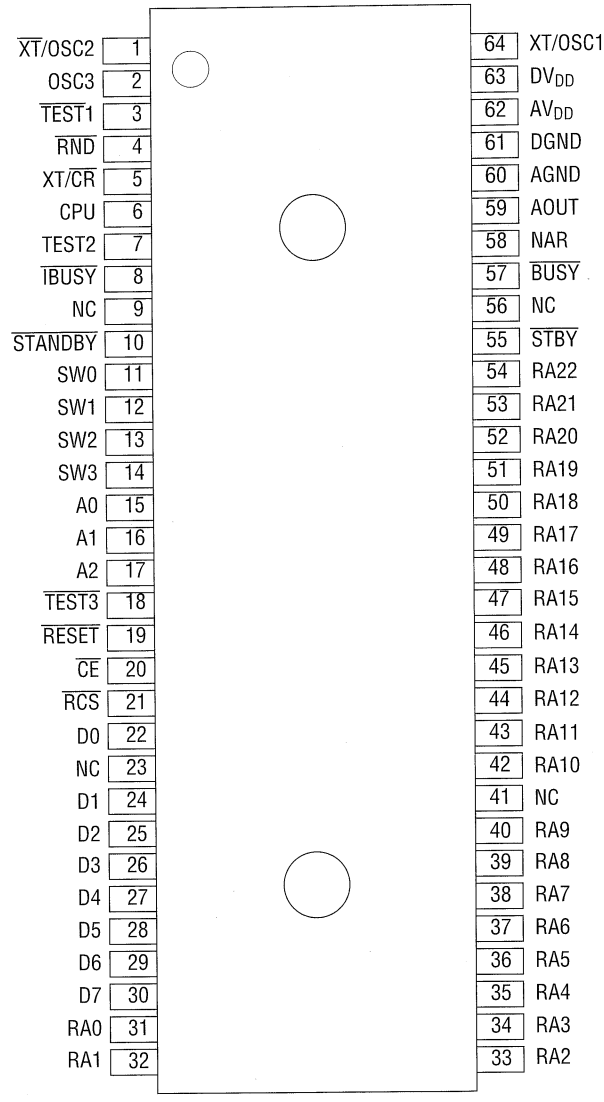
MSM66P54-03/-04GS-K

MSM6650

Product name: MSM6650GS-BK



64-Pin Plastic QFP



64-Pin Plastic S-DIP

PIN DESCRIPTIONS

Common pins for MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx, MSM6650

Symbol	Type	Description
$\overline{\text{RESET}}$	I	**Reset.** Setting this pin to "L" puts the deveice in standby status. At this time, oscillation stops, AOUT is pulled to GND, and the deveice is initialized. The MSM6650 family devices have an internal power-on reset. To operate the power-on reset correctly, power should ramp up within 1 ms. If this is not possible, apply a $\overline{\text{RESET}}$ pulse when power is turned on. This pin has an internal pull-up resistor.
$\overline{\text{BUSY}}$	O	**Busy.** This pin outputs a "L" level during playback. At power-on, this pin is at "H" level.
XT/$\overline{\text{CR}}$	I	**XT/$\overline{\text{CR}}$ selectable pin.** Set to "H" level when using ceramic oscillation. Set to "L" level when using RC oscillation.
AOUT	O	**Sound Output.** This is the synthesized output pin of the internal low-pass filter.
GND	—	**Ground.**
V_{DD}	—	**Power supply.** Insert a 0.1μF or more bypass capacitor between this pin and GND.
OSC1	I	**Oscillator 1.** This pin is a ceramic oscillator connection pin when using ceramic oscillation. This pin is an RC connection pin when using RC oscillation. When using an external clock, use this pin as the clock input.
OSC2	O	**Oscillator 2.** This pin is a ceramic oscillator connection pin when using a ceramic oscillator. This is an RC connection pin when using RC oscillation. Leave open if using an external clock. OSC2 outputs a "L" level in standby status.
OSC3	O	**Oscillator 3.** Leave open if using a ceramic oscillator. This pin is the RC connection pin when using RC oscillation. When RC oscillation is selected, OSC3 outputs a "H" level in standby status.
$\overline{\text{RND}}$	I	**Random Playback.** Random playback starts when the $\overline{\text{RND}}$ pin is set to a "L" level. At the fall of $\overline{\text{RND}}$, addresses from the random address playback circuit inside the IC are fetched. Set to a "H" level if random playback is not used. This pin has an internal pull-up resistor.
SW0-SW3	I	**Phrase Inputs.** These pins are phrase input pins corresponding to playback. If the input changes, SW0 to SW3 pins capture address data after 16 ms and speech playback commences. These pins have internal pull-down resistors.
A0-A2	I	**Phrase Inputs.** Phrase input pins correspoding to playback. The A0 input becomes invalid when the random playback function is used.

Common pins for MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx

Symbol	Type	Description
GND	—	**Ground.**
V_{DD}	—	**Power supply.** Insert a 0.1μF or more bypass capacitor between this pin and GND.
$\overline{\text{TEST}}$	I	**Test Mode.** Set to "H" level. This pin has an internal pull-up resistor.

Pins for MSM66P54-xx

Symbol	Type	Description
V_{pp}	—	Power supply used when writing data to internal OTP ROM. Leave open or set to "H" level during playback.
$\overline{PGM}$	I	Interface with voice analysis edit tool AR761 or AR762. Set to "L" level or leave open during playback.

Pins for MSM6650

Symbol	Type	Description
$\overline{CE}$	—	**Chip Enable.** $\overline{CE}$ is a timing output pin to control read of external memory. This pin outputs when $\overline{RCS}$ is at the "L" level. This pin goes high impedance when $\overline{RCS}$ is at the "H" level.
CPU	I	**CPU Mode.** Set to "L" level to select Standalone Mode. Set to "H" level to select Microcontroller Interface Mode.
D0-D7	I	**External Memory Data Bus.** Data is input when $\overline{RCS}$ is low. When $\overline{RCS}$ is high, these pins become low due to internal pull-down resistors.
$\overline{IBUSY}$	O	**I Busy.** Outputs a "L" level during voice playback (except during standby conversion time), or when the AOUT pin is at half V_{DD} level.
RA0-RA22	O	**External Memory Address.** These are address pins for an external memory output when $\overline{RCS}$ is low. These pins become high impedance status if $\overline{RCS}$ is in "H" level.
$\overline{RCS}$	I	**Read Chip Select.** The data bits D0-D7 are internally pulled down when $\overline{RCS}$ is high. Addresses and $\overline{CE}$ are output when $\overline{RCS}$ is at "L" level. The RA22-RA0 address pins and $\overline{CE}$ pin become high impedance.
$\overline{STBY}$	I	**Standby Contorl.** If set to "L" level, the MSM6650 enters standby mode 0.2 seconds after voice ends. If set to "H" level, the MSM6650 AOUT output maintains half V_{DD} after voice ends.
$\overline{STANDBY}$	O	**Standby Indicator.** This output pin remains at "L" level during oscillation.
$\overline{TEST\ 1,3}$	I	**Test.** Set these pins to "H" level. The $\overline{TEST1}$ and $\overline{TEST3}$ pins have internal pull-up resistor.
TEST2	I	**Test.** Set this pin to "L" level.
AGND	—	Analog ground pin.
DGND	—	Digital ground pin.
AV_{DD}	—	Analog power pin. Insert a 0.1 μF or more bypass capacitor in between this pin and AGND.
DV_{DD}	—	Digiral power pin. Insert a 0.1 μF or more bypass capacitor in between this pin and DGND.

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	MSM6652-56, MSM6650, MSM6652A-56A	+2.4 to +5.5			V
	V_{DD}	MSM6658A, MSM66P54	+3.5 to +5.5			V
Operating temperature	T_{op}	—	−40 to +85			°C
Master clock frequency 1	f_{OSC1}	When crystal selected	**Min.**	**Typ.**	**Max.**	MHz
			3.5	4.096	4.5	
Master clock frequency 2	f_{OSC2}	When RC selected (note)	200	256	300	kHz

Note: If RC oscillation is selected, 32kHz sampling frequency cannot be selected.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	4.2	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.8	V
"H" output voltage	V_{OH}	I_{OH}=–1 mA	4.6	—	—	V
"L" output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"H" input current 2	I_{IH2}	Internal pull-down resistance	30	90	200	µA
"L" input current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
"L" input current 2 (note)	I_{IL2}	Internal pull-up resistance	–200	–90	–30	µA
Operating power consumption	I_{DD}	—	—	6	10	mA
Standby power consumption	I_{DS}	—	—	—	10	µA
D/A output relative accuracy	$\|V_{DAE}\|$	When D/A output selected	—	—	40	mV
D/A output impedance	R_{DAO}	When D/A output selected	15	25	35	kΩ
LPF driving resistance	R_{AOUT}	—	50	—	—	kΩ
LPF output impedance	R_{LPF}	I_F=100 µA	—	1	3	kΩ

Note: Not applied to MSM66P54-xx.

DC Characteristics

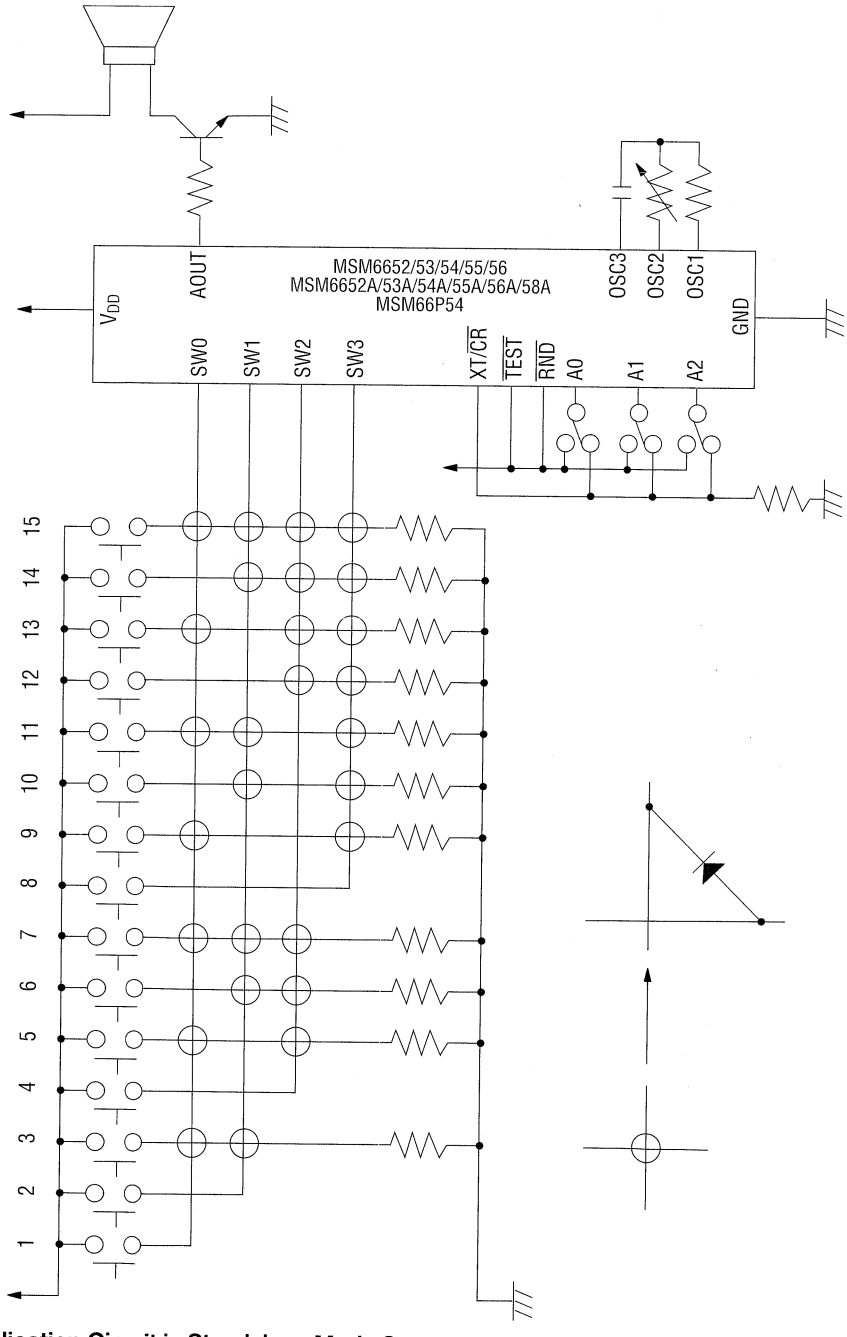
(V_{DD}=3.1 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	2.7	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.5	V
"H" output voltage	V_{OH}	I_{OH}=–1 mA	2.6	—	—	V
"L" output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"H" input current 2	I_{IH2}	Internal pull-down resistance	10	30	100	µA
"L" input current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
"L" input current 2 (note)	I_{IL2}	Internal pull-up resistance	–100	–30	–10	µA
Operating power consumiption	I_{DD}	—	—	4	7	mA
Standby power consumption	I_{DS}	—	—	—	1	µA
D/A output relative accuracy	$\|V_{DAE}\|$	When D/A output selected	—	—	20	mV
D/A output impedance	R_{DAO}	When D/A output selected	15	25	35	kΩ
LPF driving resistance	R_{AOUT}	—	50	—	—	kΩ
LPF output impedance	R_{LPF}	I_F=100 µA	—	1	3	kΩ

Note: Not applied to MSM66P54-xx.

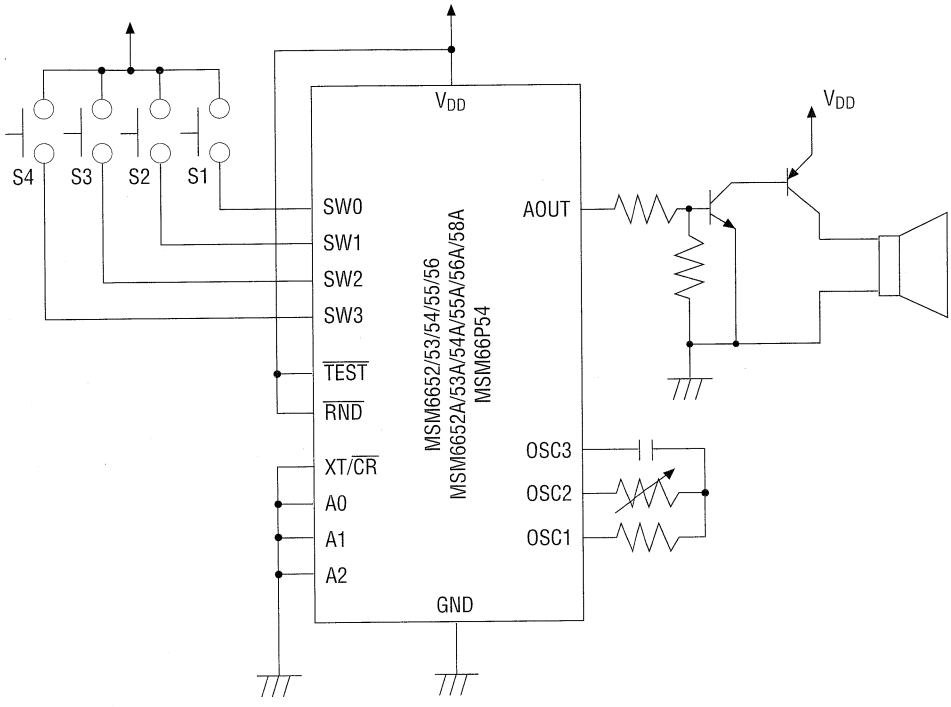
APPLICATION CIRCUITS

(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx)



Application Circuit in Standalone Mode Supporting 15 Switch-Selected Phrases

(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx)

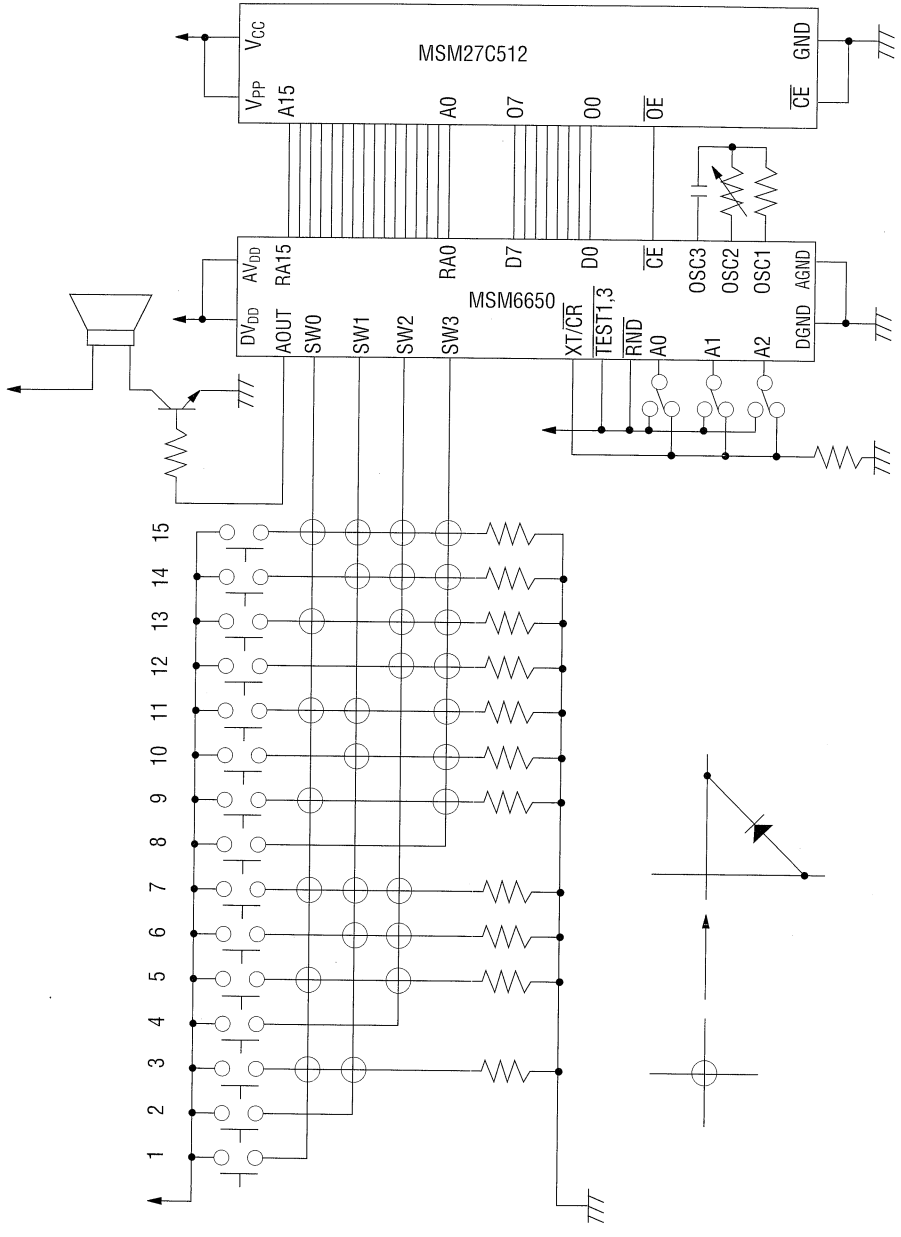


Application Circuit in Standalone Mode Supporting Four Switch-Selected Words

Switches and Playback Addresses

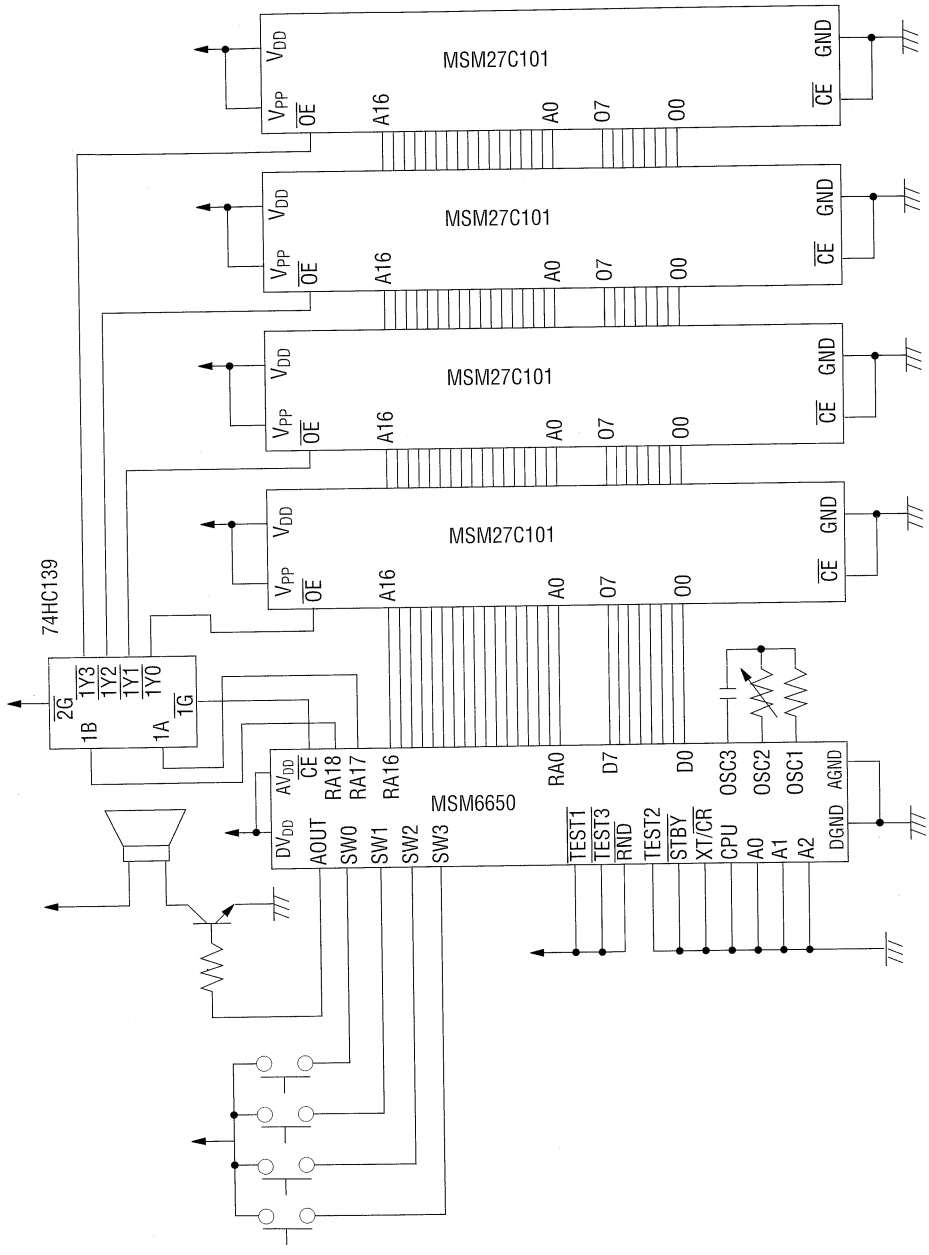
	A2	A1	A0	SW3	SW2	SW1	SW0	ADR
S1	0	0	0	0	0	0	1	01
S2	0	0	0	0	0	1	0	02
S3	0	0	0	0	1	0	0	04
S4	0	0	0	1	0	0	0	08

(MSM6650)



Application Circuit in Standalone Mode Supporting 15 Switch-Selected Phrases

(MSM6650)



Application Circuit in Standalone Mode Supporting Four 1-Mbit EPROMs

MICROCONTROLLER INTERFACE MODE

FEATURES

Device name	Data ROM size	Maximum playback time (sec)				
		f_S=4.0 kHz	f_S=6.4 kHz	f_S=8.0 kHz	f_S=16 kHz	f_S=32 kHz
MSM6652, 6652A	288 Kbits	16.9	10.5	8.4	4.2	2.1
MSM6653, 6653A	544 Kbits	31.2	19.5	15.6	7.8	3.9
MSM6654, 6654A	1 Mbit	63.8	39.9	31.9	15.9	7.9
MSM6655, 6655A	1.5 Mbits	96.5	60.3	48.2	24.1	12.0
MSM6656, 6656A	2 Mbits	129.1	80.7	64.5	32.2	16.1
MSM6658A	4 Mbits	259.7	162.9	129.8	64.9	32.4
MSM66P54	1 Mbit	63.8	39.9	31.9	15.9	7.9
MSM6650	64 Mbits (Max)	4194.3	2620.5	2096.4	1048.2	524.1

Note: Actual voice ROM area is smaller by 22 Kbits.

- 4-bit ADPCM or 8-bit PCM sound generation
- Melody function
- Edit ROM function
- Two-channel mixing function
- Fade-out function via four-step sound volume attenuation
- Serial input or parallel input selectable
- Built-in beep tone of 0.5 kHz, 1.0 kHz, 1.3 kHz, or 2.0 kHz selectable with a specific code
- Sampling frequency of 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, or 32.0 kHz (32 kHz sampling is not possible when using RC oscillation)
- Up to 127 phrases
- Built-in 12-bit D/A converter
- Built-in –40 dB/octave low-pass filter
- Standby function
- Package options:

18-pin plastic DIP (DIP18-P-300) (Product name: MSM6652-xxxRS/MSM6653-xxxRS/ MSM6654-xxxRS/MSM6655-xxxRS/ MSM6656-xxxRS/MSM6652A-xxxRS/ MSM6653A-xxxRS/MSM6654A-xxxRS/ MSM6655A-xxxRS/MSM6656A-xxxRS/)

24-pin plastic SOP (SOP24-P-430-K) (Product name: MSM6652-xxxGS-K/MSM6653-xxxGS-K/ MSM6654-xxxGS-K/MSM6655-xxxGS-K/ MSM6656-xxxGS-K/MSM6652A-xxxGS-K/ MSM6653A-xxxGS-K/MSM6654A-xxxGS-K/ MSM6655A-xxxGS-K/MSM6656A-xxxGS-K/ MSM6658A-xxxGS-K/MSM66P54-01GS-K MSM66P54-02GS-K)

20-pin plastic DIP (DIP20-P-300-W1) (Product name: MSM66P54-01RS/MSM66P54-02RS)

64-pin plastic QFP (QFP64-P-1420-BK) (Product name: MSM6650GS-BK)

64-pin plastic SDIP (SDIP64-P-750) (Product name: MSM6650SS)

• Option Table

	Pin Name	Microcontroller Interface Mode		Standalone Mode		
		Serial Input	Parallel Input	With Standby	No Standby	
MSM6652/53/54/55/56 MSM6652A/53A/54A/55A/56A/58A	—	Mask Option				(Note1)
MSM66P54	—	–01	–02	–03	–04	(Note2)
MSM6650	CPU	"H"	"H"	"L"	"L"	
	SERIAL	"H"	"L"	"L"	"L"	
	$\overline{\text{STBY}}$	"H"	"H"	"L"	"H"	

Note: 1. The options for the mask ROM-based devices are mask options. The user should send OKI an option list before starting development.
A sample of option list is shown below.
2. A code of OTP version device corresponds to one of the options. The user should specify either MSM66P54-01 or MSM66P54-02. (In this case, no option list is required.)

Oki Electric Industry Co., Ltd.

Date: _____

Option List

You are requested to develop MSM665X-XXX on the following conditions.

1. Options
There are four options for the MSM6650 family.
Choose and circle the desired option.

Option	Interface mode	Input	Standby conversion
Option A	Microcontroller	Serial	—
Option B	Microcontroller	Parallel	—
Option C	Standalone	—	Yes
Option D	Standalone	—	No

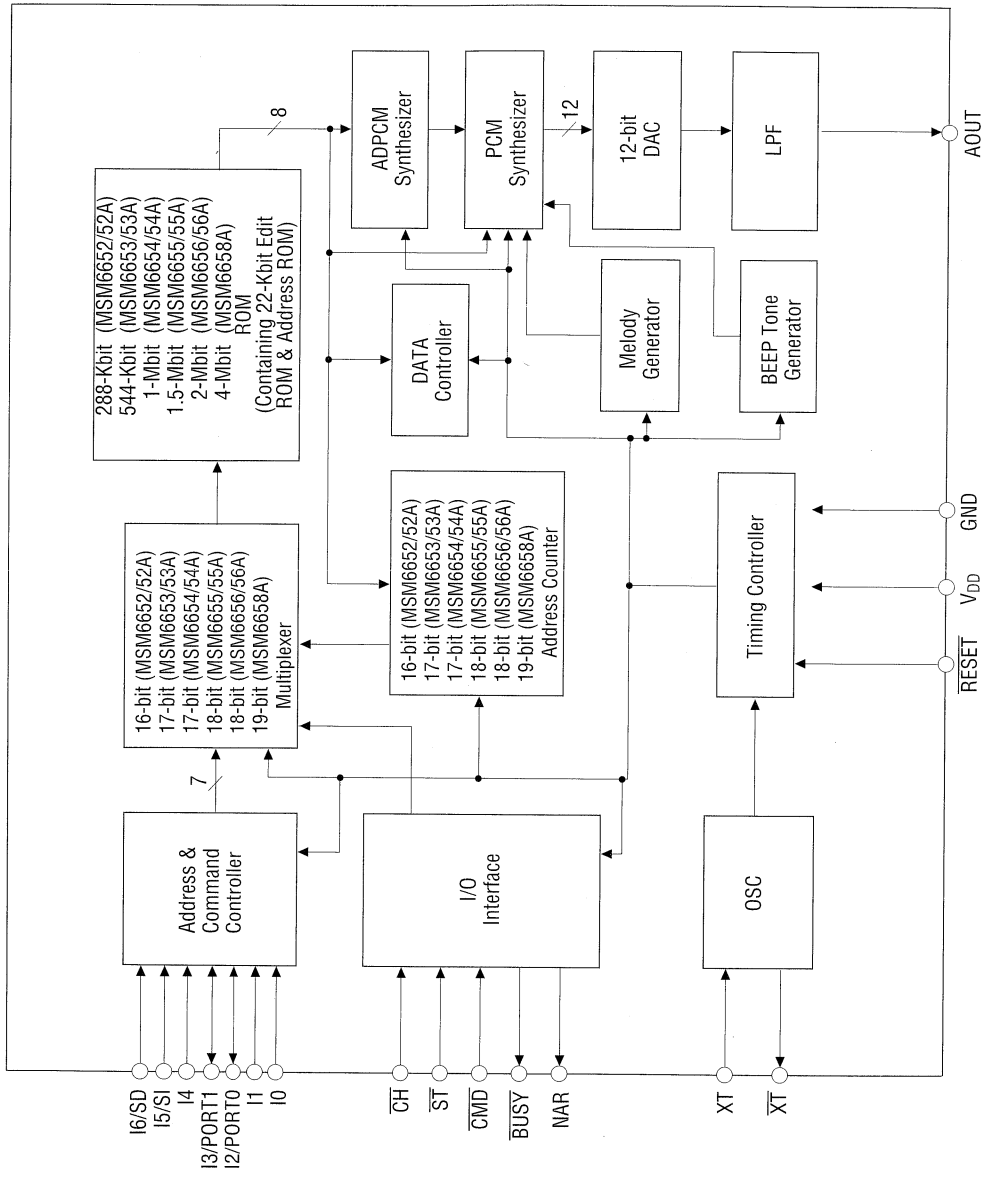
2. Package and quantity

Item	Package (circle the desired one)			Quantity	Note
Ceramic sample	18-pin DIP (ceramic)	24-pin SOP (ceramic)	chip	____pcs	Up to 10 samples. Operating temp. : 10 to 30°C
Mold sample	18-pin DIP (plastic)	24-pin SOP (plastic)	chip	____pcs	Up to 50 samples
Mass production	18-pin DIP (plastic)	24-pin SOP (plastic)	chip	____pcs per lot ____monthly	

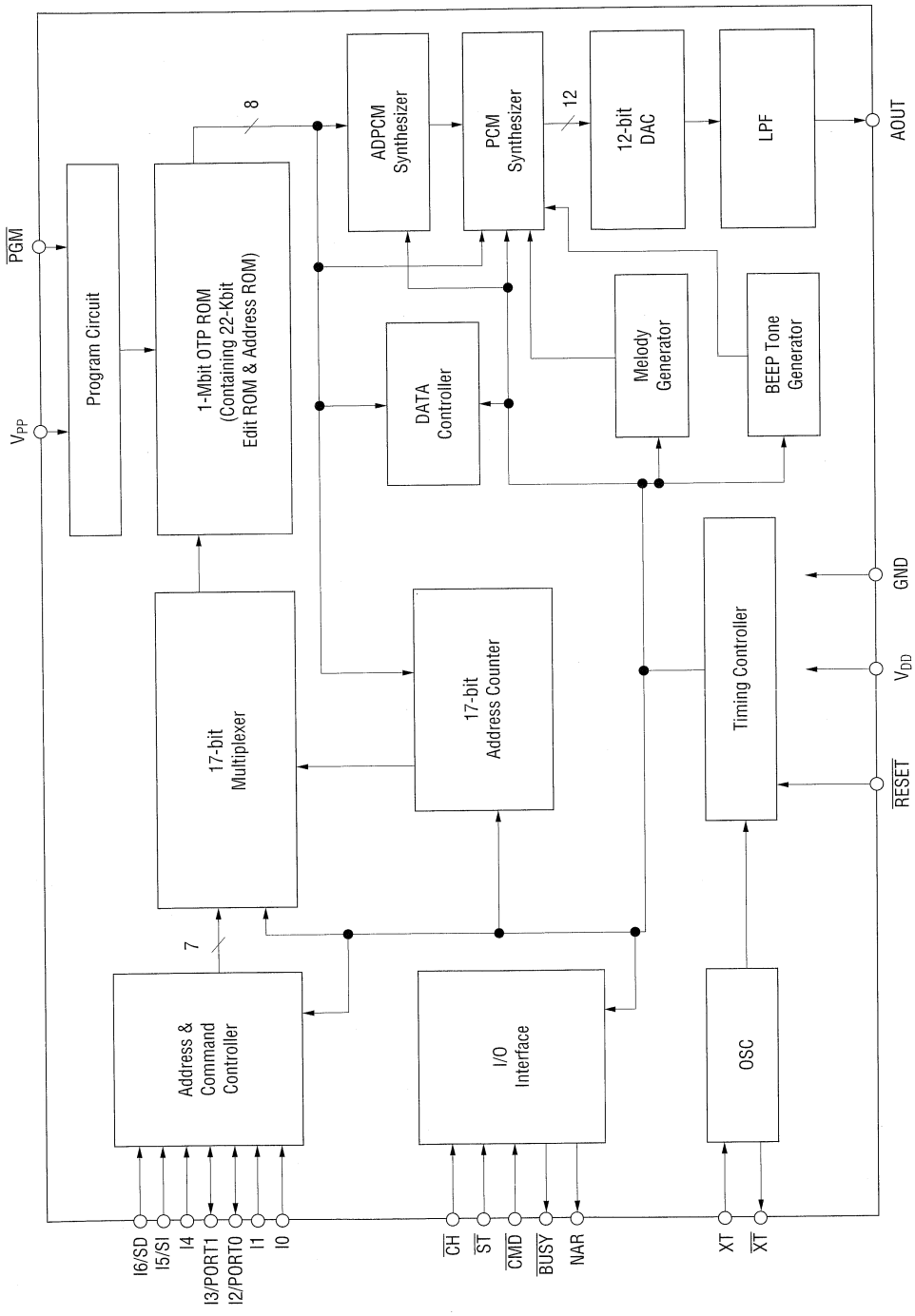
Signed by _____
Title :
Company name :

BLOCK DIAGRAMS

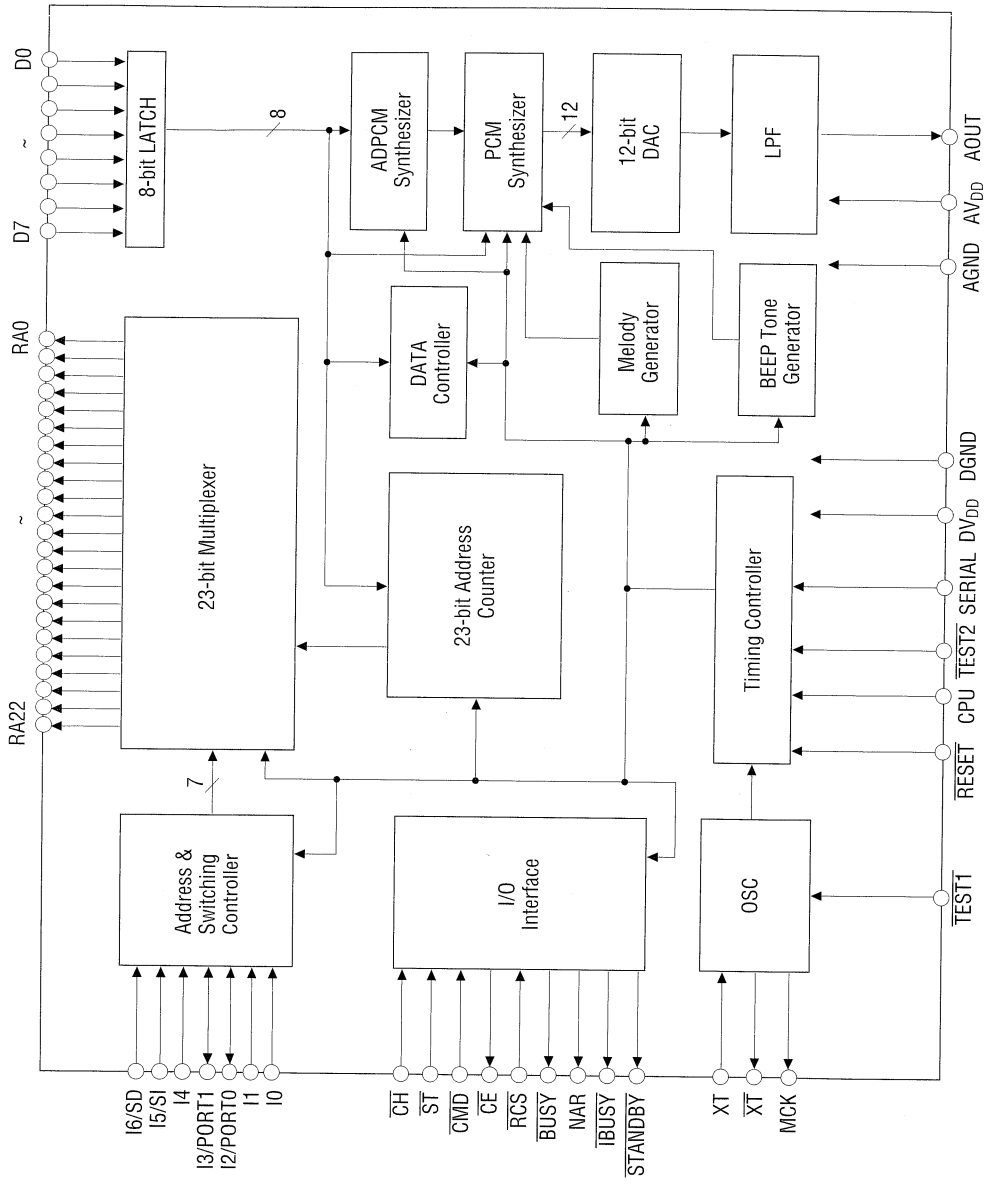
MSM6652/53/54/55/56-xxx
MSM6652A/53A/54A/55A/56A/58A-xxx



MSM66P54-xx


PGM
VPP
Program Circuit
1-Mbit OTP ROM
(Containing 22-Kbit
Edit ROM & Address ROM)
8
ADPCM
Synthesizer
PCM
Synthesizer
12
12-bit
DAC
LPF
AOUT
DATA
Controller
Melody
Generator
BEEP Tone
Generator
17-bit
Multiplexer
17-bit
Address Counter
Timing Controller
GND
VDD
RESET
7
Address &
Command
Controller
I/O
Interface
OSC
I6/SD
I5/SI
I4
I3/PORT1
I2/PORT0
I1
I0
CH
ST
CMD
BUSY
NAR
XT
XT

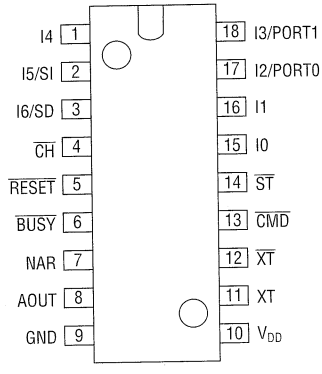
MSM6650


D0
~
D7
8-bit LATCH
8
ADPCM Synthesizer
PCM Synthesizer
12
12-bit DAC
LPF
AOUT
AVDD
AGND
RA0
~
RA22
23-bit Multiplexer
DATA Controller
Melody Generator
BEEP Tone Generator
23-bit Address Counter
Timing Controller
DGND
DVDD
SERIAL
TEST2
CPU
RESET
7
Address & Switching Controller
I/O Interface
OSC
TEST1
I6/SD
I5/SI
I4
I3/PORT1
I2/PORT0
I1
I0
CH
ST
CMD
CE
RCS
BUSY
NAR
IBUSY
STANDBY
XT
XT
MCK

PIN CONFIGURATION (TOP VIEW)

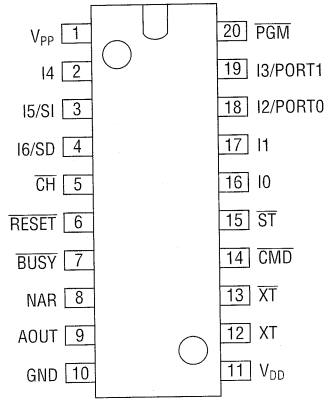
The MSM66P54-xx has two more pins than the MSM6652-6658A while their pin configurations are identical.
The additional two pins (V_{PP}, $\overline{PGM}$) of the MSM66P54-xx may be open at playback after completion of writing.

MSM6652-6656 (Mask ROM)



18-Pin Plastic DIP

MSM66P54 (OTP)

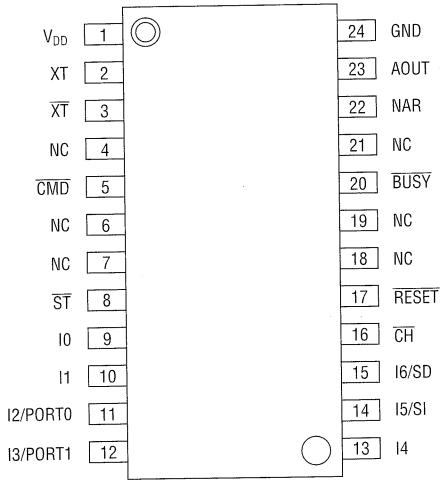


20-Pin Plastic DIP

MSM6652-xxxRS, MSM6653-xxxRS, MSM6654-xxxRS, MSM6655-xxxRS, MSM6656-xxxRS, MSM6652A-xxxRS, MSM6653A-xxxRS, MSM6654A-xxxRS, MSM6655A-xxxRS, MSM6656A-xxxRS

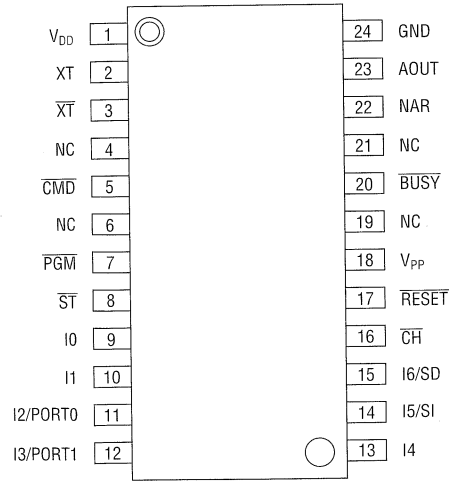
MSM66P54-01/-02RS

MSM6652-6658A (Mask ROM)



24-Pin Plastic SOP

MSM66P54 (OTP)



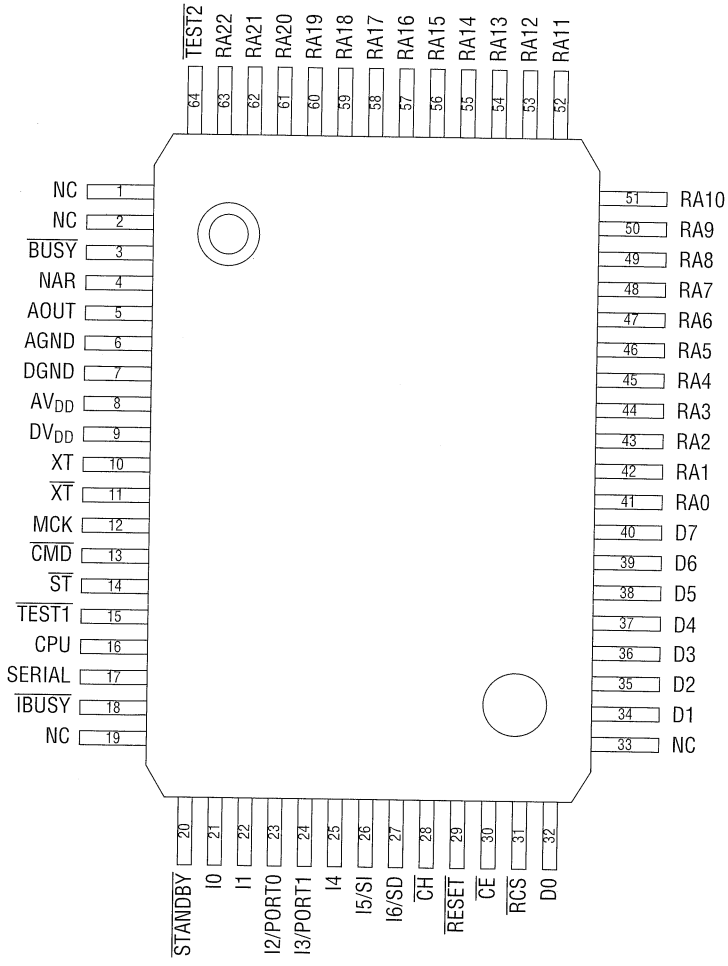
24-Pin Plastic SOP

MSM6652-xxxGS-K, MSM6653-xxxGS-K, MSM6654-xxxGS-K, MSM6655-xxxGS-K, MSM6656-xxxGS-K, MSM6652A-xxxGS-K, MSM6653A-xxxGS-K, MSM6654A-xxxGS-K, MSM6655A-xxxGS-K, MSM6656A-xxxGS-K, MSM6658A-xxxGS-K

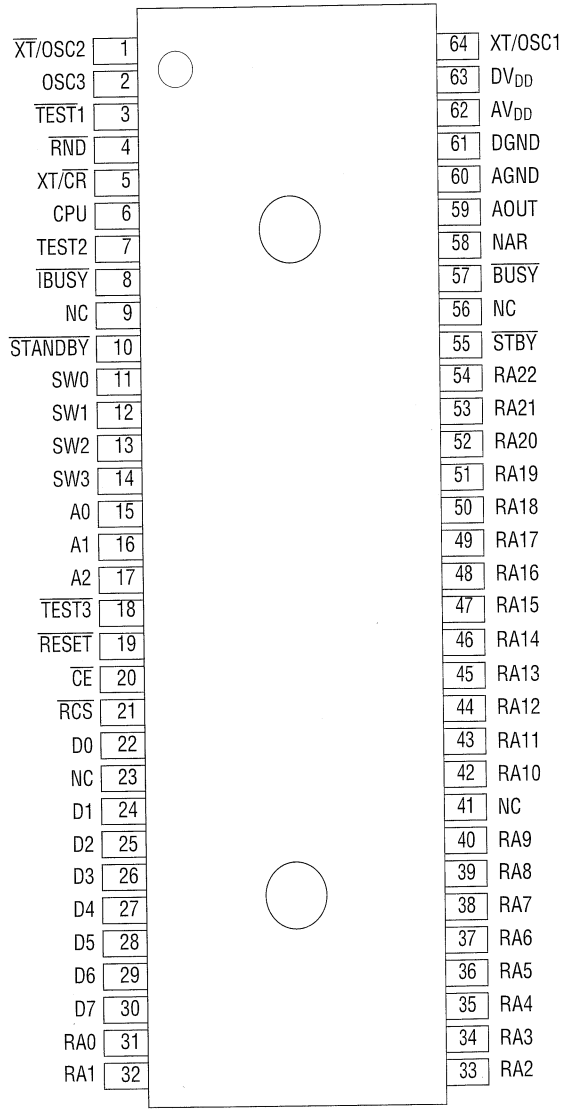
MSM66P54-01/-02GS-K

MSM6650

Product name: MSM6650GS-BK



64-Pin Plastic QFP



64-Pin Plastic S-DIP

PIN DESCRIPTIONS

Common pins for MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx, MSM6650

Symbol	Type	Description
$\overline{\text{RESET}}$	I	**Reset.** The devices enter stanby status when a low level is input to this pin. When RESET, oscillation stops. The AOUT output goes to ground and the IC status is reinitialized. The devices have an internal power-on reset. V_{DD} must be raised within 1 ms to operate power-on reset correctly. If V_{DD} is not raised within 1 ms, then the $\overline{\text{RESET}}$ pulse must be applied when power is turned ON. This pin has an internal pull-up resistor.
$\overline{\text{BUSY}}$	O	**Busy.** Outputs a "L" level during playback and a "H" level when power is turned ON.
NAR	O	The CMD and ST inputs become effective when high. NAR indicates whether the address bus (I0 through I6) is ready to accept another address. When high, it is ready to accept. NAR goes high when power is turned ON.
AOUT	O	**Analog Speech Output.** D/A converter output or LPF output is selected by entering the command.
XT	I	**Ceramic Oscillator Input.** This pin has an internal 0.5 to 5 MΩ feedback resistor between XT and $\overline{\text{XT}}$. If an external clock is used, this is the clock input pin.
$\overline{\text{XT}}$	O	**Ceramic Oscillator Output.** If an external clock is used, leave this pin open.
$\overline{\text{CMD}}$	I	**Command Input and Option Control.** This pin is used as command and option input when CMD is at the high level with $\overline{\text{ST}}$ low. If this pin is not used or serial input is optioned, set this pin to "H" level. This pin has an internal pull-up resistor.
$\overline{\text{ST}}$	I	**Start.** Speech playback starts at the fall of the $\overline{\text{ST}}$ pulse. The I0 - I6 addresses are latched at the rise of the $\overline{\text{ST}}$ pulse. Input a $\overline{\text{ST}}$ pulse when NAR goes to the high level for channels 1 and 2. This pin has an internal pull-up resistor.
$\overline{\text{CH}}$	I	**Channel Control.** Channel 1 is selected when the input is pulled high. Channel 2 is selected when the input is low. This pin has an internal pull-up resistor.
I6/SD	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is serial data (command and address) input when serial input is optioned.
I5/SI	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is used as serial clock input when serial input is optioned.
I4	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
I3/PORT1	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
I2/PORT0	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
I1, I0	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.

Common pins for MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx

Symbol	Type	Description
GND	—	**Ground pin.**
V_{DD}	—	**Power supply.** Insert a 0.1 µF or more bypass capacitor between this pin and GND.

Pins for MSM66P54-xx

Symbol	Type	Description
V_{pp}	—	Supply voltage for writing data to internal OTP ROM.
$\overline{PGM}$	I	Interface with voice analysis edit tools AR761 and AR762. Set to "L" level or leave open during playback. This pin has an internal pull-down resistor.

Pins for MSM6650

Symbol	Type	Description
AGND	—	**Analog ground pin.**
DGND	—	**Digital ground pin.**
AV_{DD}	—	**Analog power pin.** Insert a 0.1µF or more bypass capacitor between this pin and AGND.
DV_{DD}	—	**Digital power pin.** Insert a 0.1µF or more bypass capacitor between this pin and DGND.
MCK	O	**Main clock output pin.** Use MCK as a connection pin for the MSC1192, etc. When the IC is in standby status, MCK is held high.
CPU	I	**CPU Mode.** Set to "H" level to select Microcontroller Interface Mode.
SERIAL	I	**Serial/Parallel Interface Select.** This input selects either the parallel or the serial input interface. The serial input interface is selected with a high level; the parallel input interface is selected with a low level.
$\overline{CE}$	O	**Chip Enable.** $\overline{CE}$ is a timing output pin to control read of external memory. This pin outputs when $\overline{RCS}$ is at the "L" level. This pin goes high impedance when $\overline{RCS}$ is at the "H" level.
$\overline{RCS}$	I	**Read Chip Select.** The data bits D0-D7 are internally pulled down when $\overline{RCS}$ is high.
D7 - D0	I	**External Memory Data Bus.** Data is input when RCS is low. When RCS is high, these pins become low due to internal pull-down resistors.
RA22 - RA0	O	**External Memory Address.** These are address pins for an external memory output when $\overline{RCS}$ is low. These pins become high impedance status if $\overline{RCS}$ is in "H" level.
$\overline{TEST1, 2}$	I	**Test.** Set these pins to "H" level.
$\overline{IBUSY}$	O	Outputs a "L" level during playback or when AOUT is at 1/2 V_{DD} (except standby conversion)
$\overline{STANDBY}$	O	Outputs a "L" level during which the device is oscillating.

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	MSM6652-56, MSM6650, MSM6652A-56A	+2.4 to +5.5			V
		MSM6658A, MSM66P54	+3.5 to +5.5			V
Operating temperature	T_{op}	—	−40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	—	4.2	—	—	V
Low level input voltage	V_{IL}	—	—	—	0.8	V
High level output voltage	V_{OH}	I_{OH}=–1 mA	4.6	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
High level input current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High level input current 2	I_{IH2}	Internal pull-down resistor	30	90	200	µA
Low level input current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low level input current 2 (Note1)	I_{IL2}	Internal pull-up resistor	–200	–90	–30	µA
Operating current	I_{DD}	—	—	6	10	mA
Standby current	I_{DS}	—	—	—	10	µA
D/A output relative accuracy	$\|V_{DAE}\|$	When D/A output selected	—	—	40	mV
D/A output impedance	R_{DAO}	When D/A output selected (Note2)	15	25	35	kΩ
		When D/A output selected (Note3)	15	30	45	kΩ
LPF driving resisance	R_{AOUT}	When LPF output selected	50	—	—	kΩ
LPF output impedance	R_{LPF}	I_F=100 µA	—	1	3	kΩ

Note 1. Applied to $\overline{\text{RESET}}$, $\overline{\text{CMD}}$, $\overline{\text{ST}}$, $\overline{\text{CH}}$.
2. Applied to MSM6652/53/54/55/56, MSM6652A/53A/54A/55A/56A/58A, MSM6650.
3. Applied to MSM66P54.

DC Characteristics

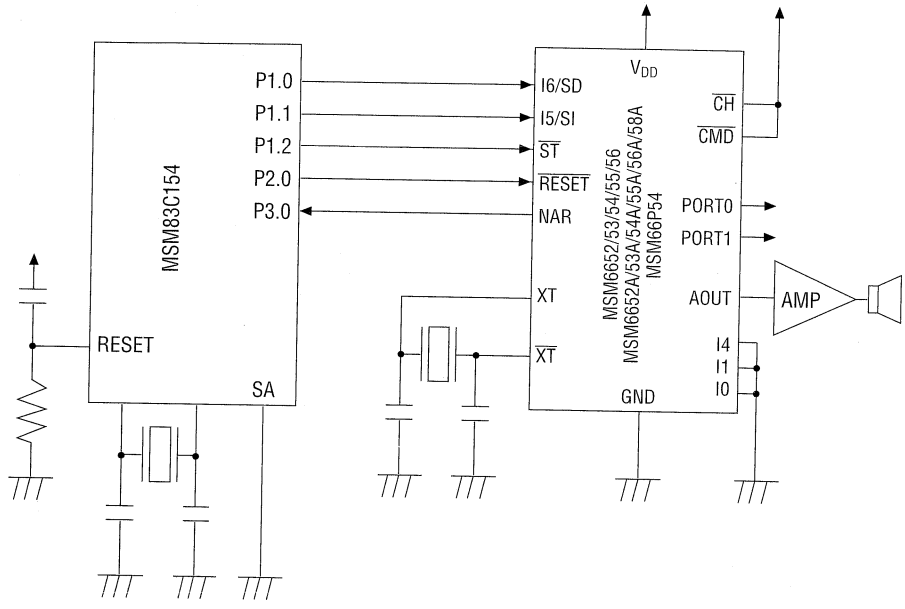
(V_{DD}=3.1 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	—	2.7	—	—	V
Low level input voltage	V_{IL}	—	—	—	0.5	V
High level output voltage	V_{OH}	I_{OH}=–1 mA	2.6	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
High level input current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High level input current 2	I_{IH2}	Internal pull-down resistor	10	30	100	µA
Low level input current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low level input current 2 (Note)	I_{IL2}	Internal pull-up resistor	–100	–30	–10	µA
Operating current	I_{DD}	—	—	4	7	mA
Standby current	I_{DS}	—	—	—	1	µA
D/A output relative accuracy	$\|V_{DAE}\|$	When D/A output selected	—	—	20	mV
D/A output impedance	R_{DAO}	When D/A output selected	15	25	35	kΩ
LPF driving resistance	R_{AOUT}	When LPF output selected	50	—	—	kΩ
LPF output impedance	R_{LPF}	I_F=100 µA	—	1	3	kΩ

Note: Applied to RESET, CMD, ST, CH. Not applied to MSM66P54-xx

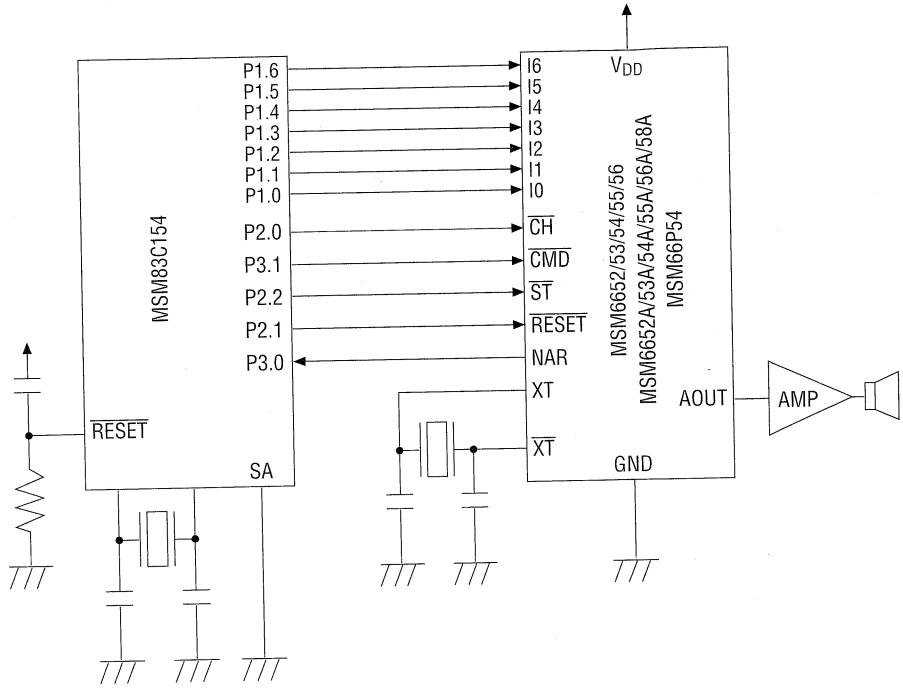
APPLICATION CIRCUITS

(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx)



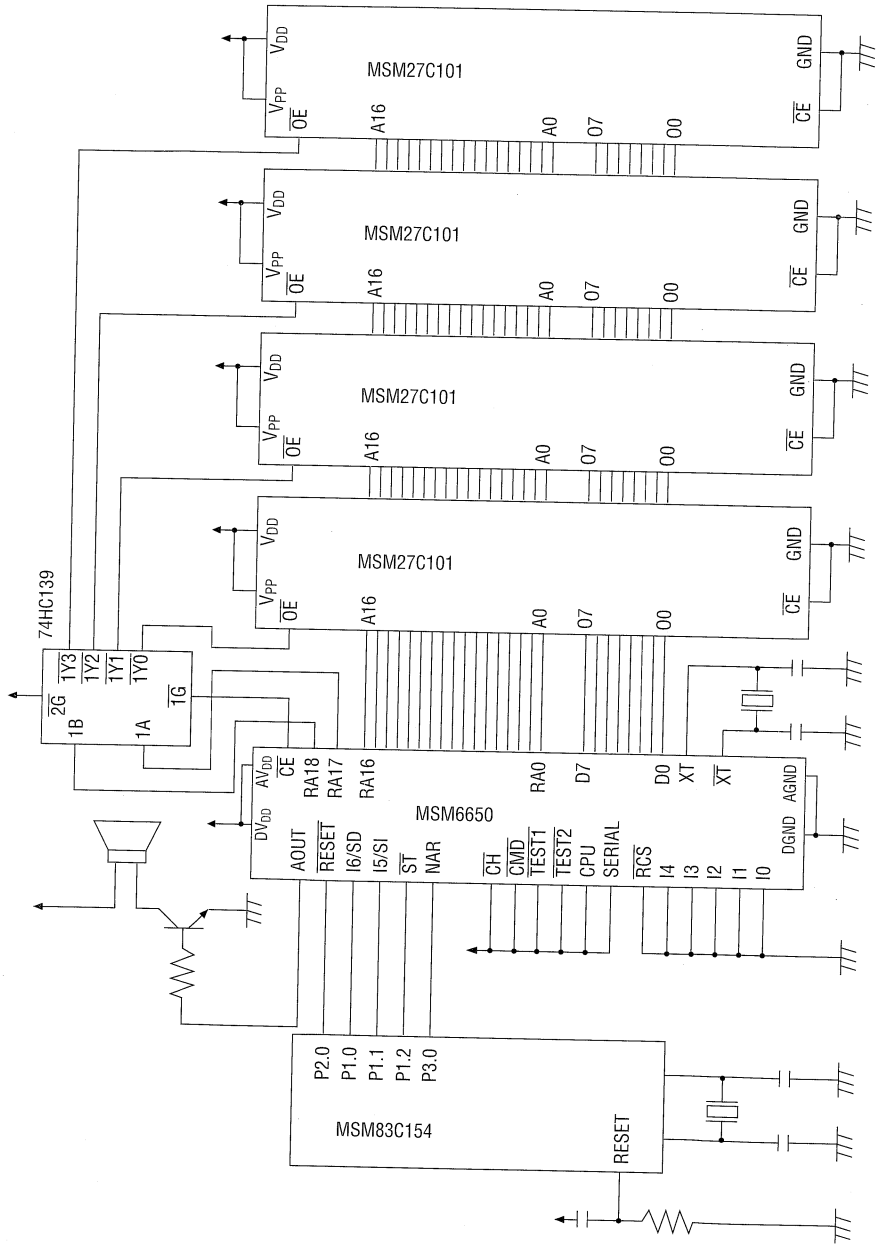
Application Circuit in Serial Input Interface Mode

(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx)



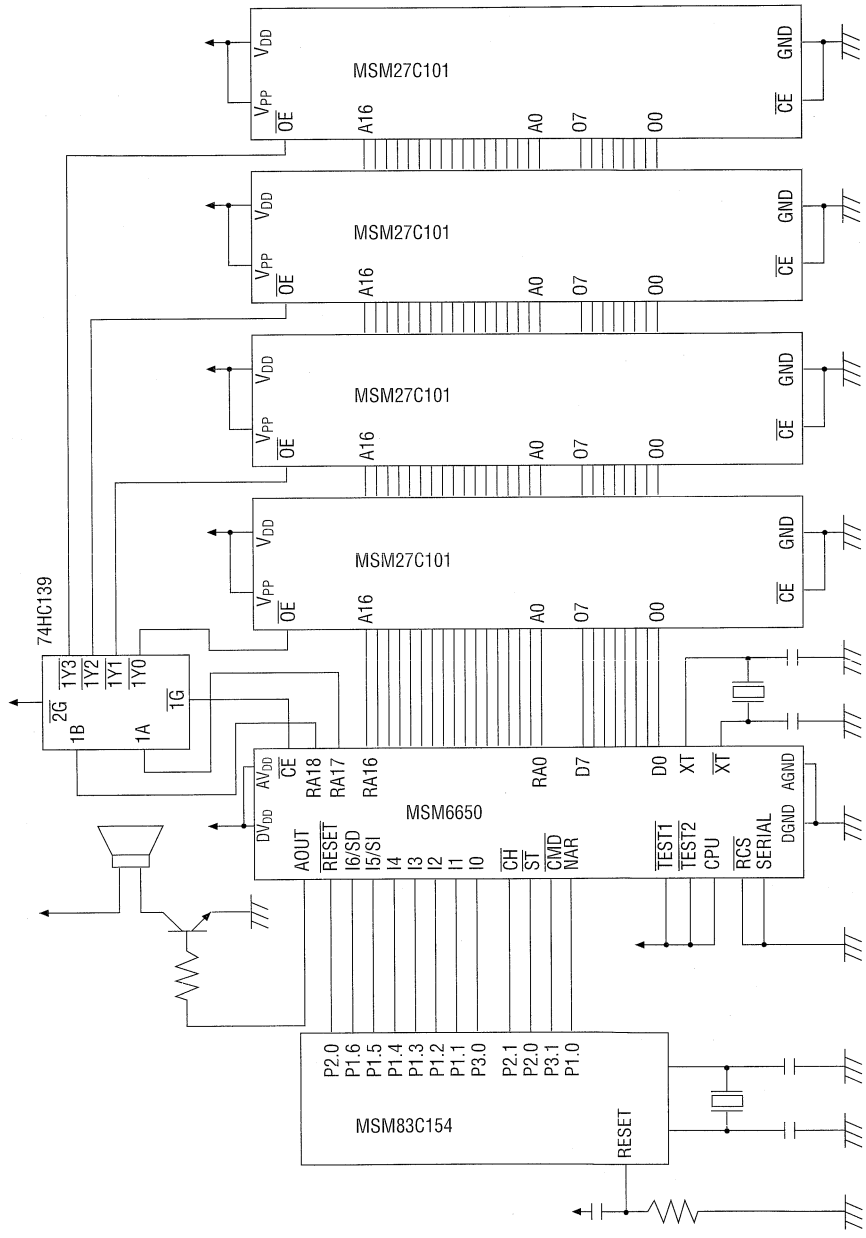
Application circuit in Parallel Input Interface Mode

(MSM6650)



Application Circuit in Microcontroller Interface Mode Using Four 1-Mbit EPROMs (Serial Input Interface)

(MSM6650)



Application Circuit in Microcontroller Interface Mode
Using Four 1-Mbit EPROMs (Parallel Input Interface)

OKI Semiconductor

MSM9802/03/05-xxx

Built-in Mask ROM Voice Synthesis IC

GENERAL DESCRIPTION

The MSM9802/03/05 is a PCM voice synthesis IC with built-in mask ROM.
This IC employs the straight PCM and OKI's nonlinear PCM methods and contains a current mode 10-bit D/A converter and a low-pass filter.
External control has been made easy by the built-in edit ROM that can form sentences by linking phrases.
With the stand-alone mode/microcontroller interface mode switching pin, the MSM9802/03/05 can support various applications.

FEATURES

Device	ROM size*	Speech period (sec)			
		f_{SAM}=4.0 kHz	f_{SAM}=6.4 kHz	f_{SAM}=8.0 kHz	f_{SAM}=16.0 kHz
MSM9802	512 Kbit	16.0	10.0	8.0	4.0
MSM9803	1 Mbit	32.4	20.3	16.2	8.1
MSM9805	2 Mbit	65.1	40.7	32.5	16.2

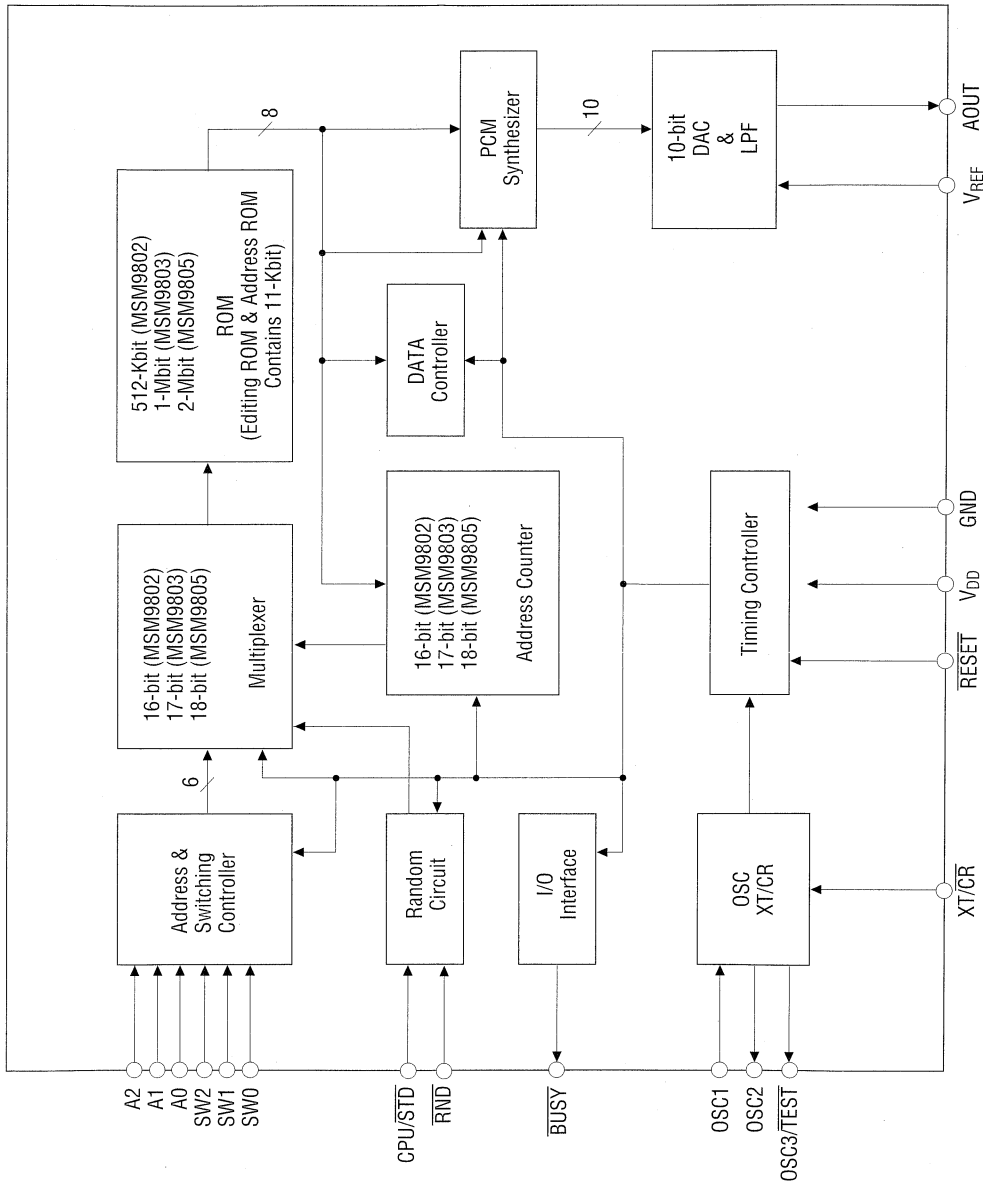
* Actual voice ROM area is smaller by 11 Kbits.

- ROM custom
- 8-bit straight PCM method/8-bit OKI's nonlinear PCM method
- Built-in edit ROM
- Random playback function
- Sampling frequency : 4.0 kHz/5.3 kHz/6.4 kHz/8.0 kHz/10.6 kHz/12.8 kHz/16.0 kHz
  Note: If RC oscillation is selected, 10.6 kHz, 12.8 kHz, and 16.0 kHz cannot be selected.
- Maximum number of phrases : 63 (Microcontroller interface mode)
  56 (Stand-alone mode)
- Built-in current mode 10-bit D/A converter
- Built-in low-pass filter
- Standby function
- RC oscillation (256 kHz)/ceramic oscillation(4.096 MHz) selectable
- Package options:
  18-pin DIP (DIP18-P-300) (Product name: MSM9802-xxxRS/MSM9803-xxxRS/MSM9805-xxxRS)
  24-pin SOP (SOP24-P-430-K) (Product name: MSM9802-xxxGS-K/MSM9803-xxxGS-K/MSM9805-xxxGS-K)
  Chip

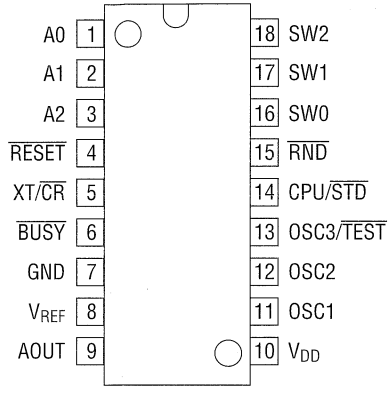
Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

(1) STAND-ALONE MODE

BLOCK DIAGRAM

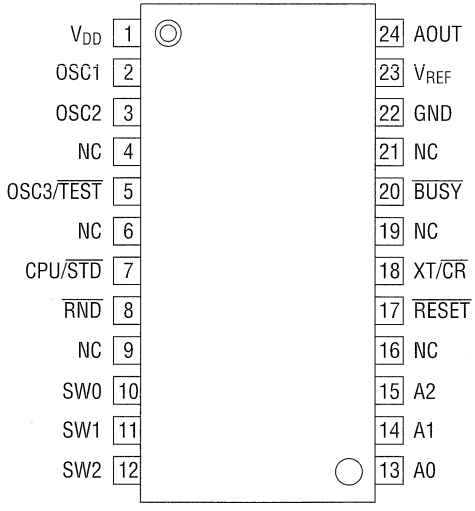


PIN CONFIGURATION (TOP VIEW) (CPU/$\overline{\text{STD}}$: " L" level)



18-Pin Plastic DIP

Note: Applicable to MSM9802-XXXRS, MSM9803-XXXRS, and MSM9805-XXXRS.



24-Pin Plastic SOP

Note: Applicable to MSM9802-XXXGS-K, MSM9803-XXXGS-K, and MSM9805-XXXGS-K.

PIN DESCRIPTIONS

Symbol	Type	Description
$\overline{\text{RESET}}$	I	The IC enters the standby state if this pin is set to "L" level. At this time, oscillation stops and AOUT output becomes GND level, then the IC returns to the initial state. This IC has a built-in power-on reset circuit. To operate power-on reset correctly, apply the power within 1 ms up to V_{DD}. If the power cannot be applied within 1 ms, apply a $\overline{\text{RESET}}$ pulse during power-on. This pin has an internal pull-up resistor.
$\overline{\text{BUSY}}$	O	Outputs "L" level while voice is being played back. In "H" level when power is turned ON.
XT/$\overline{\text{CR}}$	I	XT/CR switching pin. Set to "H" level if ceramic oscillation is used. Set to "L" level if RC oscillation is used.
CPU/$\overline{\text{STD}}$	I	Microcontroller interface/stand-alone mode switching pin. Set to "L" level if the MSM9802/03/05 is used in stand-alone mode.
V_{REF}	I	Volume setting pin. If this pin is set to GND level, the maximum current is forced in. If this pin is set to V_{DD} level, the minimum current is forced in. This pin has a built-in pull-down resistor of approx. 10 kΩ.
AOUT	O	Voice output pin. The voice signals are output as current changes. A logic "L" is output from this pin in standby state.
GND	—	Ground pin.
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 μF or more between V_{DD} and GND pins.
OSC1	I	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Input from this pin if external clock is used.
OSC2	O	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Leave this pin open if external clock is used. Outputs "L" level in standby state.
OSC3/$\overline{\text{TEST}}$	O	Leave this pin open when ceramic oscillation is used. RC connection pin when RC oscillation is selected. Outputs "H" level in standby state when RC oscillation is selected.
$\overline{\text{RND}}$	I	Random playback starts if $\overline{\text{RND}}$ pin is set to "L" level. Fetches addresses from random address generation circuit in the IC at fall of $\overline{\text{RND}}$. Set to "H" level when the random playback function is not used. This pin has internal pull-up resistor.
SW0 - SW2	I	Phrase input pins corresponding to vocalized sound. If input changes, SW0 to SW2 pins fetch addresses after 16 ms and start voice synthesis. Each of these pins has internal pull-down resistor.
A0 - A2	I	Phrase input pins corresponding to vocalized sound. A0 input becomes invalid if the random playback function is used.

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	—	+2.0 to +5.5			V
Operating Temperature	T_{op}	—	−40 to +85			°C
Master Clock Frequency 1	f_{OSC1}	When crystal is selected	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Master Clock Frequency 2	f_{OSC2}	When RC is selected (*1)	200	256	300	kHz

*1 The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the external R and C.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH}=−1 mA	4.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"H" Input Current 2 *1	I_{IH2}	Internal pull-down resistor	30	90	200	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
"L" Input Current 2 *2	I_{IL2}	Internal pull-up resistor	−200	−90	−30	µA
Operating Power Consumption	I_{DD}	—	—	6	10	mA
Standby Power Consumption	I_{DS}	Ta=−40 to +70°C	—	—	10	µA
		Ta=+70 to +85°C	—	—	50	µA
AOUT Output Current	I_{AOVT}	At maximum current output	6	9.5	15	mA
V_{REF} Pin Pull-down Resistor	R_{VREF}	—	7	10	13	kΩ

*1 Applicable to SW2-SW0
*2 Applicable to $\overline{\text{RESET}}$, $\overline{\text{RND}}$

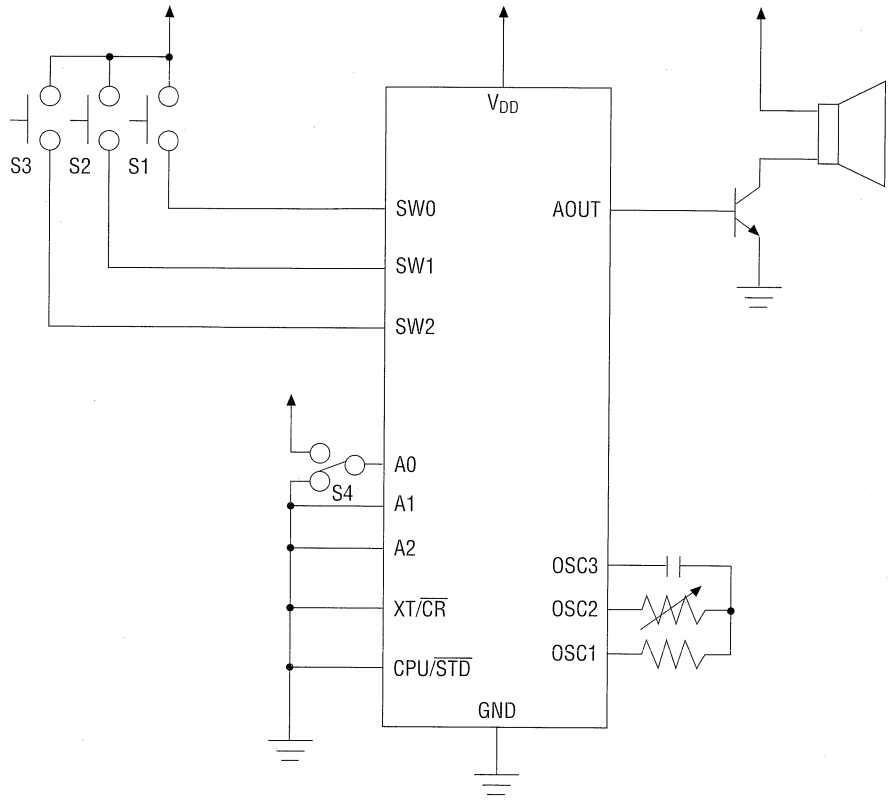
DC Characteristics

(V_{DD}=3.1 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.7	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Output Voltage	V_{OH}	I_{OH}=–1 mA	2.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"H" Input Current 2 *1	I_{IH2}	Internal pull-down resistor	10	30	100	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
"L" Input Current 2 *2	I_{IL2}	Internal pull-up resistor	–100	–30	–10	µA
Operating Power Consumption	I_{DD}	—	—	4	7	mA
Standby Power Consumption	I_{DS}	Ta=–40 to +70°C	—	—	1	µA
		Ta=+70 to +85°C	—	—	10	µA
AOUT Output Current	I_{AOVT}	At maximum current output	1.4	3.2	5	mA
V_{REF} Terminal Pull-down Resistor	R_{VREF}	—	7	10	13	kΩ

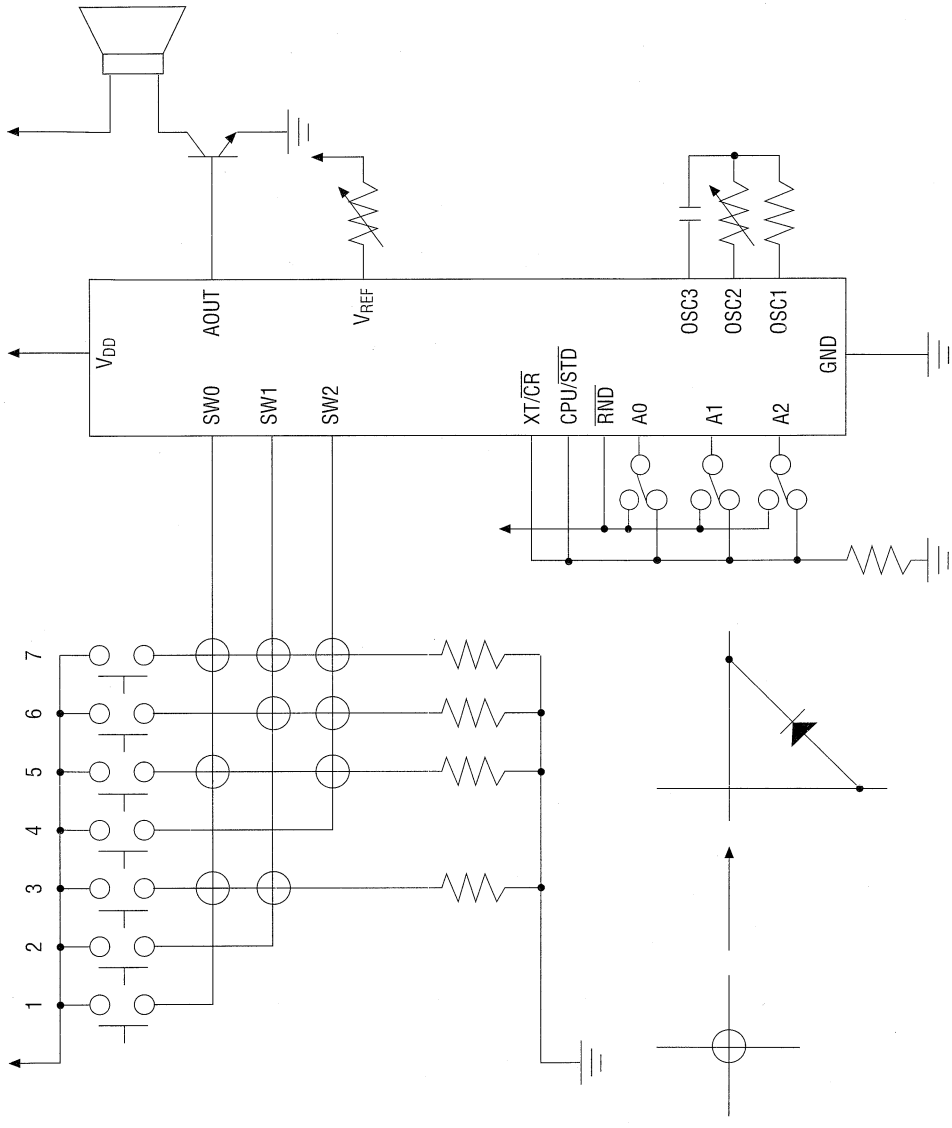
*1 Applicable to SW2-SW0
*2 Applicable to $\overline{\text{RESET}}$, $\overline{\text{RND}}$

APPLICATION CIRCUITS



		A2	A1	A0	SW2	SW1	SW0	Address [HEX]
S4="L"	S1	0	0	0	0	0	1	01
	S2	0	0	0	0	1	0	02
	S3	0	0	0	1	0	0	04
S4="H"	S1	0	0	1	0	0	1	09
	S2	0	0	1	0	1	0	0A
	S3	0	0	1	1	0	0	0C

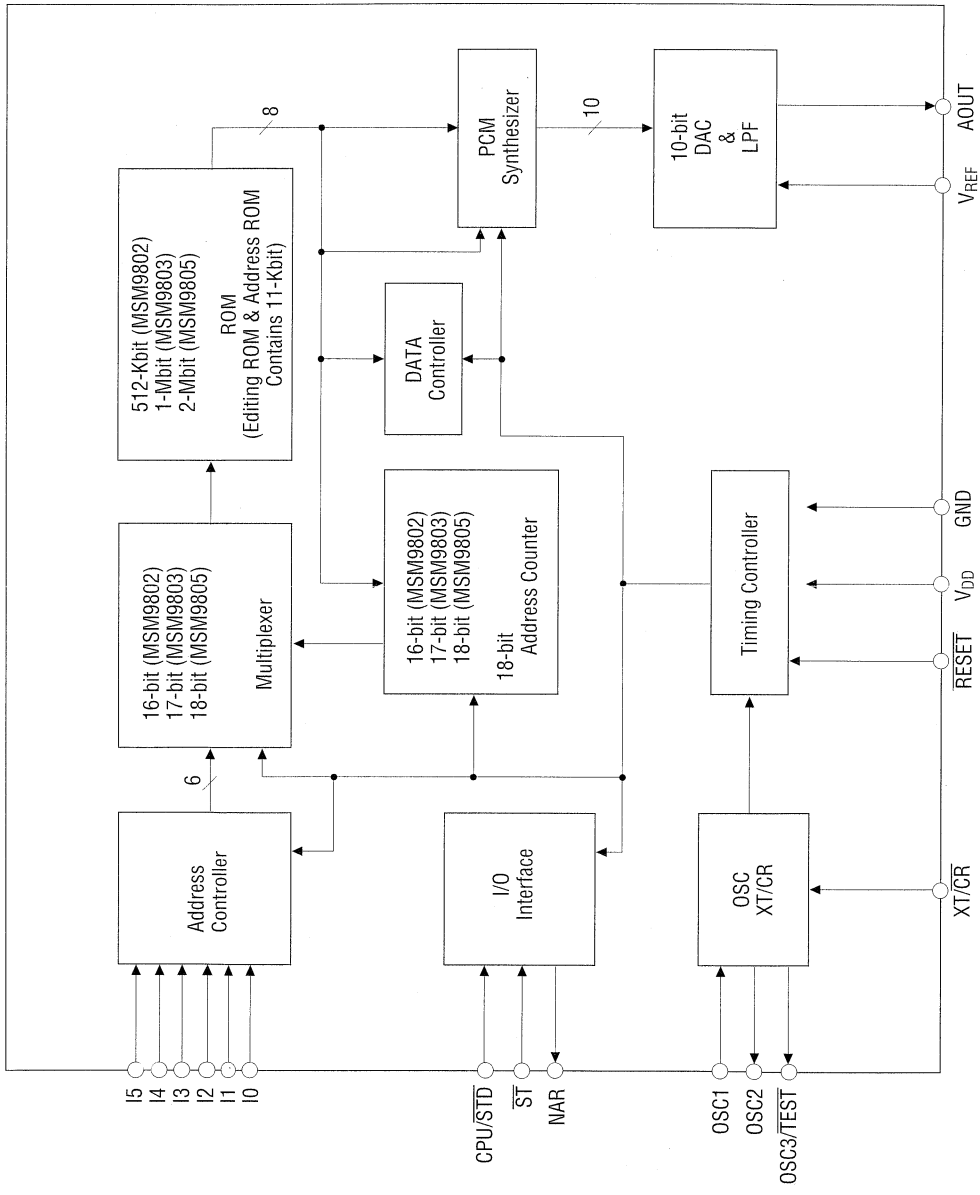
Application Circuit for Playing Six Phrases Using Four Switches



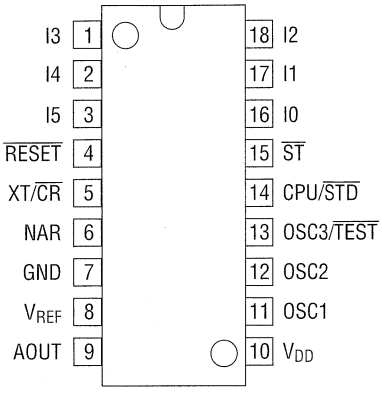
Application Circuit Using Switches

(2) MICROCONTROLLER INTERFACE MODE

BLOCK DIAGRAM

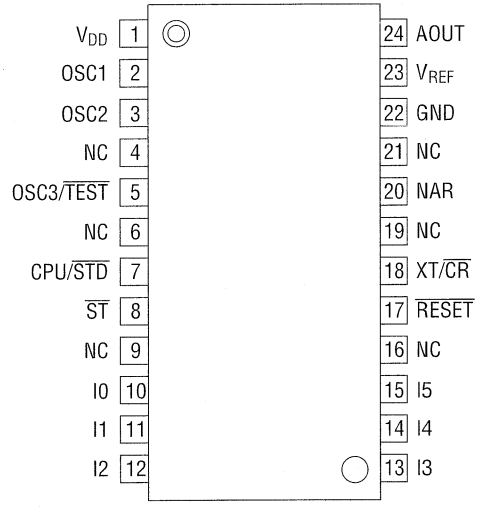


PIN CONFIGURATION (TOP VIEW) (CPU/$\overline{\text{STD}}$: "H" level)



18-Pin Plastic DIP

Note: Applicable to MSM9802-XXXRS, MSM9803-XXXRS, and MSM9805-XXXRS.



24-Pin Plastic SOP

Note: Applicable to MSM9802-XXXGS-K, MSM9803-XXXGS-K, and MSM9805-XXXGS-K.

PIN DESCRIPTIONS

Symbol	Type	Description
$\overline{RESET}$	I	The IC enters the standby state if this pin is set to "L" level. At this time, oscillation stops and AOUT output becomes GND level, then the IC returns to the initial state. This IC has a built-in power-on reset circuit. To operate power-on reset correctly, apply the power within 1 ms up to V_{DD}. If the power cannot be applied within 1ms, apply a $\overline{RESET}$ pulse during power-on. This pin has an internal pull-up resistor.
NAR	O	Signal output pin that indicates whether the 6-bit LATCH (see Block Diagram) is idle. NAR at "H" level indicates that the LATCH is empty and $\overline{ST}$ input is enabled.
XT/$\overline{CR}$	I	XT/CR switching pin. Set to "H" level if ceramic oscillation is used. Set to "L" level if RC oscillation is used.
CPU/$\overline{STD}$	I	Microcontroller interface/stand-alone mode switching pin. Set to "H" level if the MSM9802/03/05 is used in microcontroller interface mode.
V_{REF}	I	Volume setting pin. If this pin is set to GND level, the maximum current is forced in, and if set to V_{DD} level, the minimum current is forced in. This pin has a built-in pull-down resistor of approx 10 kΩ.
AOUT	O	Voice output pin. The voice signals are output as current changes. A logic "L" is output from this pin in standby state.
GND	—	Ground pin.
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 µF or more between this pin and the GND pin.
OSC1	I	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Input from this pin if external clock is used.
OSC2	O	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Leave this pin open if external clock is used. Outputs "L" level in standby state.
OSC3/$\overline{TEST}$	O	Leave this pin open when ceramic oscillation is used. RC connection pin when RC oscillation is selected. Outputs "H" level in standby state when RC oscillation is selected.
$\overline{ST}$	I	Voice synthesis starts at fall of $\overline{ST}$, and addresses I0 to I5 are fetched at rise of $\overline{ST}$. Input $\overline{ST}$ when NAR, the status signal, is at "H" level. This pin has internal pull-up resistor.
I0 - I5	I	Phrase input pins corresponding to vocalized sound.

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	—	+2.0 to +5.5			V
Operating Temperature	T_{op}	—	–40 to +85			°C
Original Oscillation Frequency 1	f_{OSC1}	When crystal is selected	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Original Oscillation Frequency 2	f_{OSC2}	When RC is selected (*1)	200	256	300	kHz

*1 The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the external R and C.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH}=–1 mA	4.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
"L" Input Current 2 (*1)	I_{IL2}	Internal pull-up resistor	–200	–90	–30	µA
Operating Power Consumption	I_{DD}	—	—	6	10	mA
Standby Power Consumption	I_{DS}	Ta=–40 to +70°C	—	—	10	µA
		Ta=+70 to +85°C	—	—	50	µA
AOUT Output Current	I_{AOUT}	At maximum current output	6	9.5	15	mA
V_{REF} Pin Pull-Down Resistor	R_{VREF}	Ta=+25°C	7	10	13	kΩ

*1 Applicable to $\overline{RESET}$, $\overline{ST}$

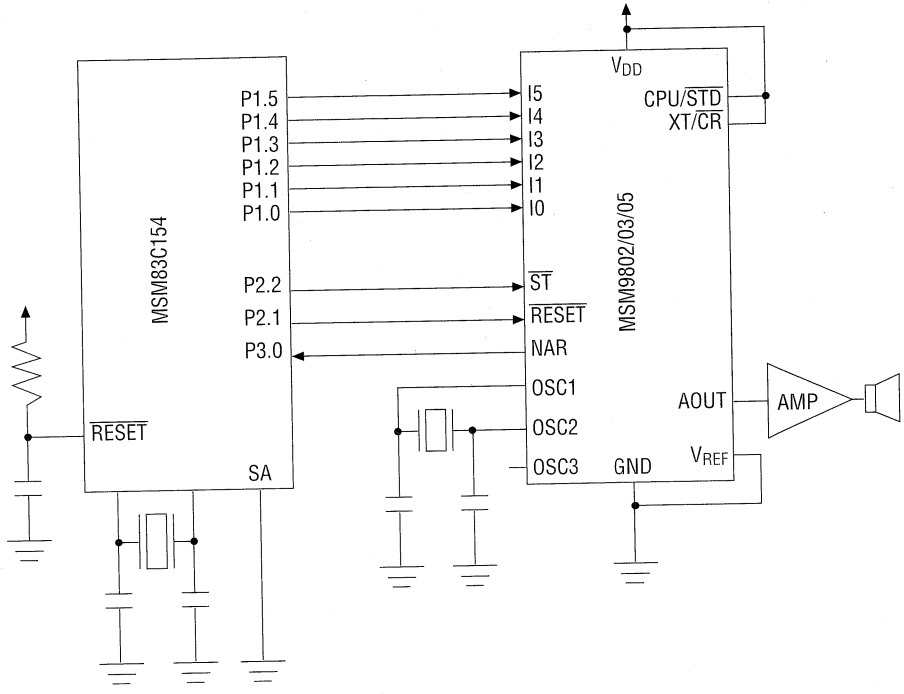
DC Characteristics

(V_{DD}=3.1 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.7	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Output Voltage	V_{OH}	I_{OH}=–1 mA	2.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
"L" Input Current 2 (*1)	I_{IL2}	Internal pull-up resistor	–100	–30	–10	µA
Operating Power Consumption	I_{DD}	—	—	4	7	mA
Standby Power Consumption	I_{DS}	Ta=–40 to +70°C	—	—	1	µA
		Ta=+70 to +85°C	—	—	10	µA
AOUT Output Current	I_{AOUT}	At maximum current output	1.4	3.2	5	mA
V_{REF} Pin Pull-down Resistor	R_{VREF}	Ta=+25°C	7	10	13	kΩ

*1 Applicable to $\overline{\text{RESET}}$, $\overline{\text{ST}}$

APPLICATION CIRCUIT



Application Circuit when Used as Microcontroller Interface

OKI Semiconductor

MSM98P05

Built-in 2-Mbit OTP ROM Voice Synthesis IC

GENERAL DESCRIPTION

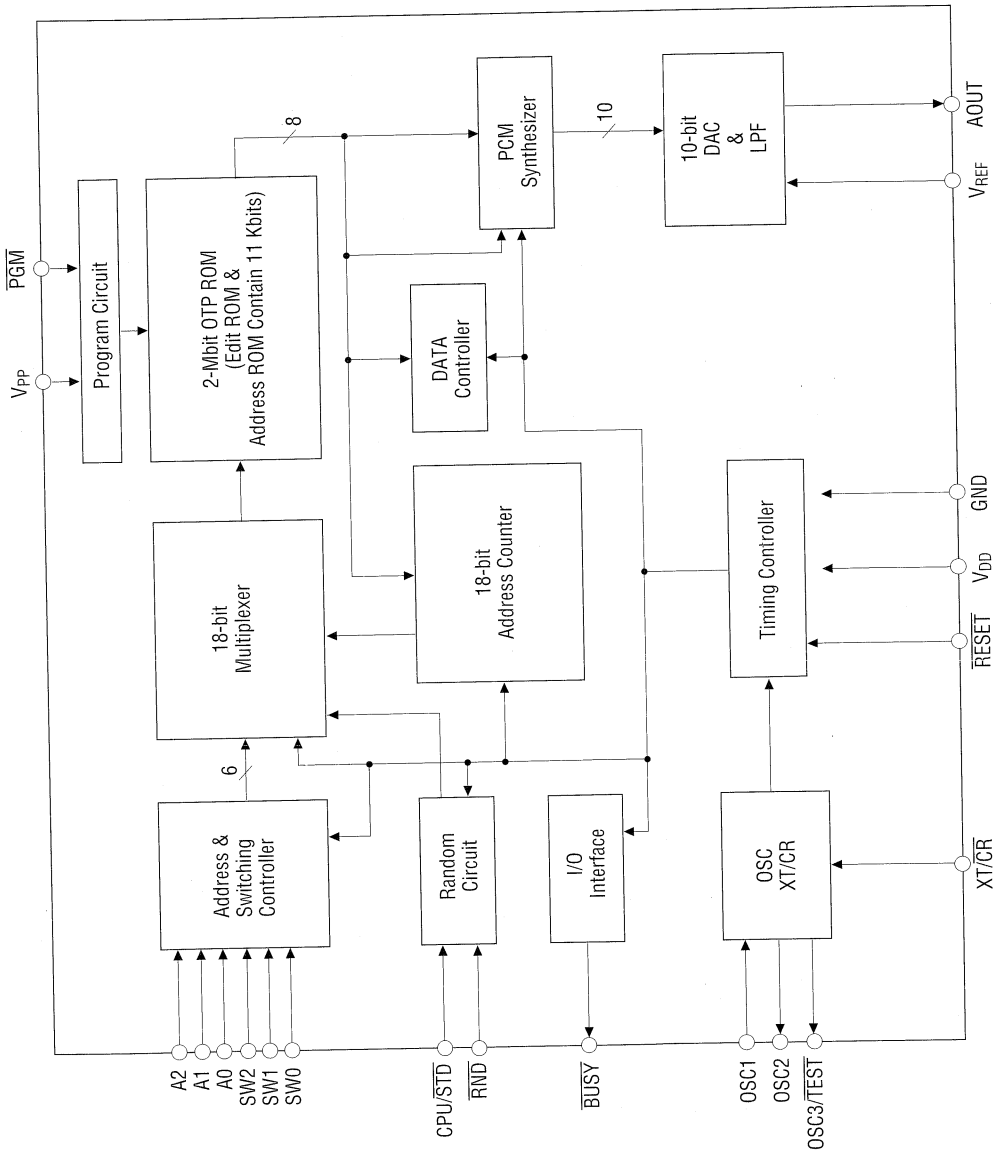
The MSM98P05 is a PCM voice synthesis IC with built-in 2-Mbit OTP (One Time PROM). This IC employs the straight PCM and OKI's nonlinear PCM methods and contains a current mode 10-bit D/A converter and a low-pass filter.
External control has been made easy by the built-in edit ROM that can form sentences by linking phrases.
With the stand-alone mode/microcontroller interface mode switching pin, the MSM98P05 can support various applications.
The products with build-in OTP are suited to applications to be produced in small quantities in a wide variery or those to be delivered with an early deadline. Demand like these, that is, production in small quantities in a wide variety and delivery with an early deadline is what the products MSM9800 family with build-in mask ROM cannot meet.

FEATURES

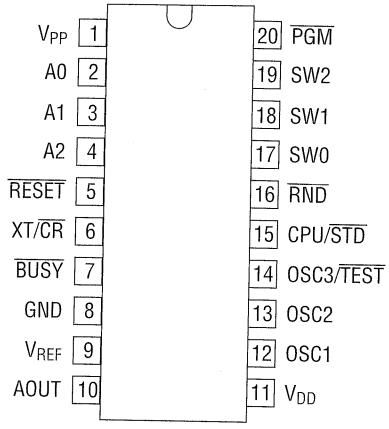
- 8-bit straight PCM method/8-bit OKI's nonlinear PCM method
- Built-in edit ROM
- Random playback function
- Sampling frequency : 4.0 kHz/5.3 kHz/6.4 kHz/8.0 kHz/10.6 kHz/12.8 kHz/16.0 kHz
  Note: If RC oscillation is selected, 10.6 kHz, 12.8 kHz, and 16.0 kHz cannot be selected.
- Maximum number of phrases : 63 (Microcontroller interface mode)
  56 (Stand-alone mode)
- Built-in current mode 10-bit D/A converter
- Built-in low-pass filter
- Standby function
- RC oscillation (256 kHz)/ceramic oscillation(4.096 MHz) selectable
- Package options:
  20-pin plastic DIP (DIP20-P-300-W1) (Product name : MSM98P05RS)
  24-pin plastic SOP (SOP24-P-430-K) (Product name : MSM98P05GS-K)

STAND-ALONE MODE

BLOCK DIAGRAM

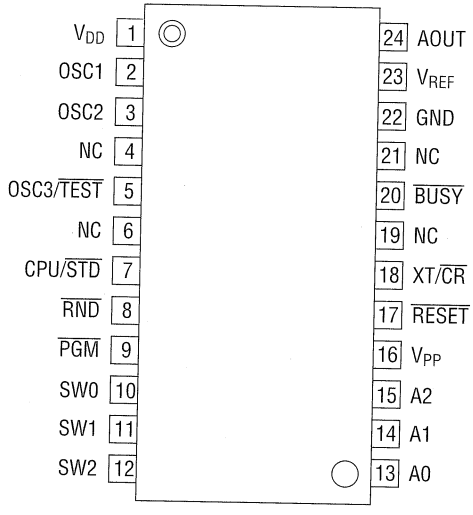


PIN CONFIGURATION (TOP VIEW) (CPU/$\overline{\text{STD}}$: " L" level)



20-Pin Plastic DIP

Note: Applies to MSM98P05RS



24-Pin Plastic SOP

Note: Applies to MSM98P05GS-K

PIN DESCRIPTIONS

Symbol	Type	Description
$\overline{\text{RESET}}$	I	The IC enters the standby state if this pin is set to "L" level. At this time, oscillation stops and AOUT output becomes GND level, then the IC returns to the initial state. This IC has a built-in power-on reset circuit. To operate power-on reset correctly, apply the power within 1 ms up to V_{DD}. If the power cannot be applied within 1 ms, apply a $\overline{\text{RESET}}$ pulse during power-on. This pin has an internal pull-up resistor.
$\overline{\text{BUSY}}$	O	Outputs "L" level while voice is being played back. In "H" level when power is turned ON.
XT/$\overline{\text{CR}}$	I	XT/CR switching pin. Set to "H" level if ceramic oscillation is used. Set to "L" level if RC oscillation is used.
CPU/$\overline{\text{STD}}$	I	Microcontroller interface/stand-alone mode switching pin. Set to "L" level if the MSM9802 is used in stand-alone mode.
V_{REF}	I	Volume setting pin. If this pin is set to GND level, the maximum current is forced in. If this pin is set to V_{DD} level, the minimum current is forced in. This pin has a built-in pull-down resistor of approx. 10 kΩ.
AOUT	O	Voice output pin. The voice signals are output as current changes. A logic "L" is output from this pin in standby state.
GND	—	Ground pin.
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 µF or more between V_{DD} and GND pins.
OSC1	I	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Input from this pin if external clock is used.
OSC2	O	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Leave this pin open if external clock is used. Outputs "L" level in standby state.
OSC3/$\overline{\text{TEST}}$	O	Leave this pin open when ceramic oscillation is used. RC connection pin when RC oscillation is selected. Outputs "H" level in standby state when RC oscillation is selected.
$\overline{\text{RND}}$	I	Random playback starts if $\overline{\text{RND}}$ pin is set to "L" level. Fetches addresses from random address generation circuit in the IC at fall of $\overline{\text{RND}}$. Set to "H" level when the random playback function is not used. This pin has internal pull-up resistor.
SW0 - SW2	I	Phrase input pins corresponding to vocalized sound. If input changes, SW0 to SW2 pins fetch addresses after 16 ms and start voice synthesis. Each of these pins has internal pull-down resistor.
A0 - A2	I	Phrase input pins corresponding to vocalized sound. A0 input becomes invalid if the random playback function is used.
V_{PP}	—	Power supply pin for writing to the built-in OTP.
$\overline{\text{PGM}}$	I	Interface pin for writing to the built-in OTP.

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	—	+2.4 to +5.5			V
Operating Temperature	T_{op}	—	−40 to +85			°C
Master Clock Frequency 1	f_{OSC1}	When crystal is selected	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Master Clock Frequency 2	f_{OSC2}	When RC is selected (*1)	200	256	300	kHz

*1 The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the external R and C.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH}=−1 mA	4.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"H" Input Current 2 *1	I_{IH2}	Internal pull-down resistor	30	90	200	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
"L" Input Current 2 *2	I_{IL2}	Internal pull-up resistor	−200	−90	−30	µA
Operating Power Consumption	I_{DD}	—	—	6	10	mA
Standby Power Consumption	I_{DS}	—	—	—	10	µA
V_{REF} Pin Pull-down Resistor	R_{VREF}	Ta=+25°C	7	10	13	kΩ

*1 Applicable to SW2-SW0
*2 Applicable to $\overline{\text{RESET}}$, $\overline{\text{RND}}$

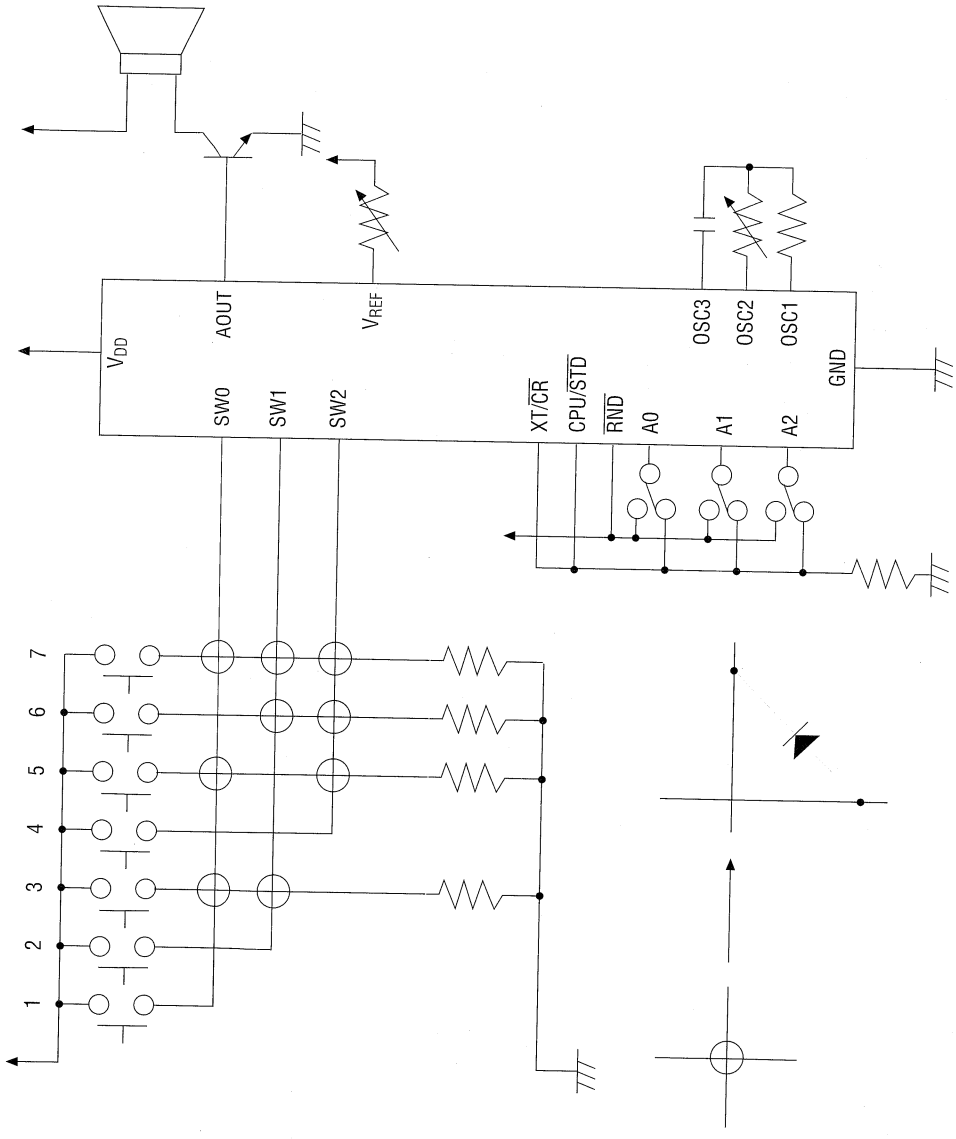
DC Characteristics

(V_{DD}=3.1 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.7	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Output Voltage	V_{OH}	I_{OH}=−1 mA	2.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH}=V_{DD}$	—	—	10	µA
"H" Input Current 2 *1	I_{IH2}	Internal pull-down resistor	10	30	100	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
"L" Input Current 2 *2	I_{IL2}	Internal pull-up resistor	−100	−30	−10	µA
Operating Power Consumption	I_{DD}	—	—	4	7	mA
Standby Power Consumption	I_{DS}	—	—	—	1	µA
V_{REF} Terminal Pull-down Resistor	R_{VREF}	Ta=+25°C	7	10	13	kΩ

*1 Applicable to SW2-SW0
*2 Applicable to $\overline{\text{RESET}}$, $\overline{\text{RND}}$

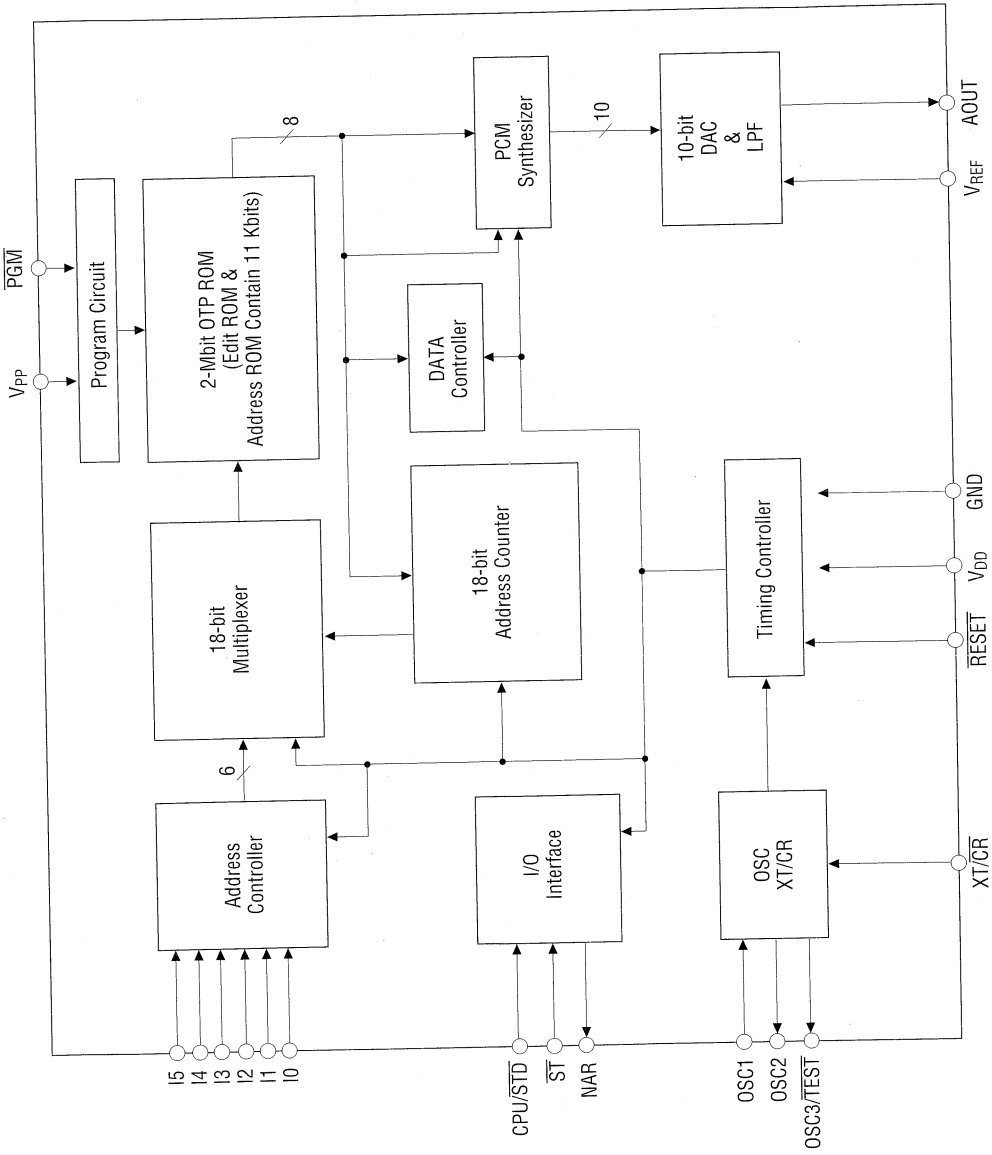
APPLICATION CIRCUIT



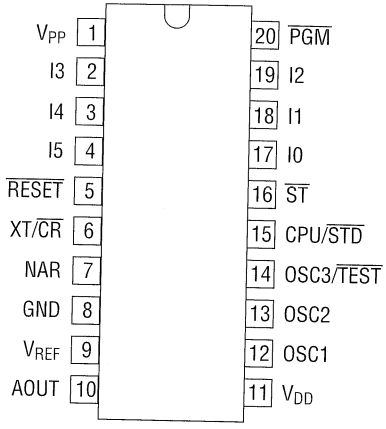
Application Circuit Using Switches

MICROCONTROLLER INTERFACE MODE

BLOCK DIAGRAM

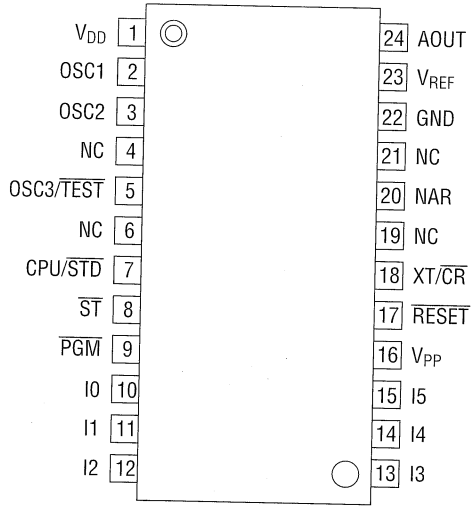


PIN CONFIGURATION (TOP VIEW) (CPU/$\overline{\text{STD}}$: "H" level)



20-Pin Plastic DIP

Note: Applies to MSM98P05RS



24-Pin Plastic SOP

Note: Applies to MSM98P05GS-K

PIN DESCRIPTIONS

Symbol	Type	Description
$\overline{\text{RESET}}$	I	The IC enters the standby state if this pin is set to "L" level. At this time, oscillation stops and AOUT output becomes GND level, then the IC returns to the initial state. This IC has a built-in power-on reset circuit. To operate power-on reset correctly, apply the power within 1 ms up to V_{DD}. If the power cannot be applied within 1ms, apply a $\overline{\text{RESET}}$ pulse during power-on. This pin has an internal pull-up resistor.
NAR	O	Signal output pin that indicates whether the 6-bit LATCH (see Block Diagram) is idle. NAR at "H" level indicates that the LATCH is empty and $\overline{\text{ST}}$ input is enabled.
XT/$\overline{\text{CR}}$	I	XT/CR switching pin. Set to "H" level if ceramic oscillation is used. Set to "L" level if RC oscillation is used.
CPU/$\overline{\text{STD}}$	I	Microcontroller interface/stand-alone mode switching pin. Set to "H" level if the MSM9802 is used in microcontroller interface mode.
V_{REF}	I	Volume setting pin. If this pin is set to GND level, the maximum current is forced in. If this pin is set to V_{DD} level, the minimum current is forced in. This pin has a built-in pull-down resistor of approx. 10 kΩ.
AOUT	O	Voice output pin. The voice signals are output as current changes. A logic "L" is output from this pin in standby state.
GND	—	Ground pin.
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and the GND pin.
OSC1	I	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Input from this pin if external clock is used.
OSC2	O	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Leave this pin open if external clock is used. Outputs "L" level in standby state.
OSC3/$\overline{\text{TEST}}$	O	Leave this pin open when ceramic oscillation is used. RC connection pin when RC oscillation is selected. Outputs "H" level in standby state when RC oscillation is selected.
$\overline{\text{ST}}$	I	Voice synthesis starts at fall of $\overline{\text{ST}}$, and addresses I0 to I5 are fetched at rise of $\overline{\text{ST}}$. Input $\overline{\text{ST}}$ when NAR, the status signal, is at "H" level. This pin has internal pull-up resistor.
I0 - I5	I	Phrase input pins corresponding to vocalized sound.
V_{PP}	—	Power supply pin for writing to the built-in OTP.
$\overline{\text{RGM}}$	I	Interface pin for writing to the built-in OTP.

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	—	+2.4 to +5.5			V
Operating Temperature	T_{op}	—	−40 to +85			°C
			Min.	Typ.	Max.	
Original Oscillation Frequency 1	f_{OSC1}	When crystal is selected	3.5	4.096	4.5	MHz
Original Oscillation Frequency 2	f_{OSC2}	When RC is selected (*1)	200	256	300	kHz

*1 The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the external R and C.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH}=−1 mA	4.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
"L" Input Current 2 (*1)	I_{IL2}	Internal pull-up resistor	−200	−90	−30	µA
Operating Power Consumption	I_{DD}	—	—	6	10	mA
Standby Power Consumption	I_{DS}	—	—	—	10	µA
V_{REF} Pin Pull-down Resistor	R_{VREF}	Ta=+25°C	7	10	13	kΩ

*1 Applicable to $\overline{\text{RESET}}$, $\overline{\text{ST}}$

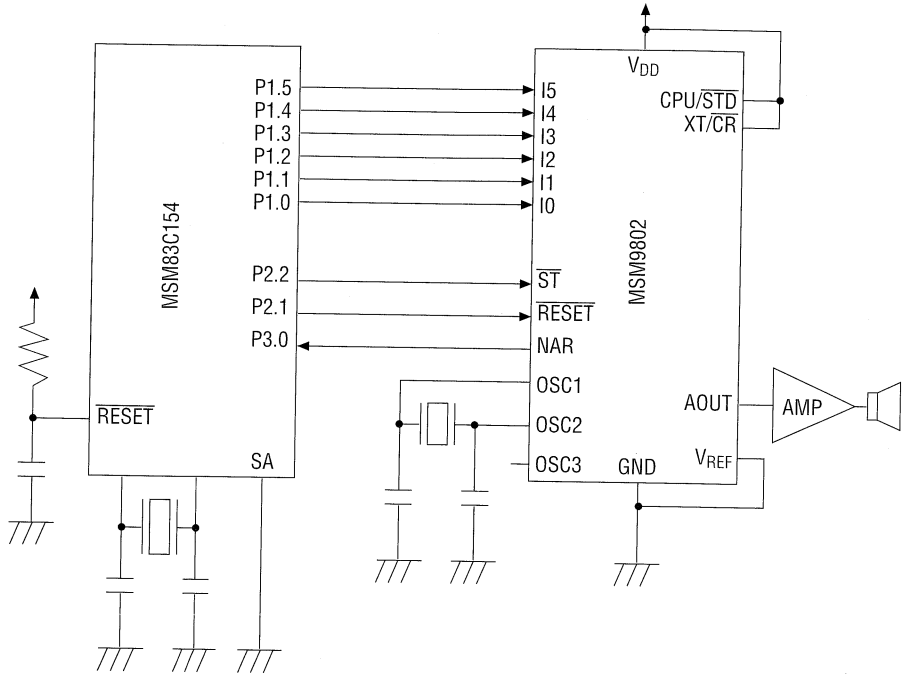
DC Characteristics

(V_{DD}=3.1 V, GND=0 V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.7	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Output Voltage	V_{OH}	I_{OH}=–1 mA	2.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"L" Input Current 1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
"L" Input Current 2 (*1)	I_{IL2}	Internal pull-up resistor	–100	–30	–10	µA
Operating Power Consumption	I_{DD}	—	—	4	7	mA
Standby Power Consumption	I_{DS}	—	—	—	1	µA
V_{REF} Pin Pull-down Resistor	R_{VREF}	Ta=+25°C	7	10	13	kΩ

*1 Applicable to $\overline{\text{RESET}}$, $\overline{\text{ST}}$

APPLICATION CIRCUIT



Application Circuit when Used as Microcontroller Interface

OKI Semiconductor

MSM9810

8-channel Mixing OKI ADPCM Type Voice LSI

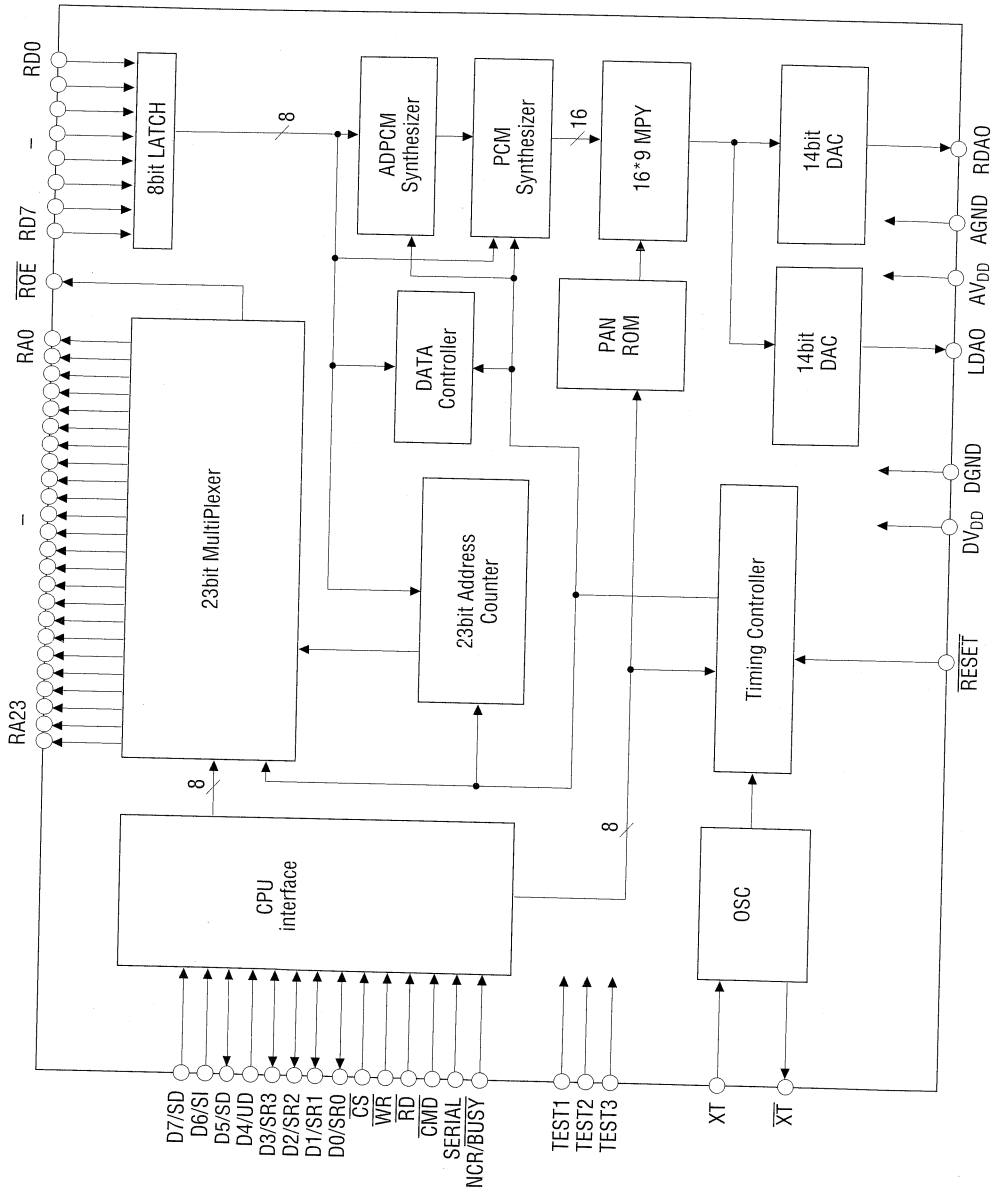
GENERAL DESCRIPTION

The MSM9810, to which up to 128 Mbits of ROM and/or EPROM storing voice data can directly be connected externally , is an IC that can playback 8 channels simultaneously.
The device is straight 8-bit PCM playback, non-linear 8-bit PCM playback, 4-bit ADPCM playback, and 4-bit ADPCM2 playback selectable and provides 2-channel stereo output and volume control.
The MSM9810 can easily configure a system by connecting voice data storage memory, power amplifier, and CPU externally.

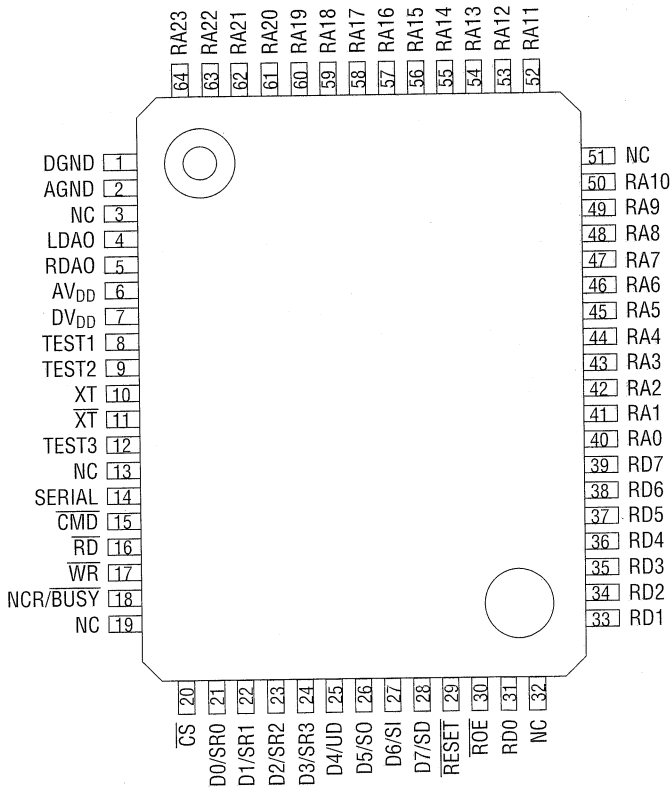
FEATURES

- Non-linear 8-bit PCM / straight 8-bit PCM / 4-bit ADPCM / 4-bit ADPCM2
- Built-in edit ROM function
- 8-channel mixing function
- Master clock frequency : 4.096 MHz
- Sampling frequency : 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.7 kHz, 12.8 kHz, 16.0 kHz, 21.3 kHz, 25.6kHz, 32.0kHz
- Maximum number of phrases : 256
- Output channel : L/R 2 channels
- Built-in volume control function (for each output channel)
- Built-in 14-bit D/A converter
- Built–in low–pass filter
- Package :
  64-pin plastic QFP(QFP64-P-1420-BK)(Product name : MSM9810GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

64-pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description
RA23-RA0	O	Address pin for external memory.
RD7-RD0	I	Data pin for external memory.
$\overline{ROE}$	O	Output enable pin for external memory.
$\overline{CMD}$	I	Command data select pin for CPU interface.
$\overline{RD}$	I	Read pin for CPU interface.
$\overline{WR}$	I	Write pin for CPU interface.
$\overline{CS}$	I	Chip select pin for CPU interface.
D7/SD	I/O	Data bus pin for CPU interface in parallel input interface. Serial data input pin in serial input interface.
D6/SI	I/O	Data bus pin for CPU interface in parallel input interface. Serial clock input pin in serial input interface.
D5/SD	I/O	Data bus pin for CPU interface in parallel input interface. Serial output pin in serial input interface.
D4/UD	I/O	Data bus pin for CPU interface in parallel input interface. Status channel select pin in serial input interface.
D3/SR3 D2/SR2 D1/SR1 D0/SR0	I/O	Data bus pin for CPU interface in parallel input interface. Status signal output pin in serial input interface. When UD pin is "H", channels 8 to 5 are output, and when UD pin is "L", channels 4 to 1 are output.
LDA0	O	DA output pin at left side.
RDA0	O	DA output pin at right side.
XT	I	XTAL or ceramic oscillator connection pin. 1 MΩ of feedback resistance is built in between pin XT (this pin) and $\overline{XT}$. When an external clock is used, input clock from this pin.
$\overline{XT}$	O	XTAL or ceramic oscillator connection pin. In standby status, this pin outputs "L" level. When external clock is used, leave this pin open.
$\overline{RESET}$	I	LSI enters standby state when "L" is input to this pin. At this time, oscillation stops, DA output becomes GND, and LSI returns to initial state. The LSI has a built-in power-on reset circuit. To operate the power-on reset circuit normally, raise power supply within 1 ms. If power supply cannot be raised within 1 ms, apply the RESET pulse when power is turned on. This pin has internal pull-up resistor.
NCR/$\overline{BUSY}$	I	Status signal select pin. When this pin is "H", NCR is output to D7-D0, and at "L", BUSY is output to D7-D0
TEST1, 2, 3	I	Pin to test LSI. Input "L" level.
DV_{DD}, AV_{DD}	—	Power supply pin.
DGND, AGND	—	GND pin.

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	—	+3.5 to +5.5	V
Operating Temperature	T_{op}	—	−40 to +85	°C
Master Clock Frequency	f_{OSC}	—	16.384	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	4.2	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	0.8	V
High-level Output Voltage	V_{OH}	I_{OH}=−1mA	4.6	—	—	V
Low-level Output Voltage	V_{OL}	I_{OL}= 2mA	—	—	0.4	V
High-level Input Current	I_{IH}	V_{IH}=V_{DD}	—	—	10	µA
Low-level Input Current	I_{IL}	V_{IL}=GND	−10	—	—	µA
Operating Current	I_{DD}	—	—	6	10	mA
Standby Current	I_{DS}	—	—	—	10	µA

MSM5218

ADPCM Voice Analysis/Synthesis IC

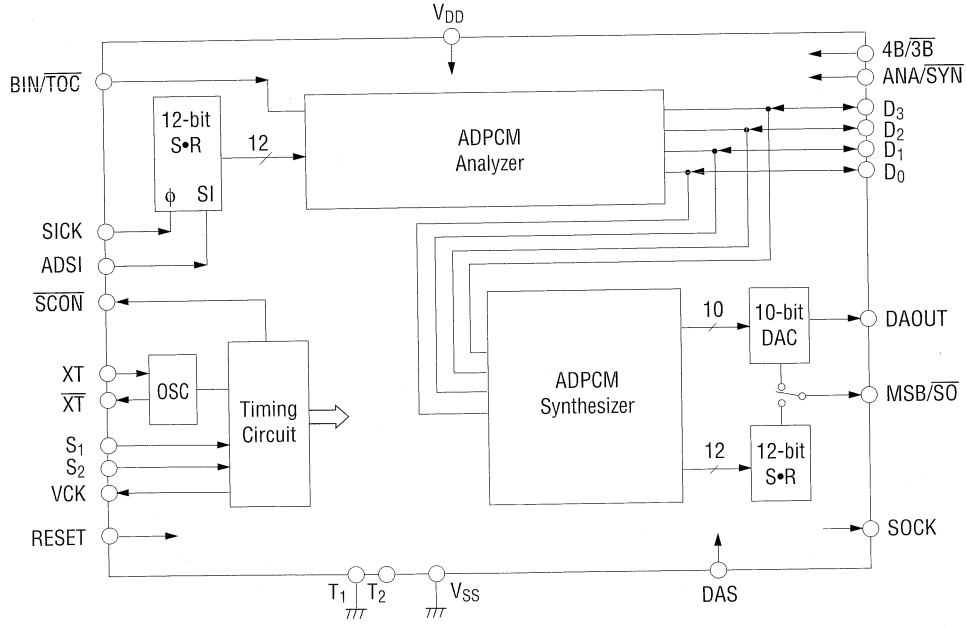
GENERAL DESCRIPTION

The MSM5218 is a complete voice analysis/synthesis IC featuring the Adaptive Differential Pulse Code Modulation (ADPCM) method of data compression. The MSM5218 contains an analysis stage where serial PCM data is compressed to 3- or 4-bit parallel ADPCM data. In addition, a synthesis stage synthesizes PCM data from ADPCM data.

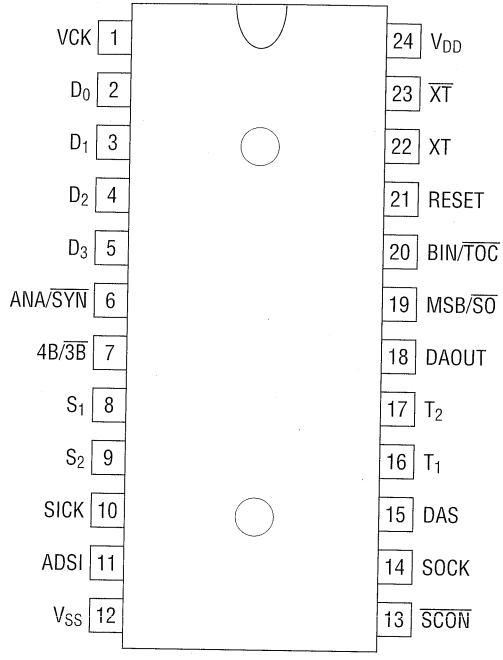
FEATURES

- ADPCM data compatible with OKI's synthesis IC MSM5205
- Analysis/synthesis switching pin provided
- Lower power consumption achieved by one-chip CMOS IC
- Built-in 10-bit D/A converter for analog output
- Variable sampling frequency (4 kHz, 6 kHz, 8 kHz)
- Master clock frequency: 384 kHz
- Package: 24-pin plastic DIP (DIP24-P-600) (Product name: MSM5218RS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



24-Pin Plastic DIP

Note: The product name actually printed on the product is "M5218".

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−3.0 to +7.0	V
Input Voltage	V_{IN}	Ta = 25°C	−3.0 to V_{DD}	V
Power Dissipation	P_D	Ta = 25°C	200 max	mW
Storage Temperature	T_{STG}	—	−55 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	—	+3 to +6	V
Operating Temperature	T_{OP}	—	−30 to +70	°C
Oscillator Frequency	f_{OSC}	Specified Oscillator	386 to 768	kHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

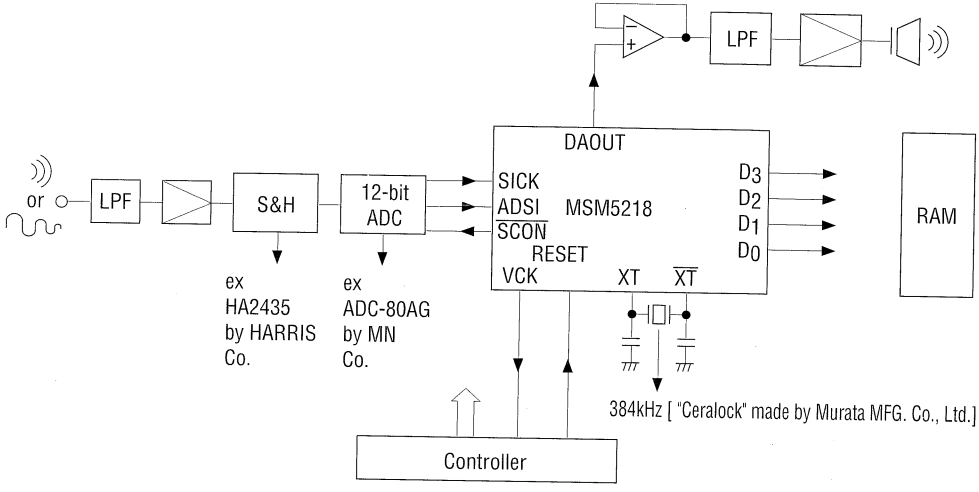
(V_{DD} = 5V±5%, Ta = −30°C to +70°C, Ta =25°C typically)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All inputs except XT, T_1, T_2	4.2	—	—	V
Input Low Voltage	V_{IL}	All inputs except XT, T_1, T_2	—	—	0.8	V
Input High Current (1)	I_{IH}	V_{IN} = V_{DD}	—	—	1	µA
Input Low Current	I_{IL}	V_{IN} = 0V	—	—	−1	µA
Output High Current	I_{OH}	$\overline{SCON}$, VCK, SOCK, MSB/$\overline{SO}$, D0 to D3 V_0 = 4.2V	−50	—	—	µA
Output Low Current	I_{OL}	$\overline{SCON}$, VCK, SOCK, MSB/$\overline{SO}$, D0 to D3 V_0 = 0.4V	50	—	—	µA
Operating Current	I_{DD}	f_{VCK} = 8kHz	—	3	6	mA
DA. OUT Output Impedance	V_{OR}	—	—	100	—	kΩ
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale V_{DD} = +5V	—	±4	—	LSB
SICK Clock Frequency	$f_{(SICK)}$	—	—	—	500	kHz
Input High Current (2)	I_{IH2}	V_{IN} = V_{DD} (Note 1)	20	—	400	µA

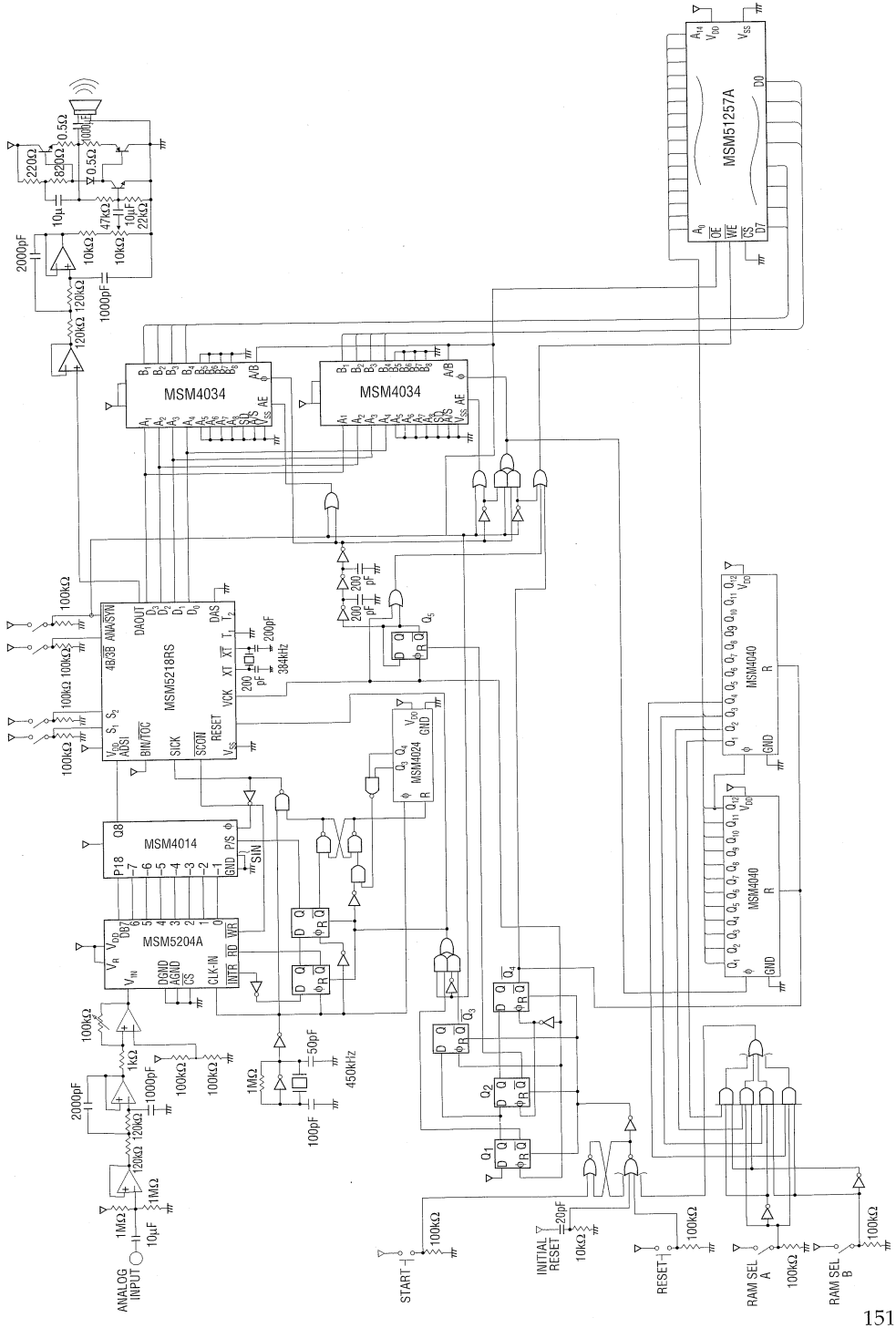
Note 1: Applicable for Reset.

APPLICATION CIRCUITS

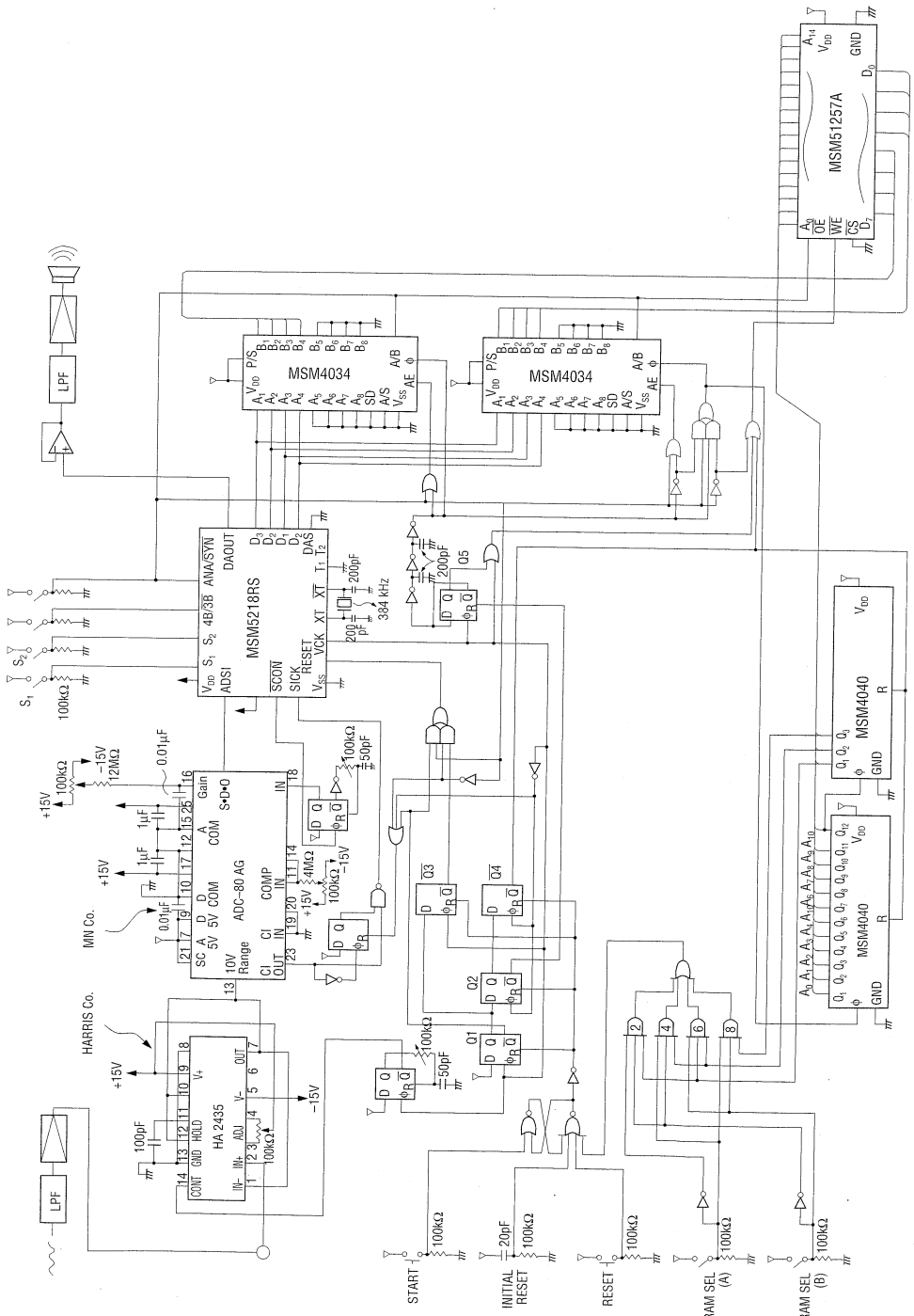
Example where a 12-bit AD Converter is Connected



Voice Analysis/Synthesis Circuit Example (When MSM5204 is Used)



Voice Analysis/Synthesis Circuit Example (When ADC-80AG by MN Co. is Used)



OKI Semiconductor

MSM6588/6588L

ADPCM Solid-State Recorder (for Serial Registers)

GENERAL DESCRIPTION

The MSM6588/6588L is a "solid-state recorder" IC developed using the ADPCM method. By externally connecting a microphone, a speaker, a speaker amplifier and a serial register or other Memory device to store ADPCM data, it can record and playback voice data similar to a tape recorder.

The MSM6588/6588L has a stand-alone mode and a microcontroller interface mode. In stand-alone mode, record/playback can be selected from a pin and it is possible to control the MSM6588 by a simple drive timing. In microcontroller interface mode, record/playback can be controlled by commands from the microcontroller in microcontroller mode, the MSM6588/6588L is much more flexible than in stand-alone operation. In addition, recording and playback with fixed message are easily implemented by connecting a serial voice ROM.

The MSM6588 and the MSM6588L support 5 V and 3 V operation respectively.

FEATURES

- 12bit A/D converter
- 12bit D/A converter
- Microphone amplifier
- Low-pass filter (LPF)
  Filter characteristics –40 dB/oct
- Serial registers
  MSM6588
  Up to four 1Mbit serial registers (MSM6685) can be driven directly
  One 512Kbit serial register (MSM6587) can be driven directly
  One 256Kbit serial register (MSM6586) can be driven directly
  MSM6588
  Up to four 1Mbit serial registers (MSM63V89C) can be driven directly
- Serial Voice ROMs
  1Mbit serial voice ROM (MSM6595A-xxx)
  2Mbit serial voice ROM (MSM6596A-xxx)
  3Mbit serial voice ROM (MSM6597A-xxx)
- Maximum recording time
  262 seconds (when using 3-bit ADPCM, 5.3 kHz sampling)
- Voice triggered starting
- Pause function
- Master clock frequency: 4.096 MHz to 8.192 MHz
- Power supply voltage
  MSM6588: Single 5 V Power supply
  MSM6588L: Single 3 V Power supply
- Package options:
  MSM6588: 44-pin plastic QFP (QFP44-P-910-2K)(Product name: MSM6588GS-2K)
  MSM6588L: 44-pin plastic QFP (QFP44-P-910-2K)(Product name: MSM6588LGS-2K)

• Differences between MSM6588 and MSM6588L

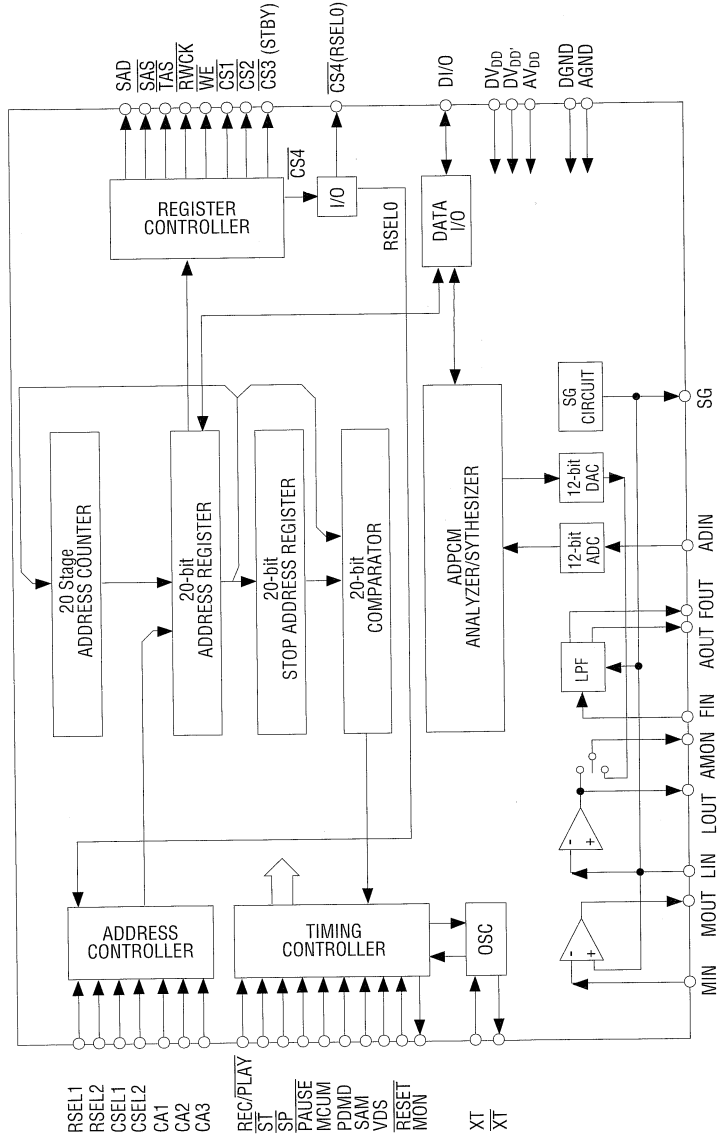
The major differences between the MSM6588 and the MSM6588L are shown below.

Parameter	MSM6588	MSM6588L
Operating voltage	3.5 to 5.5V	2.7 to 3.6V
Full scale of A/D and D/A converters	0 to V_{DD}	$\frac{1}{4}V_{DD}$ to $\frac{3}{4}V_{DD}$
Voice detection level for voice triggered starting	$\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$, $\pm\frac{V_{DD}}{16}$	$\pm\frac{V_{DD}}{128}$, $\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$
External only register	1Mbits (MSM6389C) 512Kbits (MSM6587) 256Kbits (MSM6586)	1Mbits (MSM63V89C)

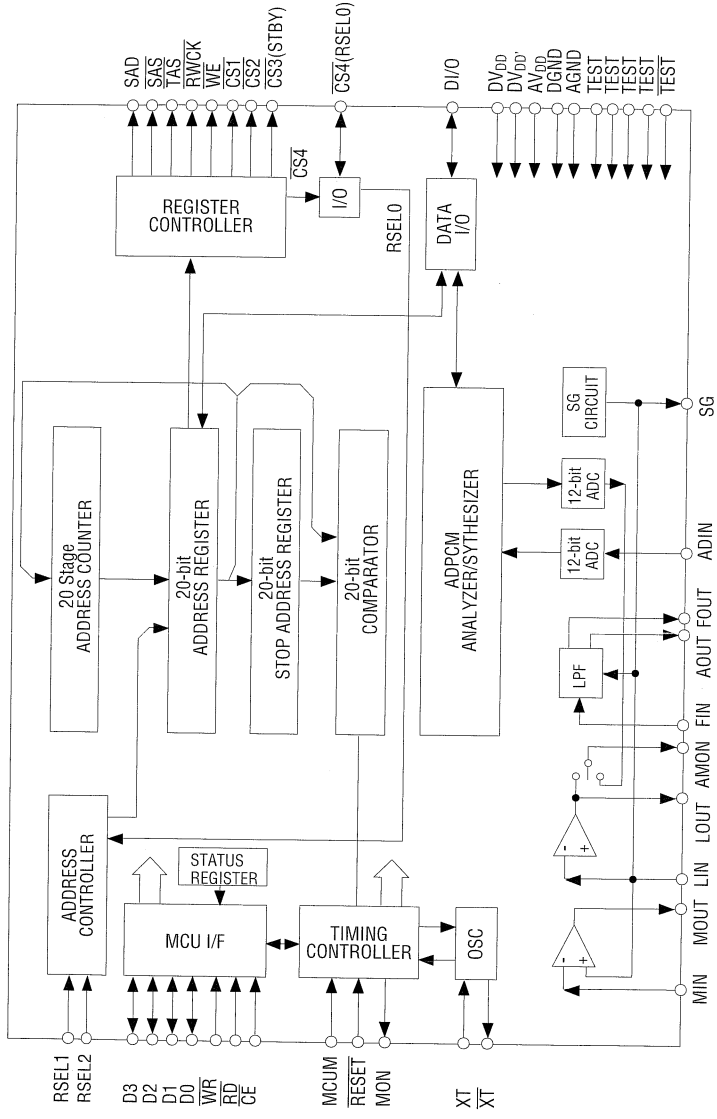
1. Characteristics in stand-alone mode
• 3-bit ADPCM
•Sampling frequency:
5.3 kHz or 8.0 kHz (when the oscillator operates at 4.096 MHz)
10.6 kHz or 16.0 kHz (when the oscillator operates at 8.192 MHz)
• Number of phrases: 1, 2, 4 or 8
2. Characteristics in microcontroller interface mode
• 3-bit/4-bit ADPCM selectable
• Sampling frequency:
4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz (when the oscillator operates at 4.096 MHz)
8.0 kHz, 10.6 kHz, 12.8 kHz or 16.0 kHz (when the oscillator operates at 8.192 MHz)
• Condition setting, start, and stop of record/playback controllable by 13 commands.

BLOCK DIAGRAM

Stand-Alone Mode

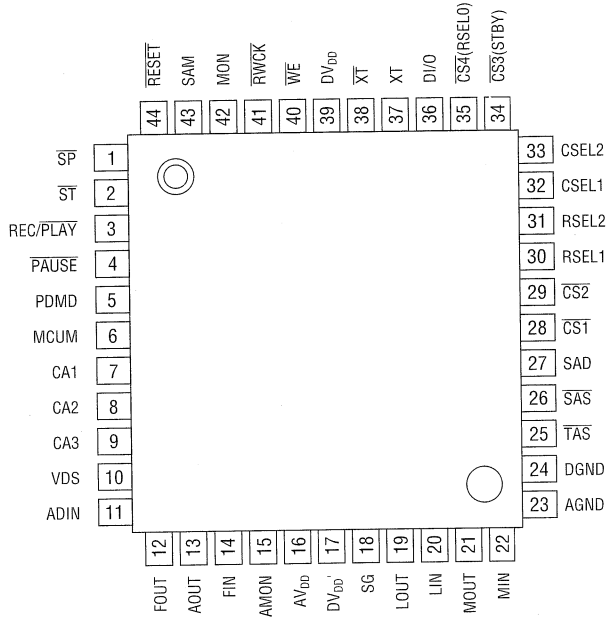


Microcontroller Interface Mode



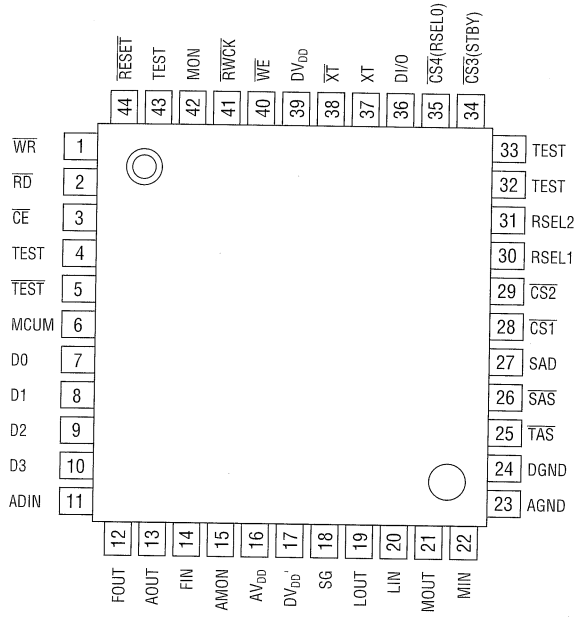
PIN CONFIGURAITON (Top View)

1. Stand-alone mode (MCUM pin = "L")



44-Pin Plastic QFP

2. Microcontroller interface mode (MCUM pin = "H")



44-Pin Plastic QFP

Selection of stand-alone mode or microcontroller interface mode is controlled by the level of the MCUM pin.

MCUM="H": microcontroller interface mode
MCUM="L": stand-alone mode

PIN DESCRIPTIONS

Common Functions in Stand-Alone Mode and Microcontroller Interface Mode

Symbol	Type	Description
DV_{DD}	—	Digital power supply pin. Insert a bypass capacitor of 0.1µF or more between this pin and the DGND pin.
DV_{DD}'	—	Digital power supply pin
AV_{DD}	—	Analog power supply pin. Insert a bypass capacitor of 0.1µF or more between this pin and the AGND pin.
DGND	—	Digital GND pin
AGND	—	Analog GND pin
SG	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	I	Inverting input pin for the built-in OP amplifier. Non-inverting input pin is connected to SG internally.
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in recording mode and to the DA converter output in playing mode. Connected to the built-in LPF input (FIN pin).
FIN	I	Input pin for the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Connected to the AD converter (ADIN pin) input.
ADIN	I	Input pin for the built-in 12-bit AD converter.
AOUT	O	Output pin for the built-in LPF. Output pin for playback waveform. Connected to the speaker drive amplifier.
SAD	O	(Serial Address Data) Connected to the SAD pin of serial register. This pin outputs the Read/Write header address.
$\overline{SAS}$	O	(Serial Address Strobe) Connected to the $\overline{SAS}$ pin of serial register. Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe) Connecd to the $\overline{TAS}$ pin of serial register. Clock pin which tranfers the serial address data to the address counter inside the serial register.

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>$\overline{RWCK}$</td><td>O</td><td>(Read/Write Clock) Connected to the $\overline{RWCK}$ pin of the serial register. Clock pin for reading and writing data to the serial registers.</td></tr>
<tr><td>$\overline{WE}$</td><td>O</td><td>(Write Enable) Connected to the $\overline{WE}$ pin of serial register. The pin to select read or write mode.</td></tr>
<tr><td>DI/O</td><td>I/O</td><td>(Data I/O) Connected to the DIN and DOUT pins of serial register. Data input and output mode.</td></tr>
<tr><td>$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$ (STBY)
$\overline{CS4}$ (RSEL0)</td><td>O
O
O
I/O</td><td>(Chip Select) Connected to the $\overline{CS}$ pin of the serial register.
$\overline{CS3}$ pin and $\overline{CS4}$ pin have different functions depending on the number of serial registers to be connected. The number of serial registers is selected by the RSEL1 and RSEL2 pins.
$\overline{CS3}$ (STBY) pin becomes $\overline{CS3}$ when four serial registers are used\, otherwise it is the STBY pin which outputs a "H" level at power down.
$\overline{CS4}$ (RSEL0) pin becomes $\overline{CS4}$ when four serial registers are used, otherwise it is the RSEL0-pin used to select the number of serial registers used.
<table><tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr><tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>$\overline{CS3}$ (STBY)</td><td>STBY</td><td>STBY</td><td>STBY</td><td>$\overline{CS3}$</td></tr><tr><td>$\overline{CS4}$ (RSEL0)</td><td>RSEL0 (I)</td><td>RSEL0 (I)</td><td>RSEL0 (I)</td><td>$\overline{CS4}$ (O)</td></tr></table></td></tr>
<tr><td>$\overline{CS4}$ (RSEL0)
RSEL1
RSEL2</td><td>I/O
I
I</td><td>(Register Select) Those pins are to select the number of serial registers to be connected.
<table><tr><td>RSEL2</td><td colspan="2">L</td><td>L</td><td>H</td><td>H</td></tr><tr><td>RSEL1</td><td colspan="2">L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>RSEL0 (CS4)</td><td>L (I)</td><td>H (I)</td><td>— (I)</td><td>— (I)</td><td>$\overline{CS4}$ (O)</td></tr><tr><td>Number of serial voice registers</td><td>One 256Kbit</td><td>One 512Kbit</td><td>One 1Mbit</td><td>Two 1Mbit</td><td>Four 1Mbit</td></tr></table></td></tr>
<tr><td>MCUM</td><td>I</td><td>This pin is to select stand-alone mode or microcontroller interface mode.
"L" level···· stand-alone mode
"H" level···· microcontroller interface mode</td></tr>
<tr><td>$\overline{RESET}$</td><td>I</td><td>The IC is initialized and goes into the power-down state by input of a "L" level.</td></tr>
<tr><td>XT</td><td>I</td><td>Connect to an oscillator. Use this input when providing an external clock. When at power down input the GND level instead.</td></tr>
<tr><td>$\overline{XT}$</td><td>O</td><td>Connect to an oscillator. Leave open when using an external clock.</td></tr>
</table>

Stand-Alone Mode

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>REC/$\overline{PLAY}$</td><td>I</td><td>This pin is to select recording or playback. When an "H" level is input, the IC is in record mode.</td></tr>
<tr><td>$\overline{ST}$</td><td>I</td><td>When an "L" level pulse is input, record/playback is started. Internal pull up connected.</td></tr>
<tr><td>$\overline{SP}$</td><td>I</td><td>When an "L" level pulse is input, record/playback is ended. Internal pull up connected.</td></tr>
<tr><td>$\overline{PAUSE}$</td><td>I</td><td>When an "L" level pulse is input, record/playback is suspended. Internal pull up connected.</td></tr>
<tr><td>CSEL1
CSEL2</td><td>I</td><td>These pins are to select the number of recorded words and control mode. When the number of the recorded words is wished to be selected in one word, select Flex mode.
<table>
<tr><td>CSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>CSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Number of recorded words</td><td>8</td><td>4</td><td>2</td><td>8</td></tr>
<tr><td>Control mode</td><td colspan="3">fixed</td><td>flex</td></tr>
</table></td></tr>
<tr><td>CA1
CA2
CA3</td><td>I</td><td>These pins are to specify the channel.
(Refer to Explanation of Functions.)</td></tr>
<tr><td>SAM</td><td>I</td><td>This pin is to select the sampling frequency.
The following is the relation between the master clock frequency (f_{OSC}) and sampling frequency (fsam).

Numbers inside the parenthenses ( ) are for f_{OSC}=4.096MHz
<table>
<tr><td>SAM</td><td>L</td><td>H</td></tr>
<tr><td>fsam</td><td>$\frac{fsamp}{768}$
(5.3kHz)</td><td>$\frac{fosc}{512}$
(8.0kHz)</td></tr>
</table></td></tr>
<tr><td>PDMD</td><td>I</td><td>This pin selects transition to the power down state.
"L" level···· The IC enters power down state automatically except during record/playback.
"H" level···· The IC enters standby state except during record/playback.
The power down state can be entered by the $\overline{RESET}$ pin. This mode must be active when using the built-in LPF in an external circuit.</td></tr>
</table>

Symbol	Type	Description
VDS	I	This pin is to select voice triggered starting that starts recording when the voice input exceeds the preset amplitude. Input an "H" level and the voice activation circuit is enabled. Input an "L" level to disabel the voice activation circuit.
MON	O	Outputs a "H" level during record/playback.

Microcontroller Interface Mode

Symbol	Type	Description
D0 D1 D2 D3	I/O	Bi-directional data bus. Performs input/output of commands and data with an external microcontroller.
$\overline{WR}$	I	This pin is to input WRITE pulses. Input is a "L" pulse when commands or data to the D0~D3 pins are to be input.
$\overline{RD}$	I	This pin is to input READ pulses. Input is a "L" pulse when output status or data from the D0~D3 pins is to read.
$\overline{CE}$	I	Chip enable. A "H" level on this pin disables WRITE (WR)/READ ($\overline{RD}$) input pulses. Input/output of data through the D0~D3 pins is disabled.
MON	O	Outputs a "H" level during record/playback. When record/playback is in operation using the EXT command, clocks for synchronization are output.
TEST $\overline{TEST}$	I	These pins are for IC testing at the factory. Input a "L" level to the TEST pin and an "H" level to the $\overline{TEST}$ pin.

ABSOLUTE MAXIMUM RATINGS (for MSM6588 (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6588 (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	Ta = 25°C	+3.5 to +5.5 (Note 5)	V
Operating temperature	T_{STG}	—	−40 to +85	°C
Master clock frequency	f_{OSC}	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6588 (5 V Version))

DC Characteristics

$DV_{DD}=DV_{DD}'=AV_{DD}$=4.5 to 5.5 V (Note 5), DGND=AGND=0 V, Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8×V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.2×V_{DD}	V
"H" output voltage	V_{OH}	I_{OH} = –40μA	V_{DD}–0.3	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
"H" input current (Note 1)	I_{IH1}	V_{IN} = V_{DD}	—	—	10	μA
"H" input current (Note 2)	I_{IH2}	V_{IN} = V_{DD}	—	—	20	μA
"L" input current (Note 3)	I_{IL1}	V_{IL} = GND	–10	—	—	μA
"L" input current (Note 2)	I_{IL2}	V_{IL} = GND	–20	—	—	μA
"L" input current (Note 4)	I_{IL3}	V_{IL} = GND	–400	—	–20	μA
Operating current consumption	I_{DD}	f_{OSC} = 8MHz, no load	—	7	15	mA
Stand by current consumption	I_{DDS}	When power down, no load Ta = –40 to +70°C	—	—	10	μA
		When power down, no load Ta = +70 to +85°C	—	—	50	μA

Note:
1. Applicable to all input pins, excluding the XT pin.
2. Applicable to the XT pin.
3. Applicable to all input pins without pull-up resistors, excluding the XT pin.
4. Applicable to input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$) with pull-up resistors, excluding the XT pin.
5. Recording and playback should be performed at a power supply voltage of 4.5 to 5.5 V. For other operations such as backing up a serial register, the IC operates at 3.5 to 5.5 V.

Analog Characteristics

$DV_{DD}=DV_{DD}'=AV_{DD}$=4.5 to 5.5 V, DGND=AGND=0 V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	V_{DD}–1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	V_{DD}	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN} = 0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50		—	kΩ
FOUT load resistance	R_{FOUT}	—	50		—	kΩ

ABSOLUTE MAXIMUM RATINGS (for MSM6588L (3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6588L (3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	Ta = 25°C	+2.7 to +3.6	V
Operating temperature	T_{STG}	—	−40 to +85	°C
Master clock frequency	f_{OSC}	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6588L (3 V Version))

DC Characteristics

$DV_{DD}=DV_{DD}'=AV_{DD}$=2.7 to 3.6 V, DGND=AGND=0 V, Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.85×V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.15×V_{DD}	V
"H" output voltage	V_{OH}	I_{OH} = –40µA	V_{DD}–0.3	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
"H" input current (Note 1)	I_{IH1}	V_{IN} = V_{DD}	—	—	10	µA
"H" input current (Note 2)	I_{IH2}	V_{IN} = V_{DD}	—	—	20	µA
"L" input current (Note 3)	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current (Note 2)	I_{IL2}	V_{IL} = GND	–20	—	—	µA
"L" input current (Note 4)	I_{IL3}	V_{IL} = GND	–400	—	–10	µA
Operating current consumption	I_{DD}	f_{OSC} = 8MHz, no load	—	7	15	mA
Stand by current consumption	I_{DDS}	When power down, no load Ta = –40 to +70°C	—	—	15	µA
		When power down, no load Ta = +70 to +85°C	—	—	100	µA

Note: 1. Applicable to all input pins, excluding the XT pin.
2. Applicable to the XT pin.
3. Applicable to all input pins without pull-up resistors, excluding the XT pin.
4. Applicable to input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$) with pull-up resistors, excluding the XT pin.

Analog Characteristics

$DV_{DD}=DV_{DD}'=AV_{DD}$=2.7 to 3.6 V, DGND=AGND=0 V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	5	mV
FIN admissible input voltage range	V_{FIN}	—	1/4×V_{DD}	—	3/4×V_{DD}	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	1/4×V_{DD}	—	3/4×V_{DD}	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN} = 0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

APPLICATION CIRCUITS

Figure 1 shows an application circuit when the MSM6588/6588L is used in stand-alone mode and four 1Mbit serial registers are used.
Figure 2 shows an application circuit when the MSM6588/6588L is used in microcontroller interface mode with two 1Mbit serial registers and one 2Mbit serial voice ROM.
Figure 3 shows an example of application circuit when record/playback is made using the EXT command for MSM6588/6588L.

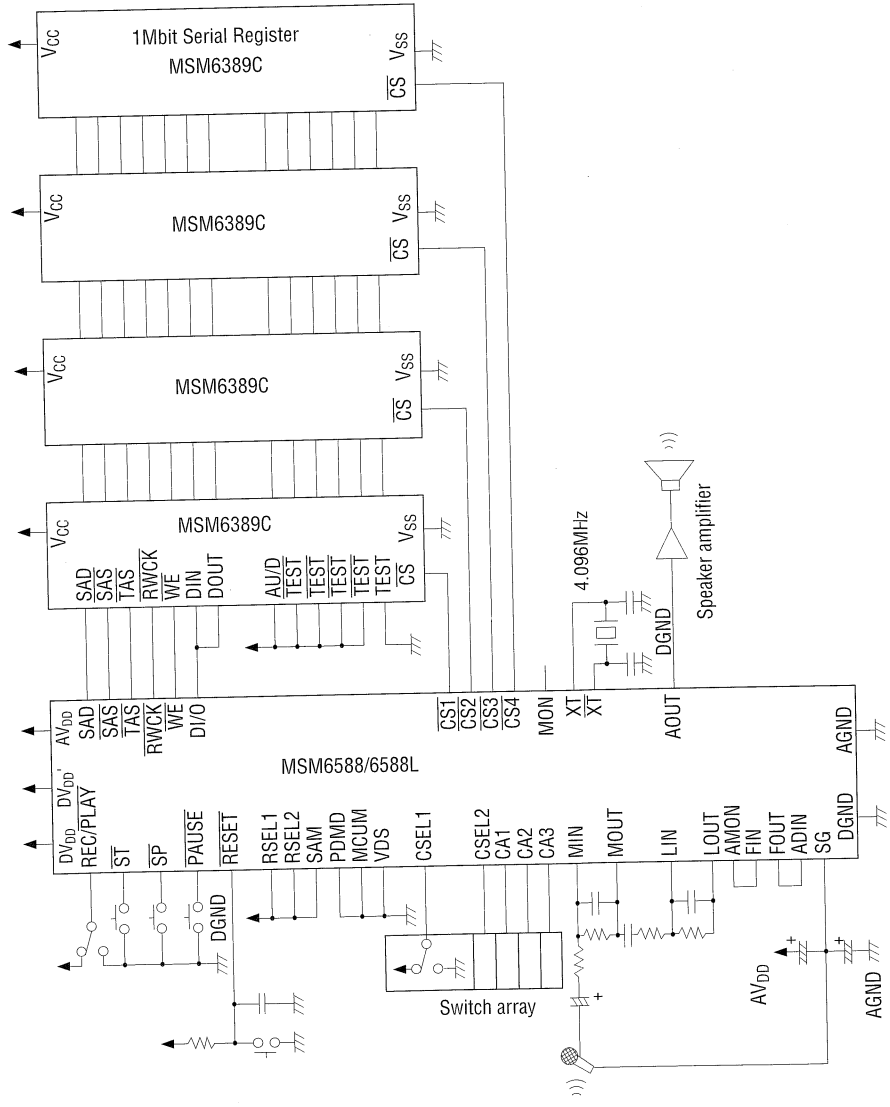


FIgure 1 Example of Application Circuit in Stand-alone Mode with 1Mbit Serial Registers

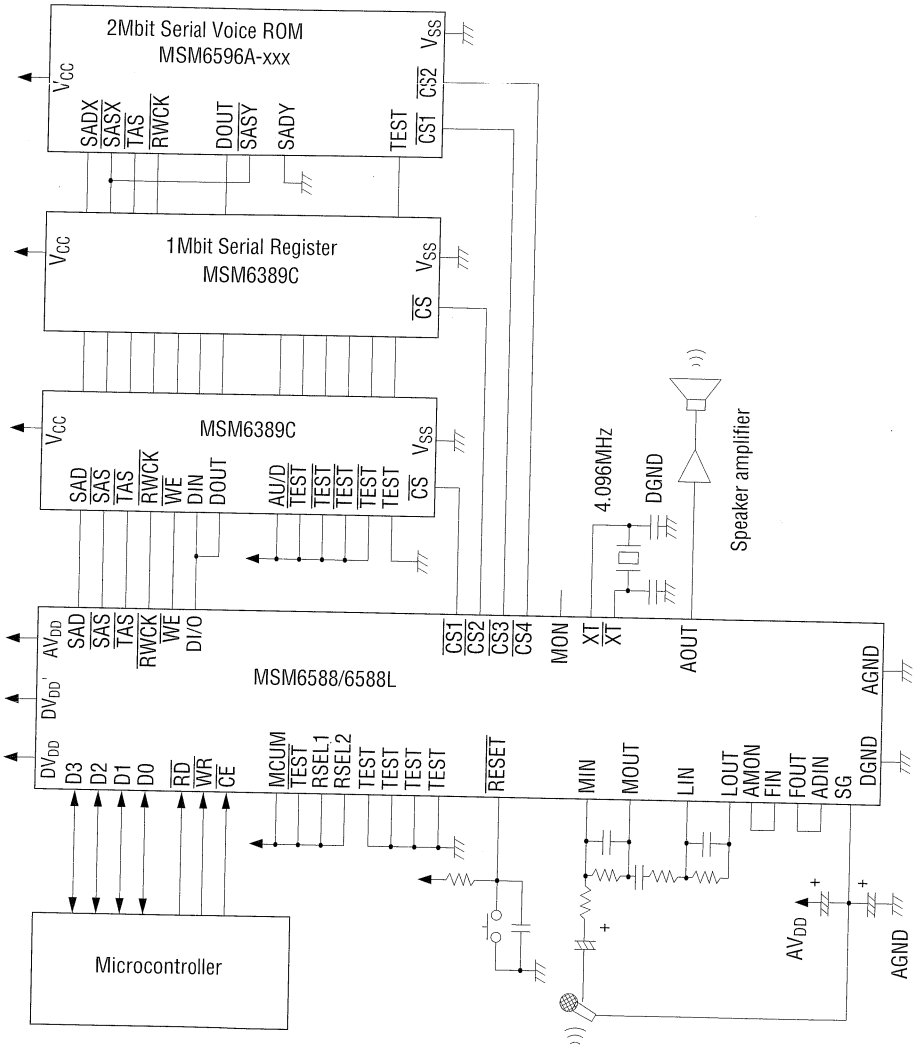


Figure 2 Example of Application Circuit in Microcontroller Interface Mode with 1Mbit Serial Registers and 2Mbit Serial Voice ROM

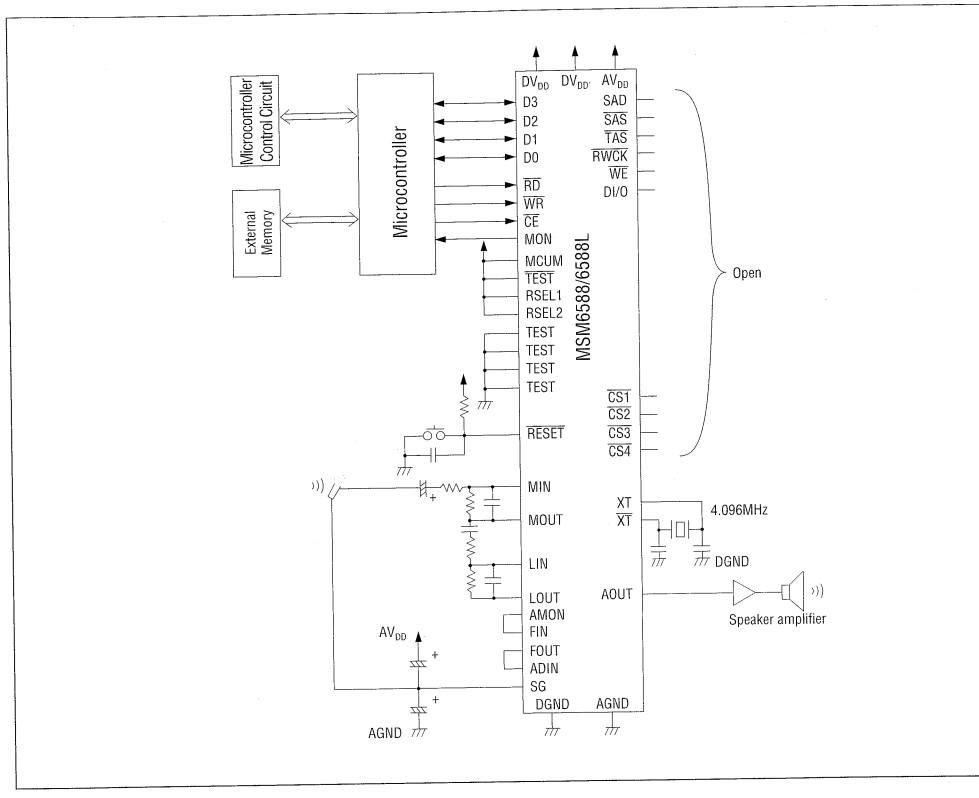


Figure 3 Application Circuit When Record/Playback is Mode Using EXT Command

MSM6688/6688L

ADPCM Solid-State Recorder IC

GENERAL DESCRIPTION

The MSM6688/6688L is a "solid-state recorder" IC developed using the ADPCM method. By externally connecting a microphone, a speaker, a speaker drive amplifier, and a dedicated register to store ADPCM data, it can record and play back voice data in a manner similar to a tape recorder.
The MSM6688 supports 5 V operation and has a stand-alone mode and a microcontroller interface mode.
The MSM6688L supports 3 V operation and controls record/playback in microcontroller interface mode.
In the stand-alone mode, record/playback conditions can be selected from pins and the MSM6688/6688L can be controlled by a simple drive timing. In the microcontroller interface mode, record/playback can be controlled by commands from the microcontroller. In the microcontroller interface mode, the MSM6688/6688L is much more flexible than in the stand-alone mode.
In addition, the MSM6688/6688L can form easily a recording and playback circuit with fixed messages by connecting serial registers and serial voice ROMs as external memories.

Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

Difference Between MSM6688 and MSM6688L

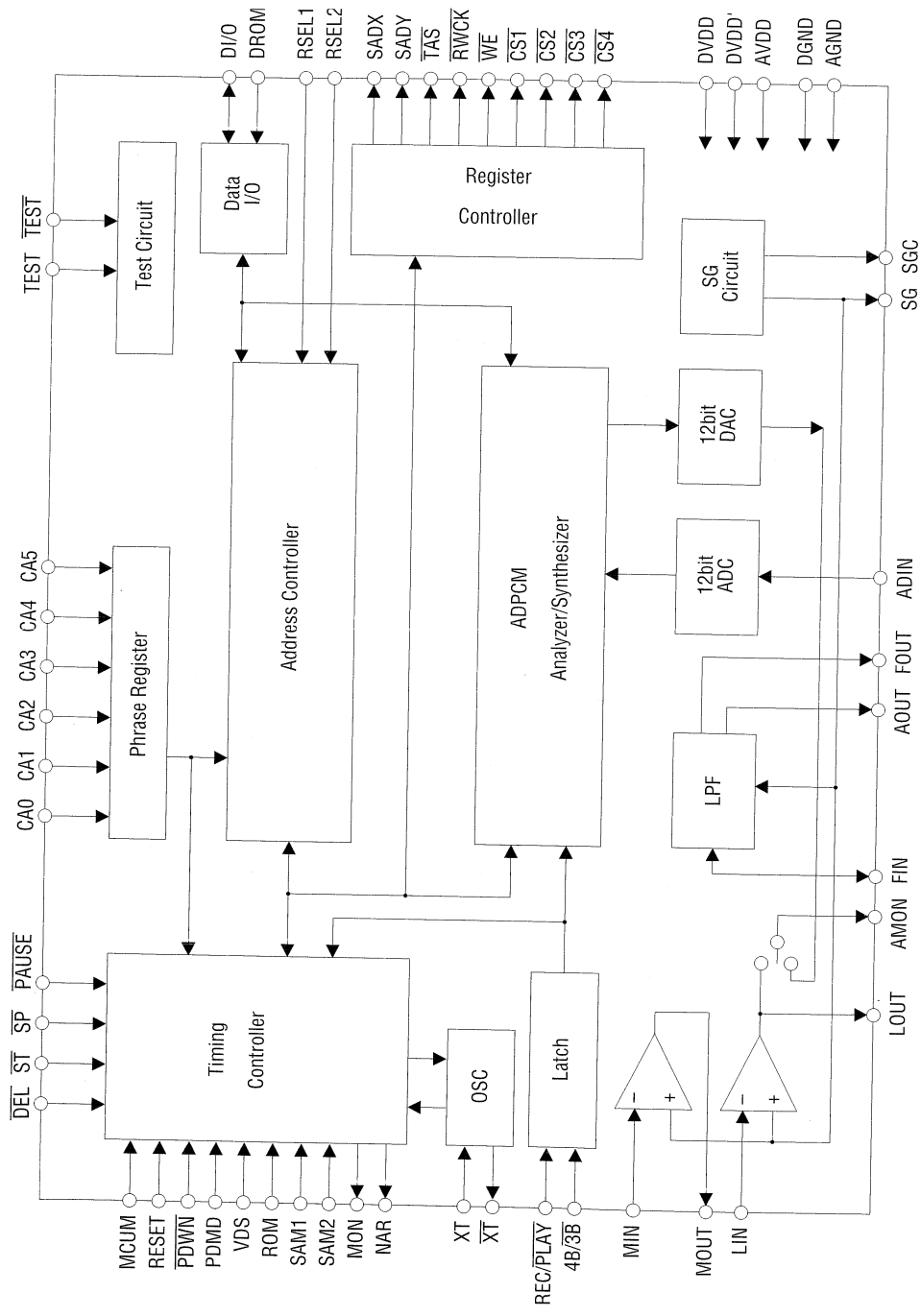
Parameter	MSM6688	MSM6688L
Operating voltage	3.5 to 5.5 V	2.7 to 3.6 V
Control mode	Standalone mode, Microcontroller interface mode	Microcontroller interface mode only
Full scale of A/D and D/A converters	0 to V_{DD}	$\frac{1}{4}$ V_{DD} to $\frac{3}{4}$ V_{DD}
Voice detection level for voice triggered starting	$\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$, $\pm\frac{V_{DD}}{16}$	$\pm\frac{V_{DD}}{128}$, $\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$
External only register	32M bits (max.) 4M bits (MSM6684B) 8M bits (MSM6685)	4M bits (max.) 4M bits (MSM66V84B)

(1) STAND-ALONE MODE (for MSM6688 (5 V Version))

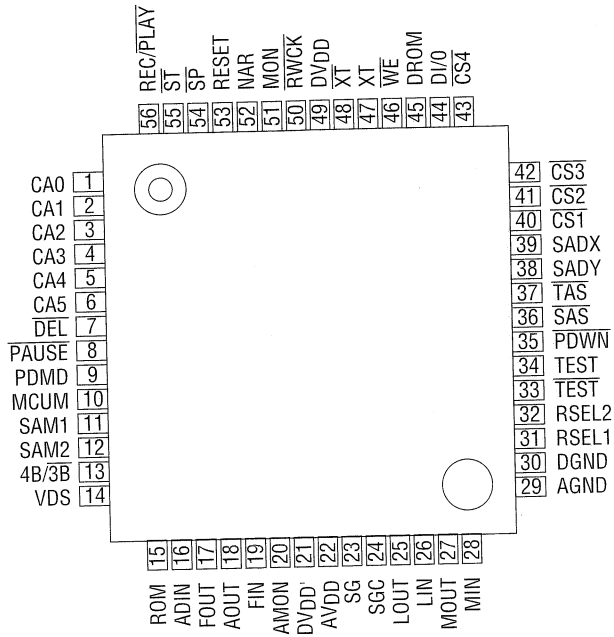
FEATURES

- 3-bit or 4-bit ADPCM
- Built-in 12-bit AD converter
- Built-in12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  Serial registers, 32M bits maximum (for variable messages)
  8M bit serial register (MSM6685) can be driven directly
  Serial voice ROMs, 4M bits maximum (for fixed messages)
  1M bit serial voice ROM (MSM6595A) can be driven directly
  2M bit serial voice ROM (MSM6596A) can be driven directly
  3M bit serial voice ROM (MSM6597A) can be driven directly
- Sampling frequency
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz (master clock frequency = 4.096 MHz)
  8.0 kHz, 10.6 kHz, 12.8 kHz, or 16.0 kHz (master clock frequency = 8.192 MHz)
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Maximum recording time (when external 32M bit RAM is connected)
  34 minutes (for 16 kbps ADPCM)
  23 minutes (for 24 kbps ADPCM)
  17 minutes (for 32 kbps ADPCM)
- Voice triggered starting function
- Pause function
- Master clock frequency: 4.096 MHz~8.192 MHz
- Power supply voltage: Single 5 V power supply
- Package options:
  MSM6688: 56-pin plastic QFP (QFP56-P-910-2K) (Product name: MSM6688GS-2K)
  MSM6688L: 56-pin plastic QFP (QFP56-P-910-2K) (Product name: MSM6688LGS-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



56-Pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description
DVDD	I	Digital power supply pin. Insert a bypass capacitor of 0.1µF or more between this pin and the DGND pin.
DVDD'	I	Digital power supply pin
AVDD	I	Analog power supply pin. Insert a bypass capacitor of 0.1µF or more between this pin and the AGND pin.
DGND	I	Digital ground pin
AGND	I	Analog ground pin
SG, SGC	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	I	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
FIN	I	Input pin of the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin).
ADIN	I	Input pin of the built-in 12-bit AD converter.
AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
SADX SADY	O	(Serial Address Data). SADX is used to connect the SAD pin of each external serial register and the SADX pin of each external serial voice ROM. SADY is used to connect the SADY pin of each external serial voice ROM. Outputs of starting address of read/write.
$\overline{SAS}$	O	(Serial Address Strobe). Used to connect the $\overline{SAS}$ pin of external serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of external serial voice ROM. Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe). Used to connect the $\overline{TAS}$ pin of each external serial register and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each serial register and serial voice ROM.
$\overline{RWCK}$	O	(Read/Write Clock). Used to connect the $\overline{RWCK}$ pin of each external serial register and the $\overline{RDCK}$ pin of each external serial voice ROM. This pin outputs a clock to read data from or write it into each external serial register.
$\overline{WE}$	O	(Write Enable) Used to connect the $\overline{WE}$ pin of each external serial register. This pin outputs $\overline{WE}$ signal to select either read or write mode.
DI/O	I/O	(Data I/O). Used to connect the DIN and DOUT pins of serial register. This pin outputs the data to be written into the serial register or inputs the data read from the serial registers.
DROM	I	(Data ROM). Used to connect the DOUT pin of each external serial voic ROM.
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O O O O	(Chip Select). Used to connect the $\overline{CS}$ pin of serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of serial voice ROM.

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>RSEL1
RSEL2</td><td>I
I</td><td>(Register Select). These are used to select the number of external serial registers.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Number of serial registers</td><td>1</td><td>2</td><td>3</td><td>4</td></tr>
</table></td></tr>
<tr><td>MCUM</td><td>I</td><td>This pin is used to select either the stand-alone mode or the microcontroller interface mode.
Low level: Stand-alone mode
High level: Microcontroller interface mode.</td></tr>
<tr><td>RESET</td><td>I</td><td>A high input level to this pin causes the MSM6688 to be initialized and to go into the power down state.</td></tr>
<tr><td>$\overline{\text{PDWN}}$</td><td>I</td><td>(Power Down). When a low level is input to this pin, the MSM6688 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6688. When an Low level is applied to this $\overline{\text{PDWN}}$ pin during recording operation, the MSM6688 is halted, and will be maintained in the power down state while PDWN is low. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>XT</td><td>I</td><td>Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>$\overline{\text{XT}}$</td><td>O</td><td>Used to connect an oscillator, when an external clock is used, this pin must be left open.</td></tr>
<tr><td>TEST
$\overline{\text{TEST}}$</td><td>I</td><td>Used to test the MSM6688. Input a low level to the TEST pin and a high level to the $\overline{\text{TEST}}$ pin.</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>ROM</td><td>I</td><td>When low, selects the record/playback operation. When high, selects the ROM playback operation.</td></tr>
<tr><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Used to select the recording mode or the playback mode. This pin is invalid during the ROM playback operation. When low, selects the playback mode. When high, selects the recording mode.</td></tr>
<tr><td>$\overline{\text{ST}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>$\overline{\text{SP}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>$\overline{\text{DEL}}$</td><td>I</td><td>When a low level pulse is applied to this pin, all phase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00: All phase deletion
ch01~ch3F: Specified phrase deletion
After powering up, be sure to input RESET signal and then to delete all phrases.
After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>CA0~CA5</td><td>I</td><td>Input pins used to specify desired phases.
A total of 63 phrases can be specified independently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="6">A total of 63 phrases can be used both for record/playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table></td></tr>
<tr><td>4B/$\overline{\text{3B}}$</td><td>I</td><td>Input pin used to select one of two types of ADPCM bit length.
When low, selects the 3-bit ADPCM.
When high, selects the 4-bit ADPCM.</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>SAM1
SAM2</td><td>I</td><td>Used to select one of the following four types of sampling frequency. The relationship between the master clock frequency (fosc) and the sampling frequency (fsamp) is shown below. Values in parentheses denote the sampling frequencies for fosc = 4.096 MHz.
<table>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>fsam</td><td>$\frac{fosc}{1024}$ (4.0kHz)</td><td>$\frac{fosc}{768}$ (5.3kHz)</td><td>$\frac{fosc}{640}$ (6.4kHz)</td><td>$\frac{fosc}{512}$ (8.0kHz)</td></tr>
</table></td></tr>
<tr><td>PDMD</td><td>I</td><td>This input pin is used to select the condition for transition to the power-down state.
Low level: The MSM6688 automatically goes to the power-down state, excepting the time the record/playback operation is being performed.
High level: The MSM6688 automatically goes to the standby state, instead of the power-down state, excepting the time the record/playback operation is being performed. In this case, the MSM6688 can be placed in the power-down state by setting the RESET pin to a high level. If it is desired to use the built-in LPF for an external circuit, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>VDS</td><td>I</td><td>Used to select the voice triggered starting that starts recording when the voice input exceeds the preset amplitude. A high input level on this pin enables the voice triggered starting circuit.</td></tr>
<tr><td>MON</td><td>O</td><td>Outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>NAR</td><td>O</td><td>Output pin to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after verifying that the NAR pin becomes high.</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	VDD	Ta=25°C	−0.3 to+7.0	V
Input Voltage	V_{IN}	Ta=25°C	−0.3 to VDD+0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	VDD	DGND=AGND=0V	+3.5 to 5.5 (Note 5)	V
Operating temperature	T_{op}	—	−40 to +85	°C
Master clock frequency	fosc	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6688 (5 V Version))

DC Characteristics

DVDD=DVDD'=AVDD=4.5 to 5.5V (Note 5)
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
High input voltage	V_{IH}	—	0.8×VDD	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×VDD	V
High output voltage	V_{OH}	I_{OH} = –40uA	VDD–0.3	—	—	V
Low output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
High input current (Note 1)	I_{IH1}	V_{IH} = VDD	—	—	10	µA
High input current (Note 2)	I_{IH2}	V_{IH} = VDD	—	—	20	µA
Low input current (Note 3)	I_{IL1}	V_{IL} = GND	–10	—	—	µA
Low input current (Note 2)	I_{IL2}	V_{IL} = GND	–20	—	—	µA
Low input current (Note 4)	I_{IL3}	V_{IL} = GND	–400	—	–20	µA
Operating current consumption	I_{DD}	fosc = 8 MHz, no load	—	15	30	mA
Standby current consumption	I_{DDS}	During power down, no load Ta=–40 to +70°C	—	—	10	µA
		During power down, no load Ta=+70 to +85°C	—	—	50	µA

Note:
1. Applies to all input pins excluding the XT pin.
2. Applies to the XT pin.
3. Applies to the all input pins without pull-up resistors, excluding the XT pin.
4. Applies to the input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, $\overline{DEL}$) with pull-up resistors, excluding the XT pin.
5. Recording and playback should be performed at a power supply voltage of 4.5 to 5.5V. For other operations such as backup for a serial register, the IC operates at 3.5 to 5.5V.

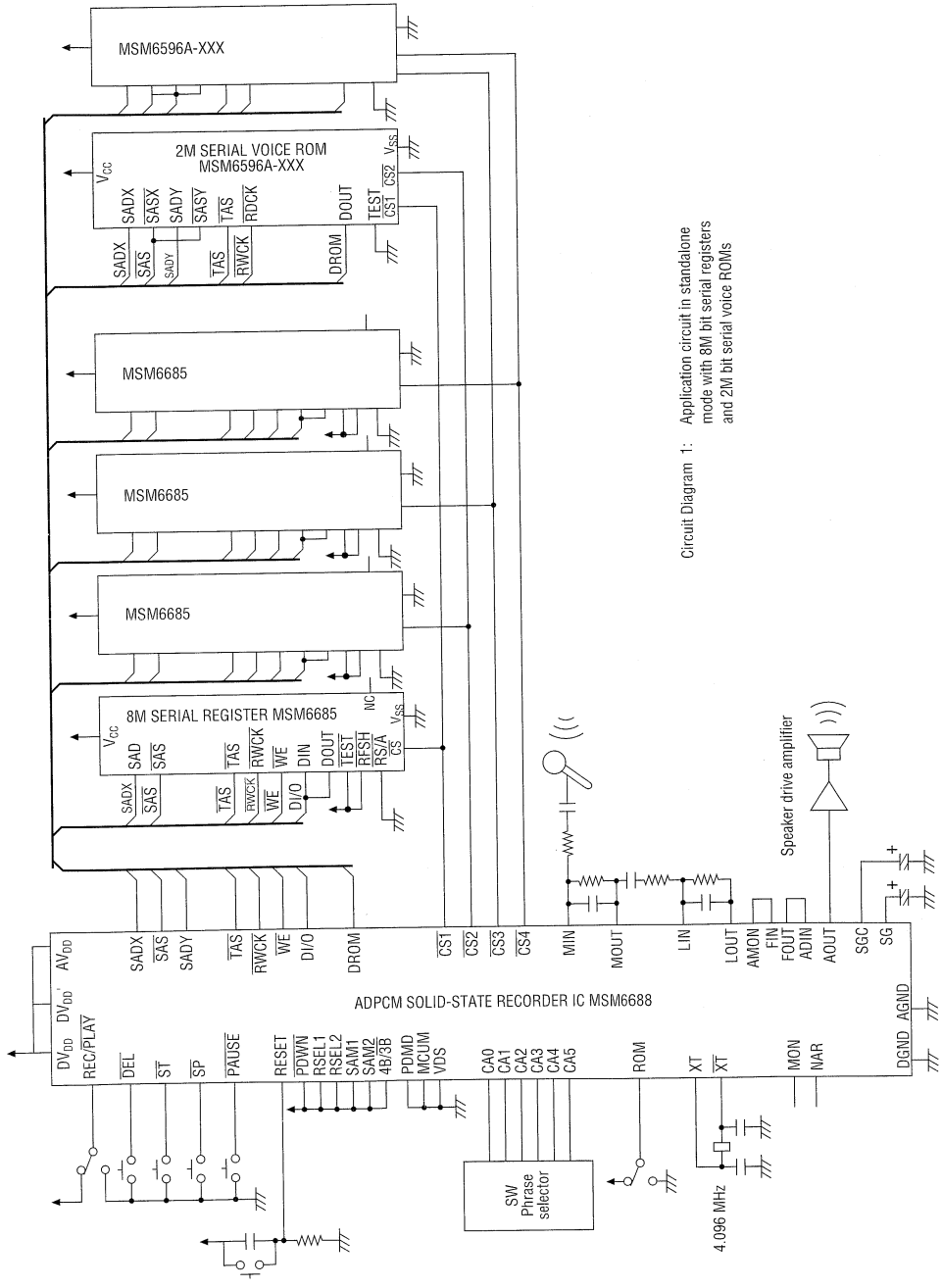
Analog Characteristics

DVDD=DVDD'=AVDD=4.5 to 5.5V
DGND=AGND=0V Ta=−40 to +85°C

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	VDD-1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	VDD	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0~4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

APPLICATION CIRCUIT

The circuit diagram 1 shows an application circuit example where the MSM6688 is used in the stand-alone mode and four 8M bit serial registers and two 2M bit serial voice ROMs also connected.



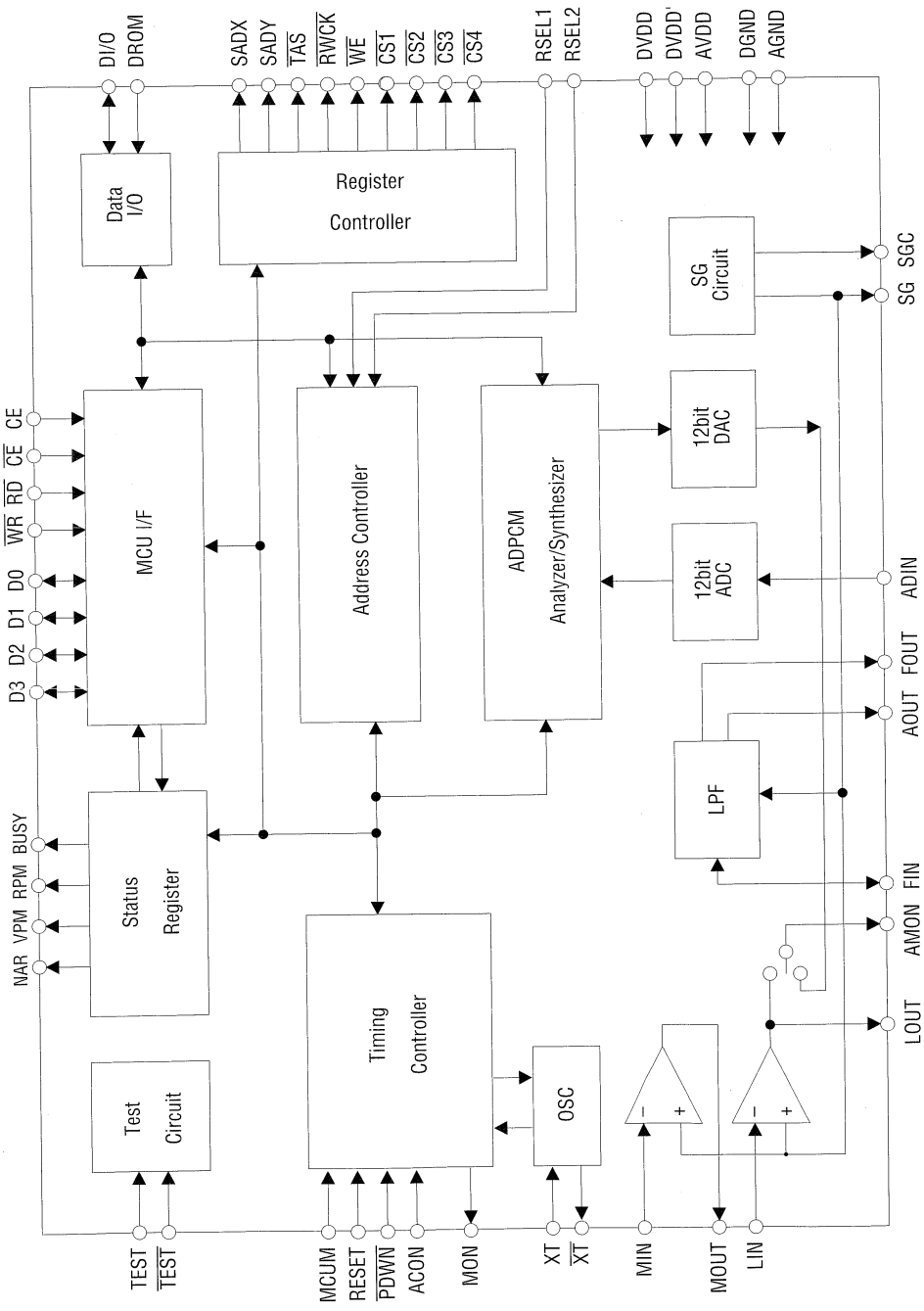
Circuit Diagram 1: Application circuit in standalone mode with 8M bit serial registers and 2M bit serial voice ROMs

(2) MICROCONTROLLER INTERFACE MODE (for MSM6688 (5 V Version) and MSM6688L (3 V Version))

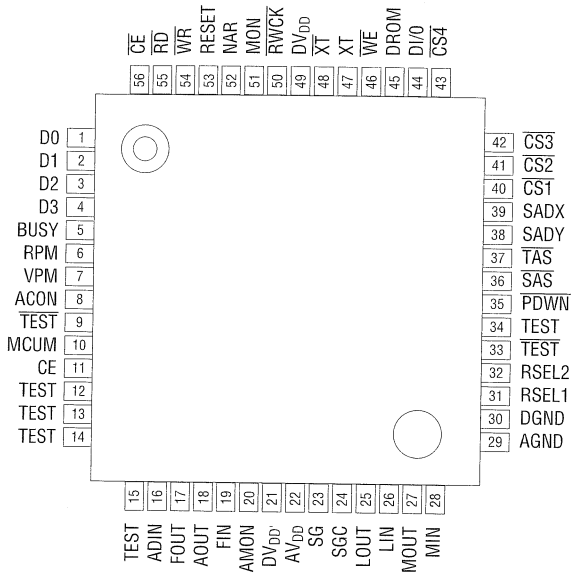
FEATURES

- 3-bit or 4-bit ADPCM
- Built-in 12-bit AD converter
- Built-in12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External only registers (for variable messages)
  MSM6688 (5 V version)
  - Serial registers, 32M bits maximum
    One 4M bit serial register (MSM6684B) can be driven directly
    Up to four 8M bit serial register (MSM6685) can be driven directly
  MSM6688L (3 V version)
  - Serial registers, 4M bits maximum
    One 4M bit serial register (MSM66V84B) can be driven directly
- External only ROMs (for fixed messages)
  - Serial voice ROMs, 4M bits maximum
    1M bit serial voice ROM (MSM6595A) can be driven directly
    2M bit serial voice ROM (MSM6596A) can be driven directly
    3M bit serial voice ROM (MSM6597A) can be driven directly
- Sampling frequency
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz (master clock frequency = 4.096 MHz)
  8.0 kHz, 10.6 kHz, 12.8 kHz or 16.0 kHz (master clock frequency = 8.192 MHz)
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Maximum recording time (when external 32M bit RAM is connected)
  34 minutes (for 16 kbps ADPCM)
  23 minutes (for 24 kbps ADPCM)
  17 minutes (for 32 kbps ADPCM)
- Voice triggered starting function
- Pause function
- Master clock frequency: 4.096 MHz ~ 8.192 MHz
- Power supply voltage
  MSM6688: Single 5 Vpower supply
  MSM6688L: Single 3 V power supply
- Package options:
  MSM6688: 56-pin plastic QFP (QFP56-P-910-2K) (Product name: MSM6688GS-2K)
  MSM6688L: 56-pin plastic QFP (QFP56-P-910-2K) (Product name: MSM6688LGS-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



56-Pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description
DVDD	I	Digital power supply pin. Insert a bypass capacitor of 0.1µF or more between this pin and the DGND pin.
DVDD'	I	Digital power supply pin
AVDD	I	Analog power supply pin. Insert a bypass capacitor of 0.1µF or more between this pin and the AGND pin.
DGND	I	Digital ground pin
AGND	I	Analog ground pin
SG, SGC	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	O	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
FIN	I	Input pin of the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin)
ADIN	I	Input pin of the built-in 12-bit AD converter.
AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
SADX SADY	O	(Serial Address Data). SADX is used to connect the SAD pin of each external serial register and the SADX pin of each external serial voice ROM. SADY is used to connect the SADY pin of each external serial voice ROM. Outputs of starting address of read/write.
$\overline{SAS}$	O	(Serial Address Strobe). Used to connect the $\overline{SAS}$ pin of external serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of external serial voice ROM Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe). Used to connect the $\overline{TAS}$ pin of each external serial register and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each serial register and serial voice ROM.
$\overline{RWCK}$	O	(Read/Write Clock). Used to connect the $\overline{RWCK}$ pin of each external serial register and the RDCK pin of each external serial voice ROM. This pin outputs a clock to read data from or write it into each external serial register.
$\overline{WE}$	O	(Write Enable) Used to connect the $\overline{WE}$ pin of each external serial register. This pin outputs $\overline{WE}$ signal to select either read or write mode.
DI/O	I/O	(Data I/O). Used to connect the DIN and DOUT pins of DRAM and serial register. This pin outputs the data to be written into the serial register or inputs the data read from the serial registers.
DROM	I	(Data ROM). Used to connect the DOUT pin of each external serial voiceROM.

Symbol	Type	Description
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O O O O	(Chip Select). Used to connect the $\overline{CS}$ pin of serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of each serial voice ROM.
RSEL1 RSEL2	I I	(Register Select). These are used to select the number of external serial registers. RSEL2: L L H H RSEL1: L H L H Number of serial registers: 1 2 3 4
MCUM	I	This pin is used to select either the stand-alone mode or the microcontroller interface mode. Low level: Stand-alone mode High level: Microcontroller interface mode
RESET	I	A high input level at this pin causes the MSM6688/6688L to be initialized and to go into the power down state.
$\overline{PDWN}$	I	(Power Down). When a low level is input to this pin, the MSM6688 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6688/6688L. When an low level is applied to this $\overline{PDWN}$ pin during recording operation, the MSM6688/6688L is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low. After this pin is restored to a high level, postprocessing for recording will be performed.
D0 D1 D2 D3	I/O	Bi-directional data bus to transfer commands and data to and from an external microcontroller.
$\overline{WR}$	I	Write pulse input pin. Inputting a low pulse to this $\overline{WR}$ pin causes a command or data to be input via D0~D3 pins.
$\overline{RD}$	I	Read pulse input pin. Inputting a low pulse to this $\overline{RD}$ pin causes status bits or data to be output via D0~D3 pins.
$\overline{CE}$ CE	I I	Chip enable input pins. When the $\overline{CE}$ pin is set to a low level or the CE pin is set to a high level, the write pulse ($\overline{WR}$), read pulse ($\overline{RD}$) can be accepted. When the $\overline{CE}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{WR}$) and read pulse ($\overline{RD}$) cannot be accepted so that data cannot be transferred to and from via D0~D3 pins.
BUSY	O	Outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0~D3 pins. The state of this BUSY pin is the same as the contents of the BUSY bit of the status register.
RPM	O	Outputs a high level during recording or playback operation. The state of this RPM is the same as the contents of the RPM bit of the status register.
VPM	O	Outputs a high level during the standby for voice after the start of voice triggered recording and the record/playback is stopped temporarily by inputting the PAUSE command. The state of this VPM pin is the same as the contents of the VPM bit of the status register.

Symbol	Type	Description
NAR	O	This NAR bit indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM playback operation, specify the next phrase after making sure that the NAR output is high, and input the START command.
ACON	I	Used to select the use or nonuse of the pop noise suppression circuit at the analog output (AOUT) pin. When low level, the pop noise suppression circuit is not used. When high level, the pop noise suppression circuit is used.
XT	I	Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.
$\overline{XT}$	O	Used to connect an oscillator, when an external clock is used, this pin must be left open.
MON	O	Outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
TEST $\overline{TEST}$	I	Used to test the MSM6688/6688L. Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.

ABSOLUTE MAXIMUM RATINGS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	VDD	Ta=25°C	−0.3 to+7.0	V
Input voltage	V_{IN}	Ta=25°C	−0.3 to VDD+0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	VDD	DGND=AGND=0V	+3.5 to +5.5 (Note 3)	V
Operating temperature	T_{op}	—	−40 to +85	°C
Master clock frequency	fosc	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6688 (5 V Version))

DC Characteristics

DVDD=DVDD'=AVDD=4.5 to 5.5V (Note 3)
DGND=AGND=0V Ta=−40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.8×VDD	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×VDD	V
High output voltage	V_{OH}	I_{OH}=−40μA	VDD−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2mA	—	—	0.45	V
High input current (Note 1)	I_{IH1}	V_{IH}=VDD	—	—	10	μA
High input current (Note 2)	I_{IH2}	V_{IH}=VDD	—	—	20	μA
Low input current (Note 1)	I_{IL1}	V_{IL}=GND	−10	—	—	μA
Low input current (Note 2)	I_{IL2}	V_{IL}=GND	−20	—	—	μA
Operating current consumption	I_{DD}	fosc = 8 MHz, no load	—	15	30	mA
Standby current consumption	I_{DDS}	During power down, no load, Ta=−40 to +70°C	—	—	10	μA
		During power down, no load, Ta=+70 to +85°C	—	—	50	μA

Note: 1. Applies to all input pins excluding the XT pin.
2. Applies to the XT pin.
3. Recording and playback should be performed at a power supply voltage of 4.5 to 5.5V. For other operations such as backup for a serial register, the IC operates at 3.5 to 5.5V.

Analog Characteristics

DVDD=DVDD'=AVDD=4.5 to 5.5V
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	VDD-1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	VDD	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

ABSOLUTE MAXIMUM RATINGS (for MSM6688L (3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	VDD	Ta=25°C	−0.3 to+7.0	V
Input voltage	V_{IN}	Ta=25°C	−0.3 to VDD+0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6688L (3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	VDD	DGND=AGND=0V	+2.7 to +3.6	V
Operating temperature	T_{op}	—	−40 to +85	°C
Master clock frequency	fosc	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6688L (3 V Version))

DC Characteristics

DVDD=DVDD'=AVDD=2.7 to 3.6V
DGND=AGND=0V Ta=−40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.85×VDD	—	—	V
Low input voltage	V_{IL}	—	—	—	0.15×VDD	V
High output voltage	V_{OH}	I_{OH}=−40μA	VDD−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2mA	—	—	0.45	V
High input current (Note 1)	I_{IH1}	V_{IH}=VDD	—	—	10	μA
High input current (Note 2)	I_{IH2}	V_{IH}=VDD	—	—	20	μA
Low input current (Note 1)	I_{IL1}	V_{IL}=GND	−10	—	—	μA
Low input current (Note 2)	I_{IL2}	V_{IL}=GND	−20	—	—	μA
Operating current consumption	IDD	fosc = 8 MHz, no load	—	15	30	mA
Standby current consumption	IDDS	During power down, no load, Ta=−40 to +70°C	—	—	15	μA
		During power down, no load, Ta=+70 to +85°C	—	—	100	μA

Note: 1. Applies to all input pins excluding the XT pin.
2. Applies to the XT pin.

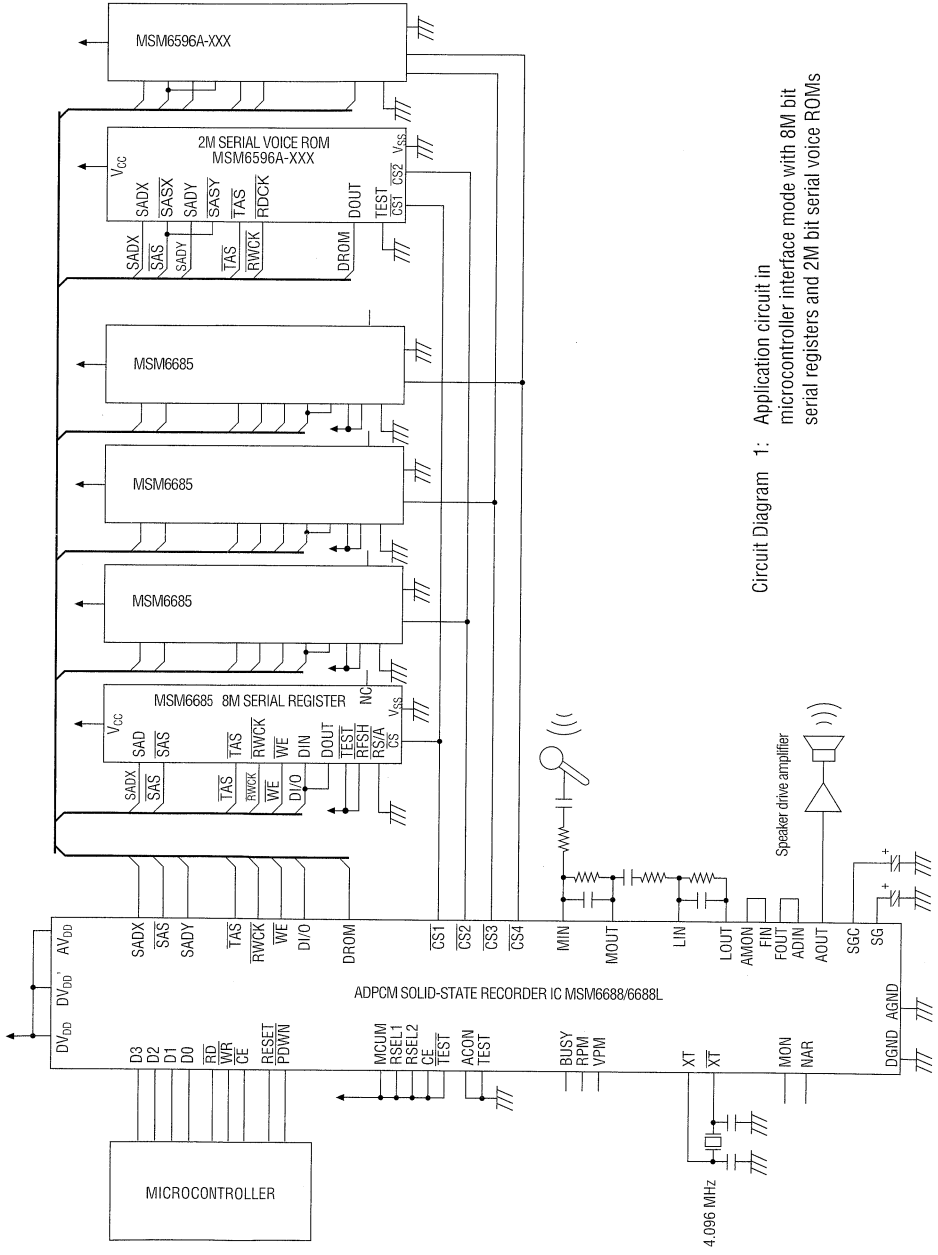
Analog Characteristics

DVDD=DVDD'=AVDD=2.7 to 3.6V
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1/4×VDD	—	3/4×VDD	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	VDD	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

APPLICATION CIRCUIT

The circuit diagram 1 shows an application circuit example where the MSM6688/6688L is used in the microcontroller interface mode and four 8M bit serial registers and two 2M bit serial voice ROMs are connected.



Circuit Diagram 1: Application circuit in microcontroller interface mode with 8M bit serial registers and 2M bit serial voice ROMs

MSM6789A/6789L

SBC Solid-State Recorder IC

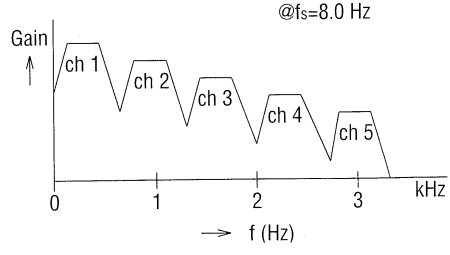
GENERAL DESCRIPTION

The MSM6789A/6789L, an improved version of MSM6788, is a solid-state recorder developed using the Sub Band Coding (SBC) method.
Just like MSM6788, the MSM6789A/6789L has a stand-alone mode and a microcontroller interface mode. In the stand-alone mode, record/playback conditions can be selected from pins and the MSM6789A/6789L can be controlled by a simple drive timing. In the microcontroller interface mode, record/playback can be controlled by commands from the microcontroller, and more functions are available than in the stand-alone mode.
The MSM6789A/6789L can directly drive serial voice ROM as external memory as well as serial register or general-purpose DRAM* (1-bit × or 4-bit × type selectable) as external memories, which allows a recording and playback circuit with fixed messages to be built easily. The method from microcontroller is the same as the MSM6788.
* Only for MSM6789A

- Difference between MSM6788 and MSM6789A

	MSM6788	MSM6789A
General DRAM	Unavailable	Available
Unvoiced-part elimination function	No	Yes
PCM playback	No	Yes

- SBC method:
  The SBC method divides voice frequencies into five bands and codes the component for each of the bands separately, as shown below.



Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

• Difference between MSM6789A and MSM6789L

Parameter	MSM6789A	MSM6789L
Operating voltage	4.5 to 5.5 V	3.0 to 3.6 V
External memory	General-purpose DRAM, 32 Mbits (max.) 1-Mbit DRAM (MSM514256B, MSM511000B) 4-Mbit DRAM (MSM514400C, MSM514100C) 16-Mbit DRAM (MSM511740CA, MSM5116100A) ARAM*, 32 Mbits (max.) Serial register, 32 Mbits (max.) 4 Mbits (MSM6684B) 8 Mbits (MSM6685)	16 Mbits (max.) 4 Mbits (MSM66V84B)

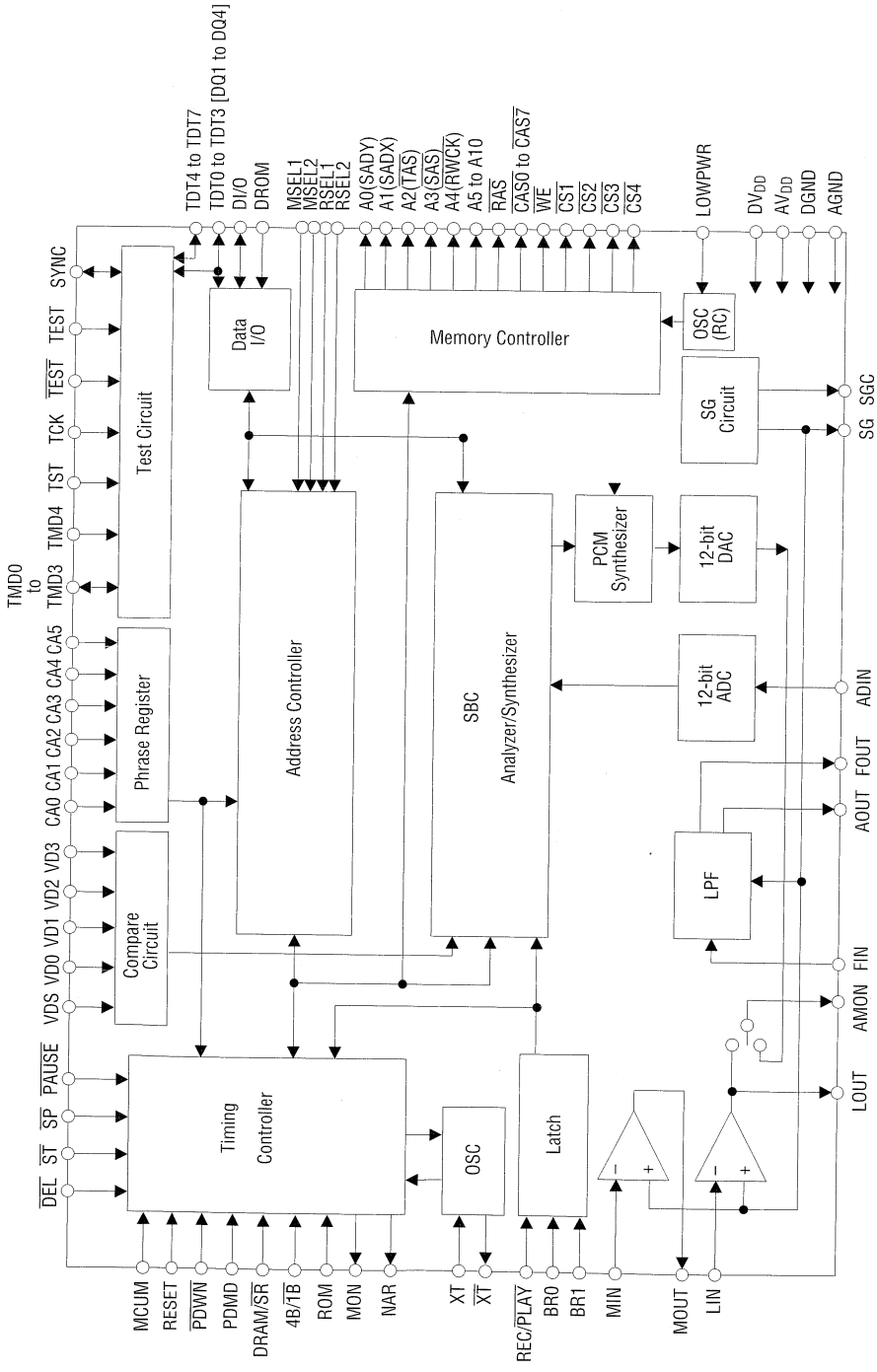
* Use ARAM which has no failed bits in its first 64 Kbits.

STAND-ALONE MODE

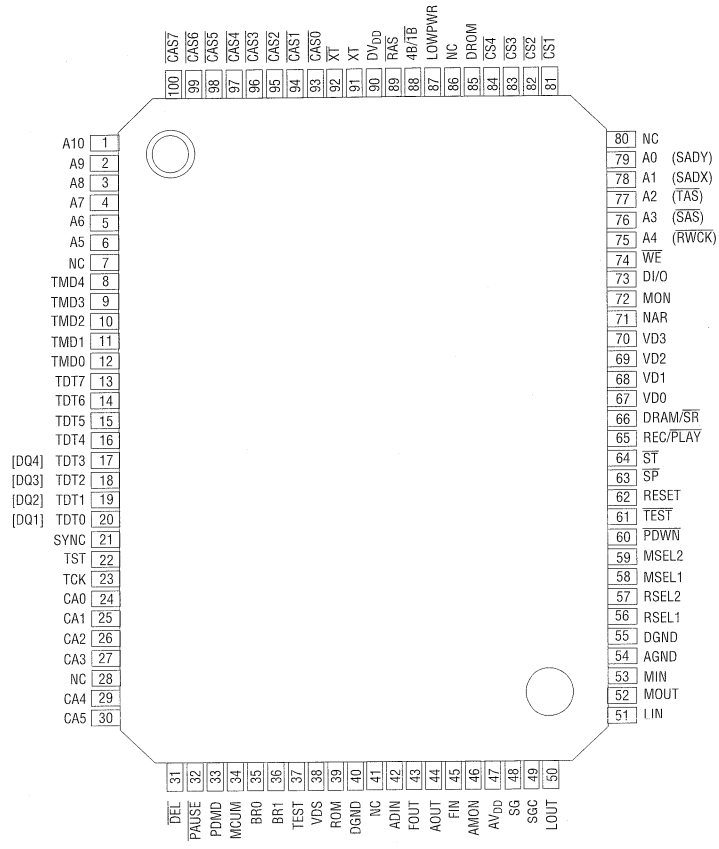
FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  MSM6789A (5 V version)
    General-purpose DRAM, 32 Mbits maximum (for variable messages)
      1-Mbit DRAM : Can be directly driven (MSM514256B, MSM511000B)
      4-Mbit DRAM : Can be directly driven (MSM514400C, MSM514100C)
      16-Mbit DRAM : Can be directly driven (MSM5117400A, MSM5116100A)
    ARAM, 32 Mbits maximum (for variable messages)
      Note :Use the first 64 Kbits with no failed bits for the ARAM.
    Serial register, 32 Mbits maximum (for variable messages)
      4-Mbit serial register : Can be directly driven (MSM6684B)
      8-Mbit serial register : Can be directly driven (MSM6685)
  MSM6789L (3.3 V version)
    Serial register, 16 Mbits maximum (for variable messages)
      4-Mbit serial resister: Can be directly driven (MSM66V84B)
  MSM6789A (5 V version) and MSM6789L (3.3 V version)
    Serial voice ROM, 4 Mbits maximum (for fixed messages)
      1-Mbit serial voice ROM : Can be directly driven (MSM6595A)
      2-Mbit serial voice ROM : Can be directly driven (MSM6596A)
      3-Mbit serial voice ROM : Can be directly driven (MSM6597A)
- Bit rate
  10.0, 12.6, 16.0 kbps (at 8 kHz sampling freq.)
  7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)
- Maximum recording time (when one 8-Mbit serial register is connected)
  13.8 minutes (for 10.0 kbps SBC) 18.4 minutes (for 7.5 kbps SBC)
  11.0 minutes (for 12.6 kbps SBC) 14.6 minutes (for 9.5 kbps SBC)
  8.6 minutes (for 16.0 kbps SBC) 11.5 minutes (for 12.0 kbps SBC)
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Unvoiced-part elimination function (voice detect level can be set)
- Pausing function
- Master clock frequency: 6.0 MHz to 8.192 MHz
- Power supply voltage:
    MSM6789A : Single 5 V power supply
    MSM6789L : Single 3.3 V power supply
- Package options:
    MSM6789A : 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK)
    MSM6789L : 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

( ) : Pins for connecting serial voice ROM
[ ] : Pins for connecting 4-bit × type DRAM
NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1 µF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1 µF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	—	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
66	DRAM/$\overline{SR}$	I	This pin selects whether memory to be connected externally is DRAM or serial register. Low level : Serial register High level : DRAM
88	4B/$\overline{1B}$	I	This pin selects either 1-bit × type DRAM or 4-bit × type DRAM. Low level : 1-bit × type High level : 4-bit × type
79 78	A0 (SADY) A1 (SADX)	O	These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also connect to SAD pin of serial register and serial voice ROM at the time of serial register selection. These pins output leading addresses of read/write.
77	A2 ($\overline{TAS}$)	O	This pin connects to A2 of DRAM at the time of DRAM selection. It also connects to $\overline{TAS}$ pin of serial register and serial voice ROM at the time of serial register selection. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	A3 ($\overline{SAS}$)	O	This pin connects to A3 of DRAM at the time of DRAM selection. It also connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM at the time of serial register selection. Clock pin to write serial addresses.
75	A4 ($\overline{RWCK}$)	O	This pin connects to A4 of DRAM at the time of DRAM selection. It also connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM at the time of serial register selection. Clock pin to read data from and write data into the serial register.
1-6	A10-A5	O	This pin connects to pins A5-A10 of DRAM at the time of DRAM selection. This pin outputs addresses of read/write.

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

Pin	Symbol	Type	Description
74	$\overline{WE}$	O	**Write Enable.** This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	I/O	**Data I/O.** This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data.
85	DROM	I	**Data ROM.** This pin connects to the DOUT pin of the serial voice ROM.
89	$\overline{RAS}$	O	This is a row address strobe pin of DRAM at the time of DRAM selection.
93-100	$\overline{CAS0}$-$\overline{CAS7}$	O	These are the column address strobe pins of DRAM at the time of DRAM selection. $\overline{CAS7}$, an addresss output pin, is connected to pin A11 of DRAM at the time 16-Mbit DRAM selection.
81 82 83 84	$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	**Chip Select.** These pins connect to $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.
58 59	MSEL1 MSEL2	I I	These pins select the capacity of the memory to be connected externally.
56 57	RSEL1 RSEL2	I I	These pins select the number of DRAMs and serial registers to be connected externallly. • When DRAM is selected (DRAM/$\overline{SR}$ = High level)

MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity
L	L	L	L	1M × 4
L	L	L	H	4M × 1
L	L	H	L	1M × 8
L	L	H	H	1M × 4 + 4M × 1
L	H	L	L	4M × 2
L	H	L	H	4M × 2
L	H	H	L	4M × 3
L	H	H	H	4M × 3
H	L	L	L	4M × 4
H	L	L	H	16M × 1
H	L	H	L	4M × 6
H	L	H	H	4M × 6
H	H	L	L	4M × 8
H	H	L	H	4M × 8
H	H	H	L	16M × 2
H	H	H	H	16M × 2

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>• When serial register is selected (DRAM/$\overline{SR}$ = Low level)
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M × 4</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>8M × 1</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>8M × 2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>8M × 3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>8M × 4</td></tr>
</table></td></tr>
<tr><td>87</td><td>LOWPWR</td><td>I</td><td>This pin selects $\overline{CAS}$-before-$\overline{RAS}$ refresh period of DRAM at the time of power down when DRAM is selected.
Low level : 15 µs max.
High level : 125 µs max.</td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789A to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{PDWN}$</td><td>I</td><td>Power Down. When a low level is input, the MSM6789A goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789A to be reset. When a Low level is applied to this pin during recording operation, the MSM6789A is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low level. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>91</td><td>XT</td><td>I</td><td>Oscillator Connection. When an external clock is used, input the clock through this pin. During the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>92</td><td>$\overline{XT}$</td><td>O</td><td>Oscillator Connection. When an external clock is used, this pin must be left open.</td></tr>
<tr><td>37
61</td><td>TEST
$\overline{TEST}$</td><td>I</td><td>MSM6789A Test. Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.</td></tr>
<tr><td>9-12
13-20
21</td><td>TMD3-TMD0
TDT7-TDT0
SYNC</td><td>I/O</td><td>MSM6789A Test. This pin must be left open.</td></tr>
<tr><td>17-20</td><td>TDT3-TDT0
[DQ4]-[DQ1]</td><td>I/O</td><td>Connect these pins to DQ1-DQ4 of DRAM at the time of 4-bit × type DRAM selection. Otherwise these pins must be left open as they are MSM6789A test pins.</td></tr>
<tr><td>22
23
8</td><td>TST
TCK
TMD4</td><td>I</td><td>MSM6789A Test. Input a low level signal.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>39</td><td>ROM</td><td>I</td><td>Playback Operation. When set to low, this pin selects the record/playback operation (only for the SBC method). When set to high, it selects the ROM playback operation (for the SBC and PCM methods).</td></tr>
<tr><td>65</td><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Recording mode or playback mode selection. This pin is invalid during the ROM playback operation. When set to low, it selects the playback mode. When set to high, it selects the recording mode.</td></tr>
<tr><td>64</td><td>$\overline{\text{ST}}$</td><td>I</td><td>Start Playback. When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>63</td><td>$\overline{\text{SP}}$</td><td>I</td><td>Stop Playback.When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>32</td><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>Playback Pause. When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>31</td><td>$\overline{\text{DEL}}$</td><td>I</td><td>Phrase Delection. When a low level pulse is applied to this pin, all phrase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00: All phrase deletion
ch01 to ch3F: Specified phrase deletion
After power up, be sure to input a RESET signal and then delete all phrases.
After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>24-30</td><td>CA0-CA5</td><td>I</td><td>Desired Phrase Specification.
A total of 63 phrases can be specified indepedently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phrase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="6">A total of 63 phrases can be used for both record /playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>35
36</td><td>BR0
BR1</td><td>I</td><td>Bit Rate Selection. This pin selects one of the following three types of bit rate (master clock frequency f_{OSC} = 8.192 MHz). This pin is invalid during the ROM playback operation.
<table>
<tr><th>BR1</th><th>BR0</th><th>Bit rate</th></tr>
<tr><td>L</td><td>L</td><td>16.0 kbps</td></tr>
<tr><td>L</td><td>H</td><td>12.6 kbps</td></tr>
<tr><td>H</td><td>L</td><td>10.0 kbps</td></tr>
<tr><td>H</td><td>H</td><td>Unused</td></tr>
</table></td></tr>
<tr><td>33</td><td>PDMD*1</td><td>I</td><td>Transition to the Power-down State.
Low level: The MSM6789A automatically goes to the power-down state, except when the record/playback operation is performed.
High level: The MSM6789A automatically goes to the standby state, instead of the power-down state, except when the record/playback operation is performed. In this case, the MSM6789A can be placed in the power-down state by setting the RESET or PDWN pin to a high level. If an external circuit is used for the built-in LPF, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>67-70</td><td>VD0-VD3</td><td>I</td><td>These pins set the voice detect level for the voice triggered starting and unvoiced-part elimination.</td></tr>
<tr><td>38</td><td>VDS</td><td>I</td><td>This pin selects the voice triggered starting or the unvoiced-part elimination.
Voice triggered starting: Input a High level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Unvoiced-part elimination: Input a Low level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Note: When neither the voice triggered starting nor the unvoiced-part elimination is used, input a Low level to VD0 to VD3.</td></tr>
<tr><td>72</td><td>MON</td><td>O</td><td>This pin outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>71</td><td>NAR</td><td>O</td><td>Output to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after the NAR pin goes to high positively.</td></tr>
</table>

*1 When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input voltage	V_{IN}	Ta=25°C	−0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.5 to +5.5*4	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5 V*4
DGND=AGND=0 V, Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.8×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=−40 µA	V_{DD}−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current *1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current *2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input currcent *1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
Low input current *2	I_{IL2}	V_{IL}=GND	−20	—	—	µA
Low input current *3	I_{IL3}	V_{IL}=GND	−400	—	−20	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

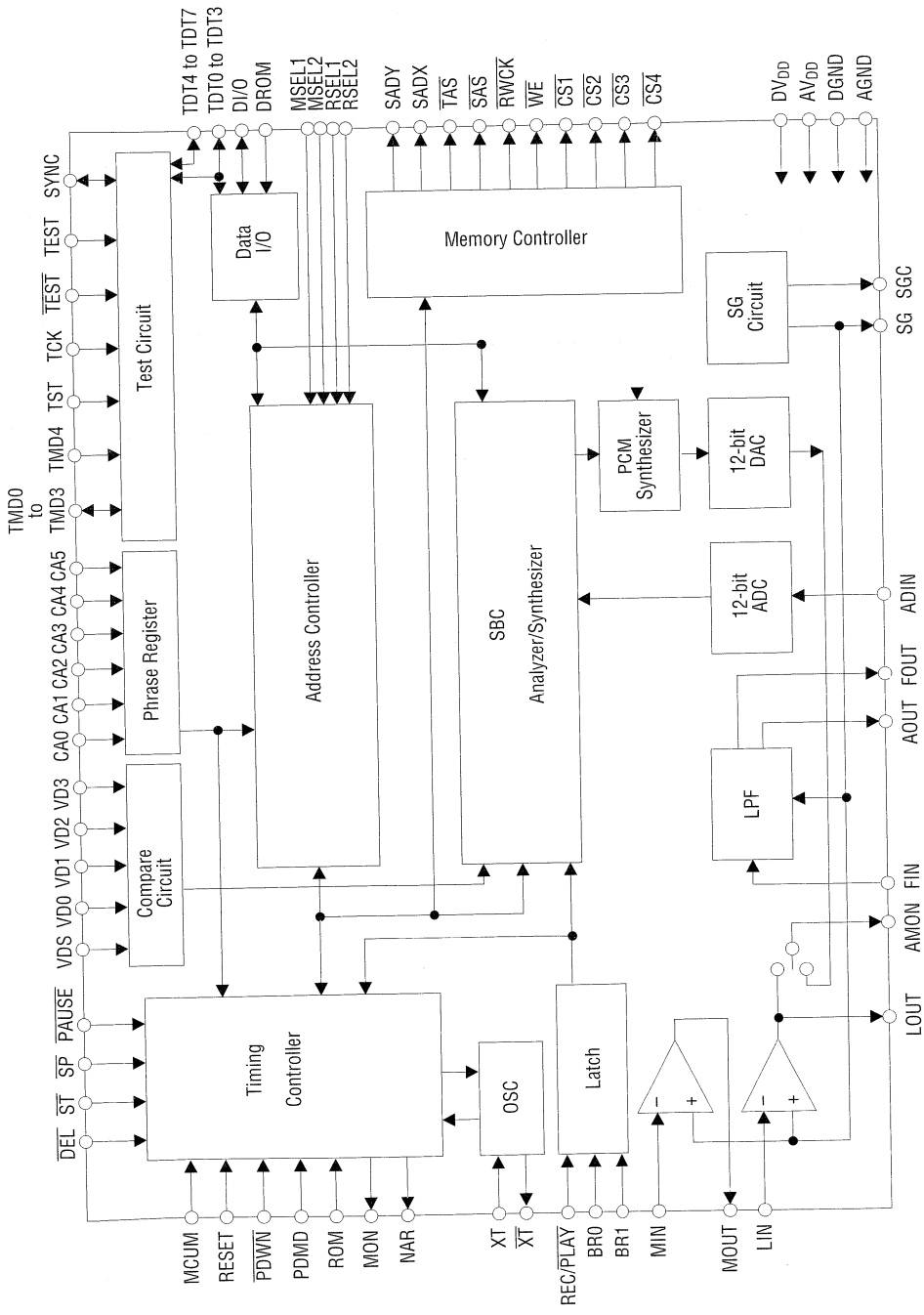
*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.
*3 Applies to the input pins with pull-up resistor ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, $\overline{DEL}$) excluding the XT pin.
*4 The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

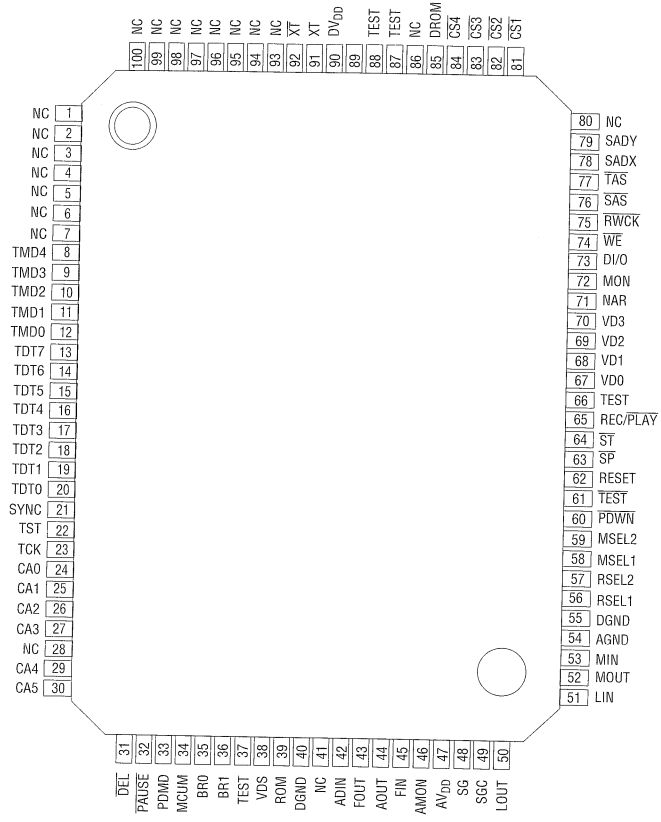
$DV_{DD}=AV_{DD}=4.5$ to 5.5 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	$V_{DD}-1$	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-map open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3 V Version))



100-Pin Plastic QFP

NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1 µF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1 µF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	—	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
79 78	SADY SADX	O	They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write.
77	$\overline{TAS}$	O	This pin connects to $\overline{TAS}$ pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	$\overline{SAS}$	O	This pin connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM. Clock pin to write serial addresses.
75	$\overline{RWCK}$	O	This pin connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM. Clock pin to read data from and write data into the serial register.
74	$\overline{WE}$	O	**Write Enable.** This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	I/O	**Data I/O.** This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data.
85	DROM	I	**Data ROM.** This pin connects to the DOUT pin of the serial voice ROM.
81 82 83 84	$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	**Chip Select.** These pins connect to $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>58
59</td><td>MSEL1
MSEL2</td><td>I
I</td><td>These pins select the capacity of the memory to be connected externally.</td></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>These pins select the number of and serial registers to be connected externallly.
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M × 4</td></tr>
</table></td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789L to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{\text{PDWN}}$</td><td>I</td><td>Power Down. When a low level is input, the MSM6789L goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789L to be reset. When a Low level is applied to this pin during recording operation, the MSM6789L is halted, and will be maintained in the power down state while $\overline{\text{PDWN}}$ is low level. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>91</td><td>XT</td><td>I</td><td>Oscillator Connection. When an external clock is used, input the clock through this pin. During the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>92</td><td>$\overline{\text{XT}}$</td><td>O</td><td>Oscillator Connection. When an external clock is used, this pin must be left open.</td></tr>
<tr><td>37
61</td><td>TEST
$\overline{\text{TEST}}$</td><td>I</td><td>MSM6789L Test. Input a low level to the TEST pin and a high level to the $\overline{\text{TEST}}$ pin.</td></tr>
<tr><td>9-12
13-20
21</td><td>TMD3-TMD0
TDT7-TDT0
SYNC</td><td>I/O</td><td>MSM6789L Test. This pin must be left open.</td></tr>
<tr><td>17-20</td><td>TDT3-TDT0</td><td>I/O</td><td>These pins must be left open as they are MSM6789L test pins.</td></tr>
<tr><td>22
23
8</td><td>TST
TCK
TMD4</td><td>I</td><td>MSM6789L Test. Input a low level signal.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>39</td><td>ROM</td><td>I</td><td>Playback Operation. When set to low, this pin selects the record/playback operation (only for the SBC method). When set to high, it selects the ROM playback operation (for the SBC and PCM methods).</td></tr>
<tr><td>65</td><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Recording mode or playback mode selection. This pin is invalid during the ROM playback operation. When set to low, it selects the playback mode. When set to high, it selects the recording mode.</td></tr>
<tr><td>64</td><td>$\overline{\text{ST}}$</td><td>I</td><td>Start Playback. When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>63</td><td>$\overline{\text{SP}}$</td><td>I</td><td>Stop Playback.When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>32</td><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>Playback Pause. When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>31</td><td>$\overline{\text{DEL}}$</td><td>I</td><td>Phrase Delection. When a low level pulse is applied to this pin, all phrase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00: All phrase deletion
ch01 to ch3F: Specified phrase deletion
After power up, be sure to input a RESET signal and then delete all phrases.
After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>24-30</td><td>CA0-CA5</td><td>I</td><td>Desired Phrase Specification.
A total of 63 phrases can be specified indepedently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phrase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="6">A total of 63 phrases can be used for both record /playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>35
36</td><td>BR0
BR1</td><td>I</td><td>Bit Rate Selection. This pin selects one of the following three types of bit rate (master clock frequency f_{OSC} = 8.192 MHz). This pin is invalid during the ROM playback operation.
<table>
<tr><th>BR1</th><th>BR0</th><th>Bit rate</th></tr>
<tr><td>L</td><td>L</td><td>16.0 kbps</td></tr>
<tr><td>L</td><td>H</td><td>12.6 kbps</td></tr>
<tr><td>H</td><td>L</td><td>10.0 kbps</td></tr>
<tr><td>H</td><td>H</td><td>Unused</td></tr>
</table></td></tr>
<tr><td>33</td><td>PDMD*1</td><td>I</td><td>Transition to the Power-down State.
Low level: The MSM6789L automatically goes to the power-down state, except when the record/playback operation is performed.
High level: The MSM6789L automatically goes to the standby state, instead of the power-down state, except when the record/playback operation is performed. In this case, the MSM6789L can be placed in the power-down state by setting the RESET or PDWN pin to a high level. If an external circuit is used for the built-in LPF, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>67-70</td><td>VD0-VD3</td><td>I</td><td>These pins set the voice detect level for the voice triggered starting and unvoiced-part elimination.</td></tr>
<tr><td>38</td><td>VDS</td><td>I</td><td>This pin selects the voice triggered starting or the unvoiced-part elimination.
Voice triggered starting: Input a High level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Unvoiced-part elimination: Input a Low level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Note: When neither the voice triggered starting nor the unvoiced-part elimination is used, input a Low level to VD0 to VD3.</td></tr>
<tr><td>72</td><td>MON</td><td>O</td><td>This pin outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>71</td><td>NAR</td><td>O</td><td>Output to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after the NAR pin goes to high positively.</td></tr>
</table>

*1 When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input voltage	V_{IN}	Ta=25°C	−0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=3.0 to 3.6 V
DGND=AGND=0 V, Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.85×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.15×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=−40 µA	V_{DD}−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current *1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current *2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input currcent *1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
Low input current *2	I_{IL2}	V_{IL}=GND	−20	—	—	µA
Low input current *3	I_{IL3}	V_{IL}=GND	−400	—	−20	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.
*3 Applies to the input pins with pull-up resistor ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, $\overline{DEL}$) excluding the XT pin.

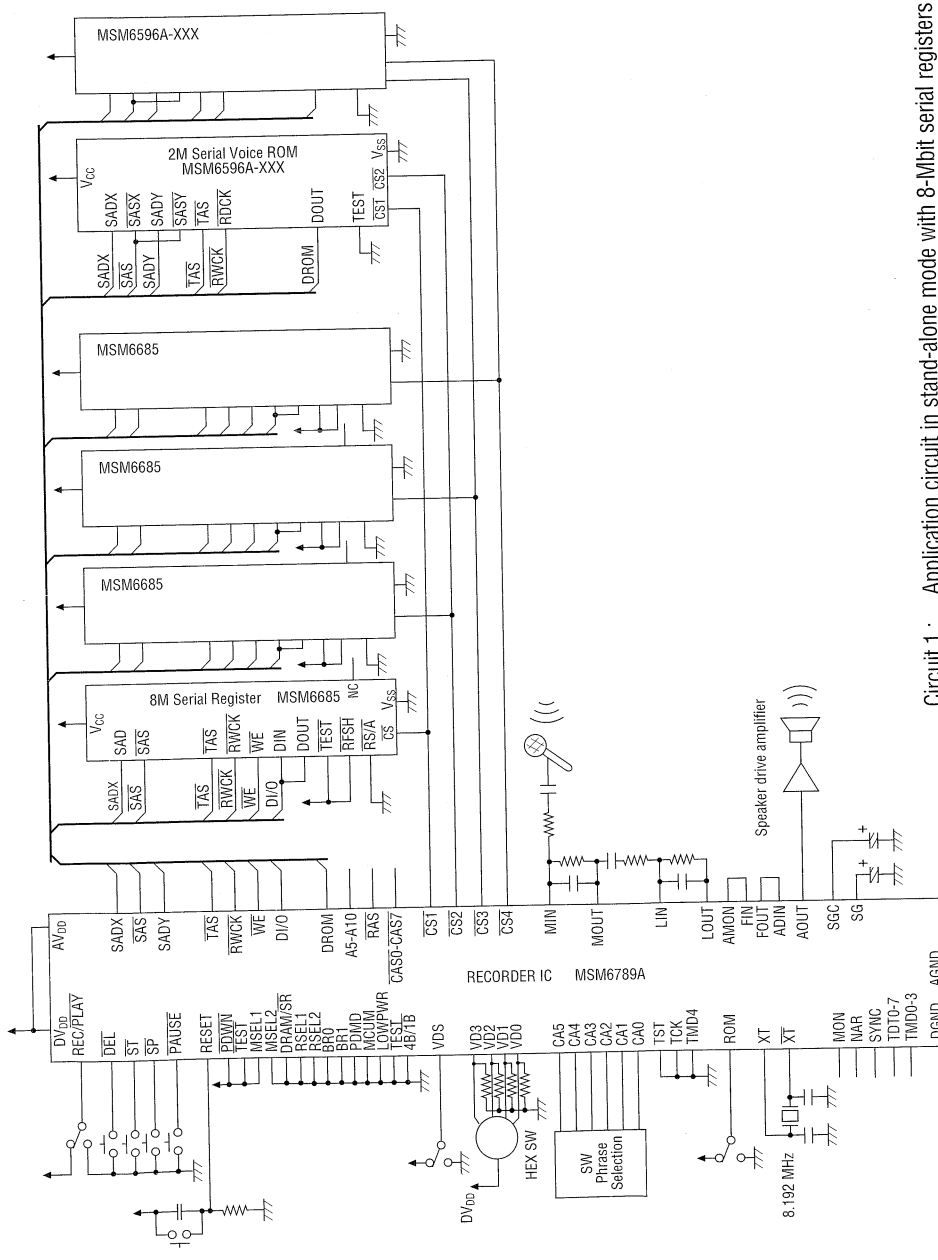
Analog Characteristics

$DV_{DD}=AV_{DD}=3.0$ to 3.6 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	20	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	$V_{DD}-1$	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-map open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	400	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	100	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	100	—	—	kΩ

APPLICATION CIRCUITS (for MSM6789A (5 V version))

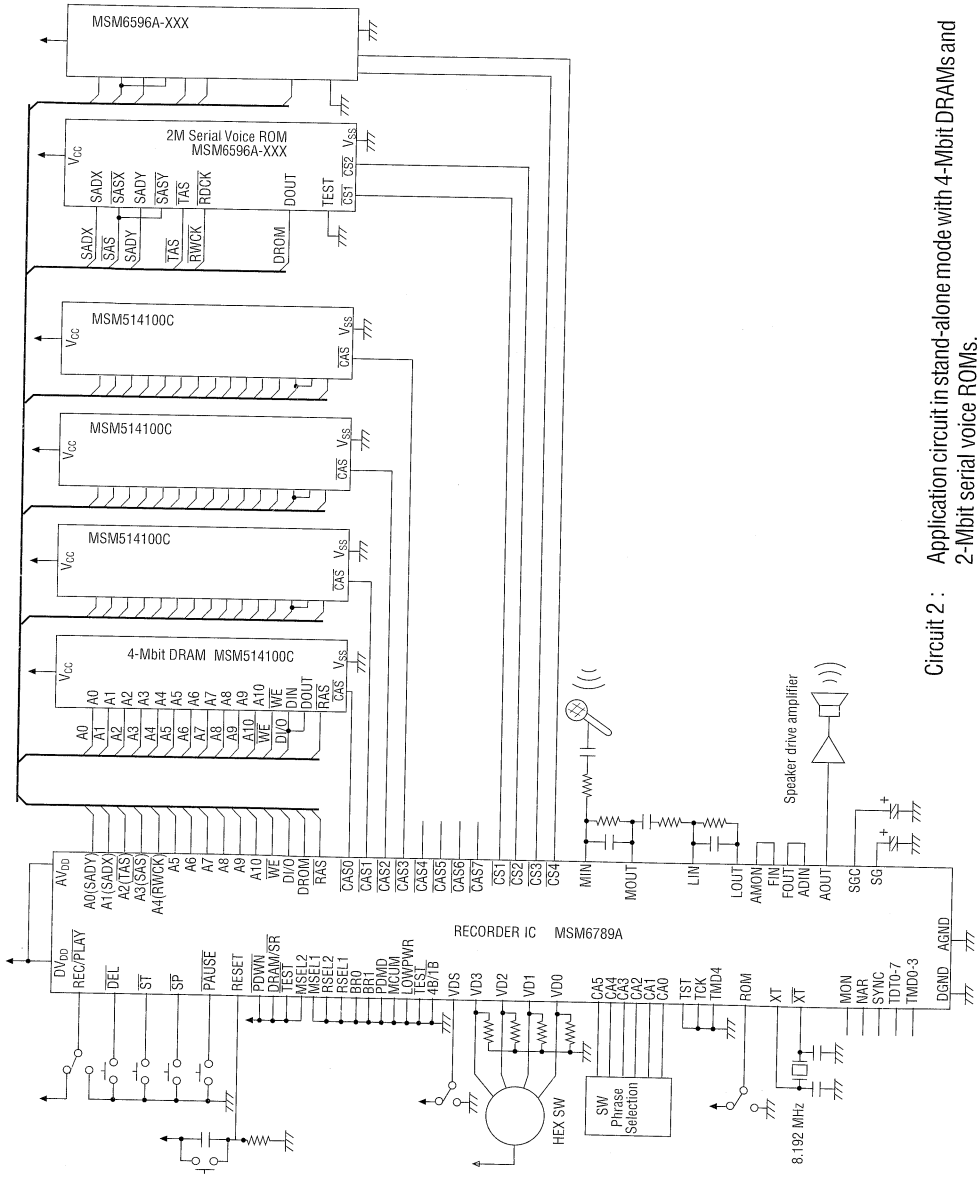
This is an application circuit example when the MSM6789A is used in stand-alone mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.



Circuit 1 : Application circuit in stand-alone mode with 8-Mbit serial registers and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

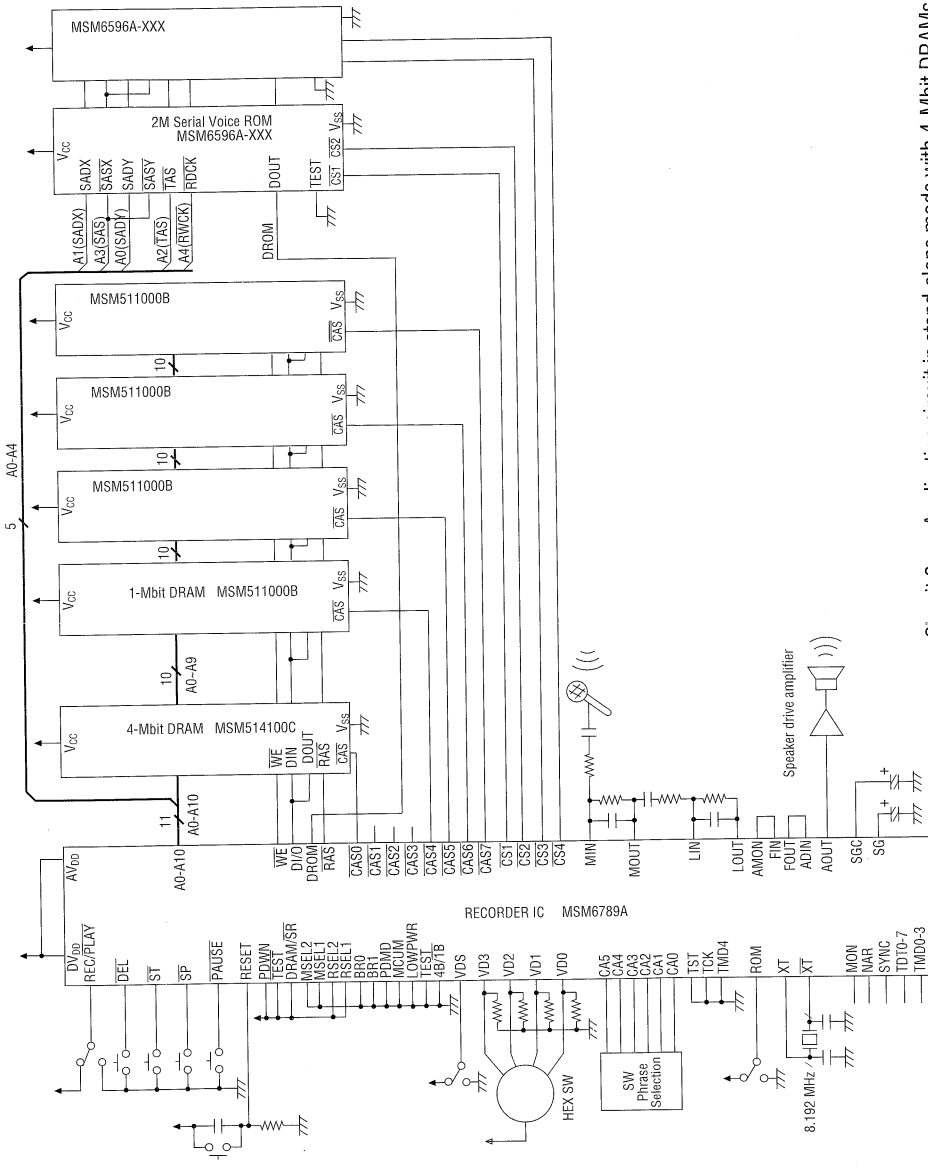
This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 2 : Application circuit in stand-alone mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

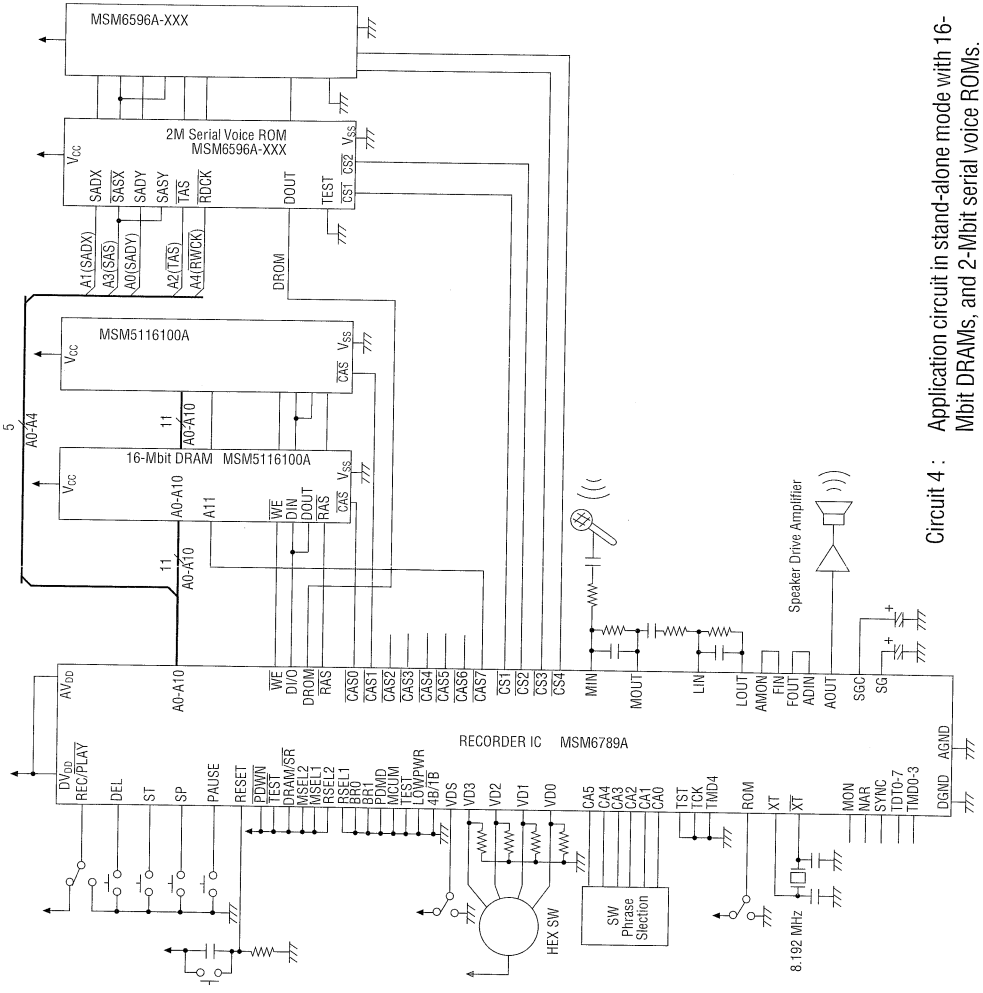
This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 3 : Application circuit in stand-alone mode with 4-Mbit DRAMs, 1-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

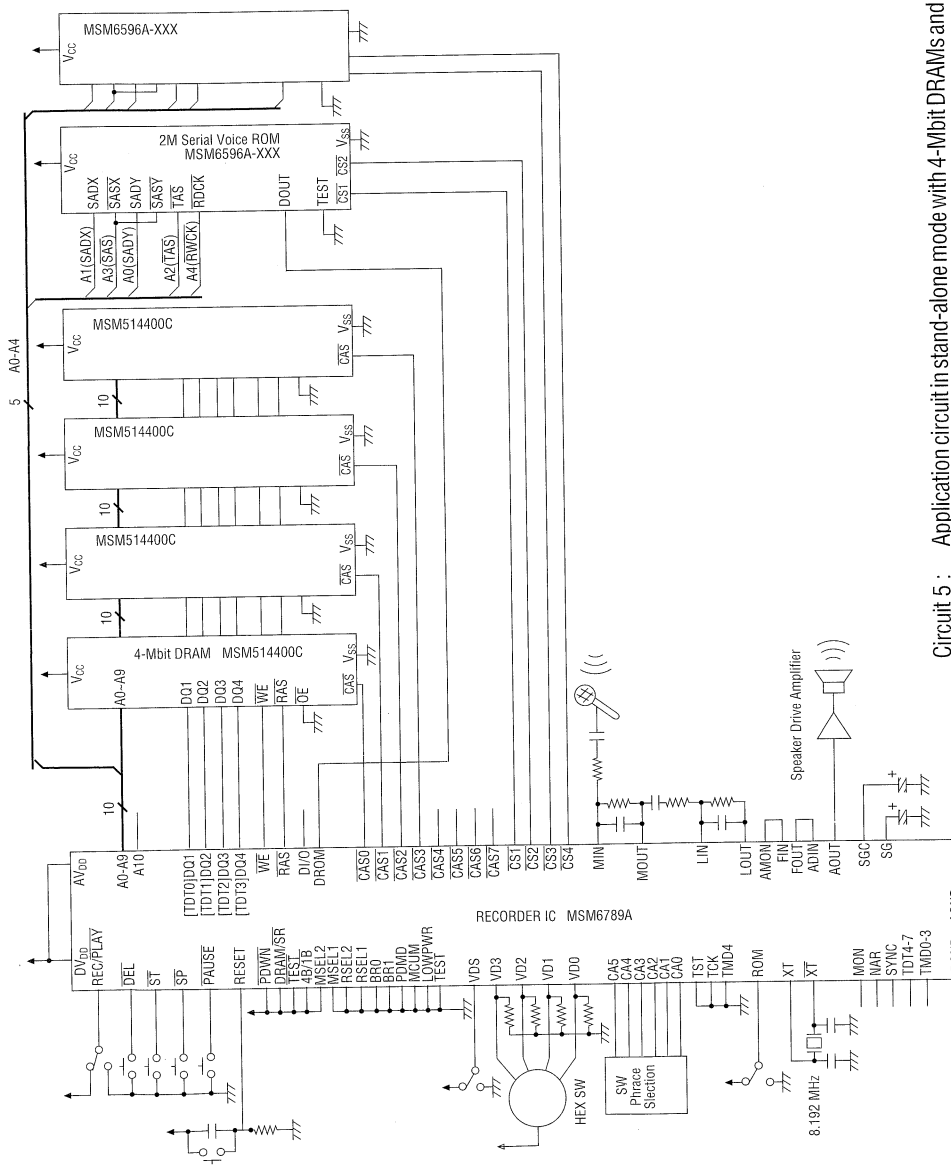
This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 4 : Application circuit in stand-alone mode with 16-Mbit DRAMs, and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

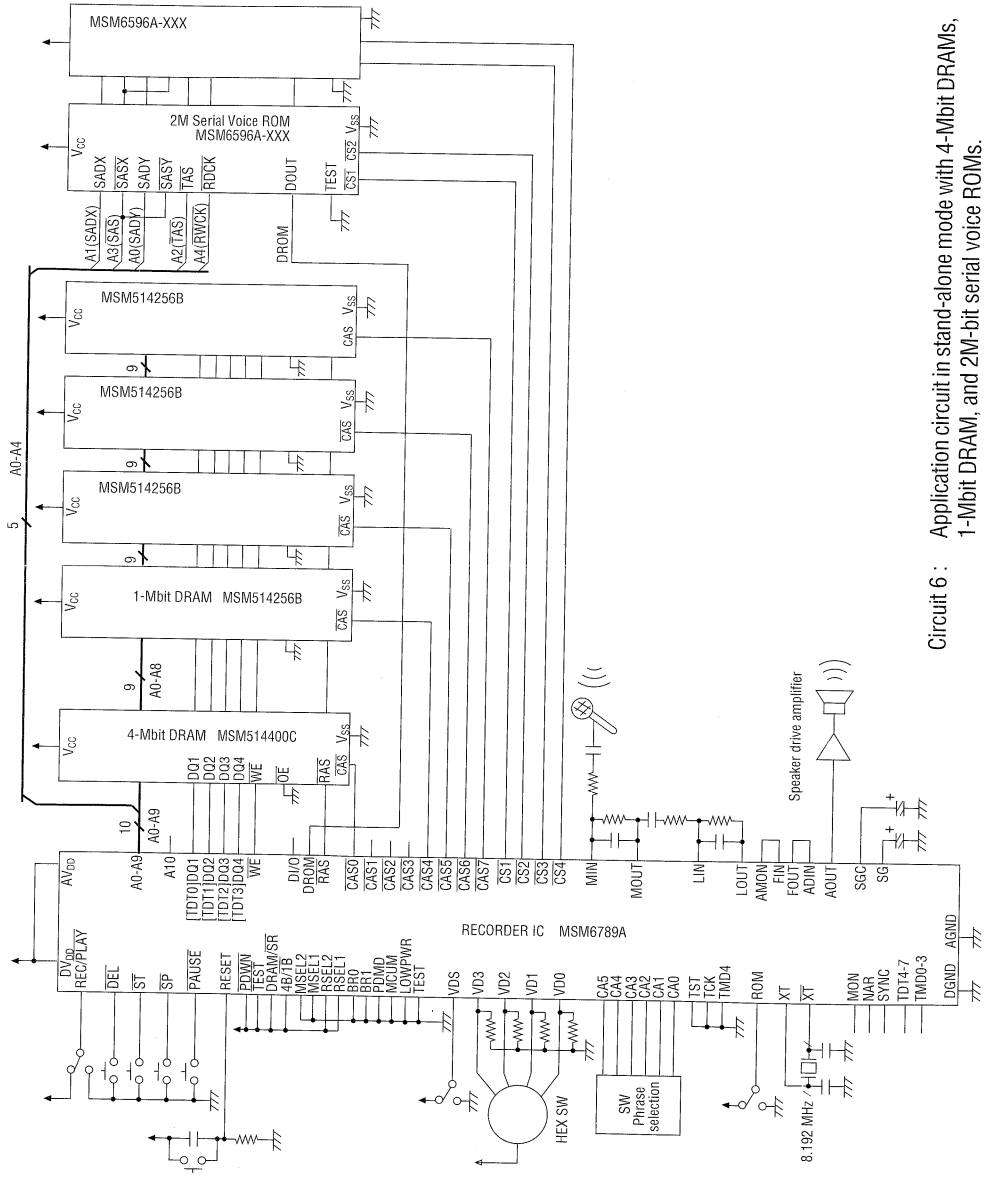
This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 5 : Application circuit in stand-alone mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

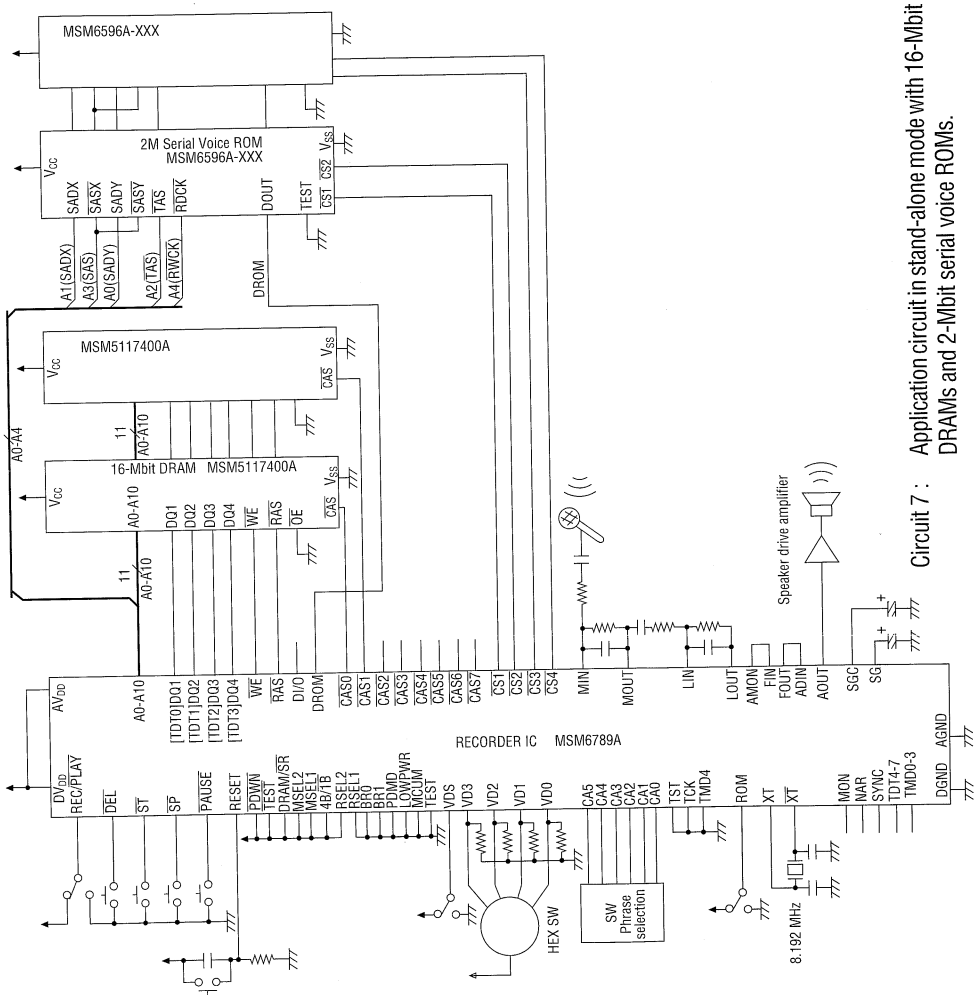
This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit × type), and two 2-Mbit serial voice ROMs.



Circuit 6 : Application circuit in stand-alone mode with 4-Mbit DRAMs, 1-Mbit DRAM, and 2M-bit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

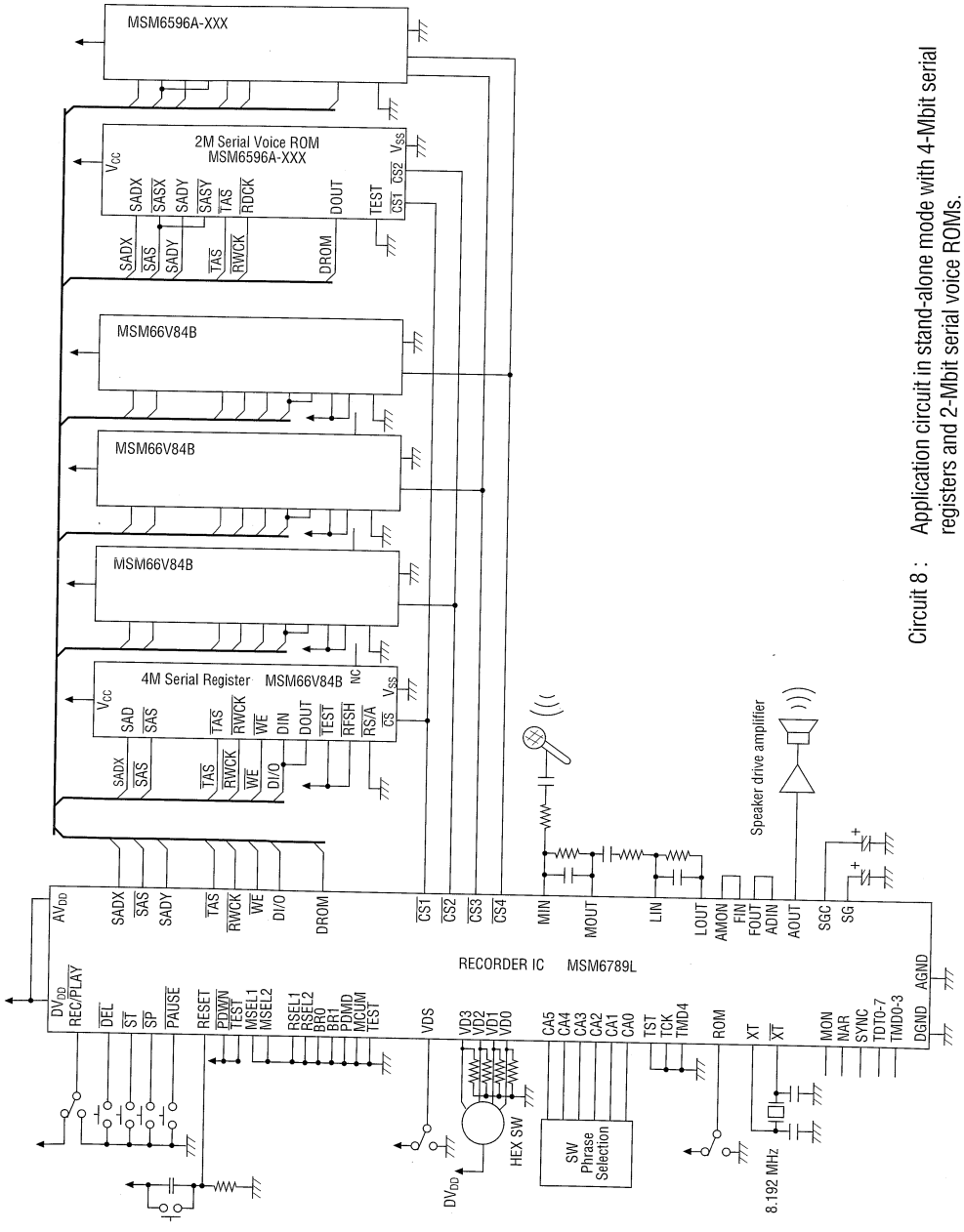
This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 7 : Application circuit in stand-alone mode with 16-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in stand-alone mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.



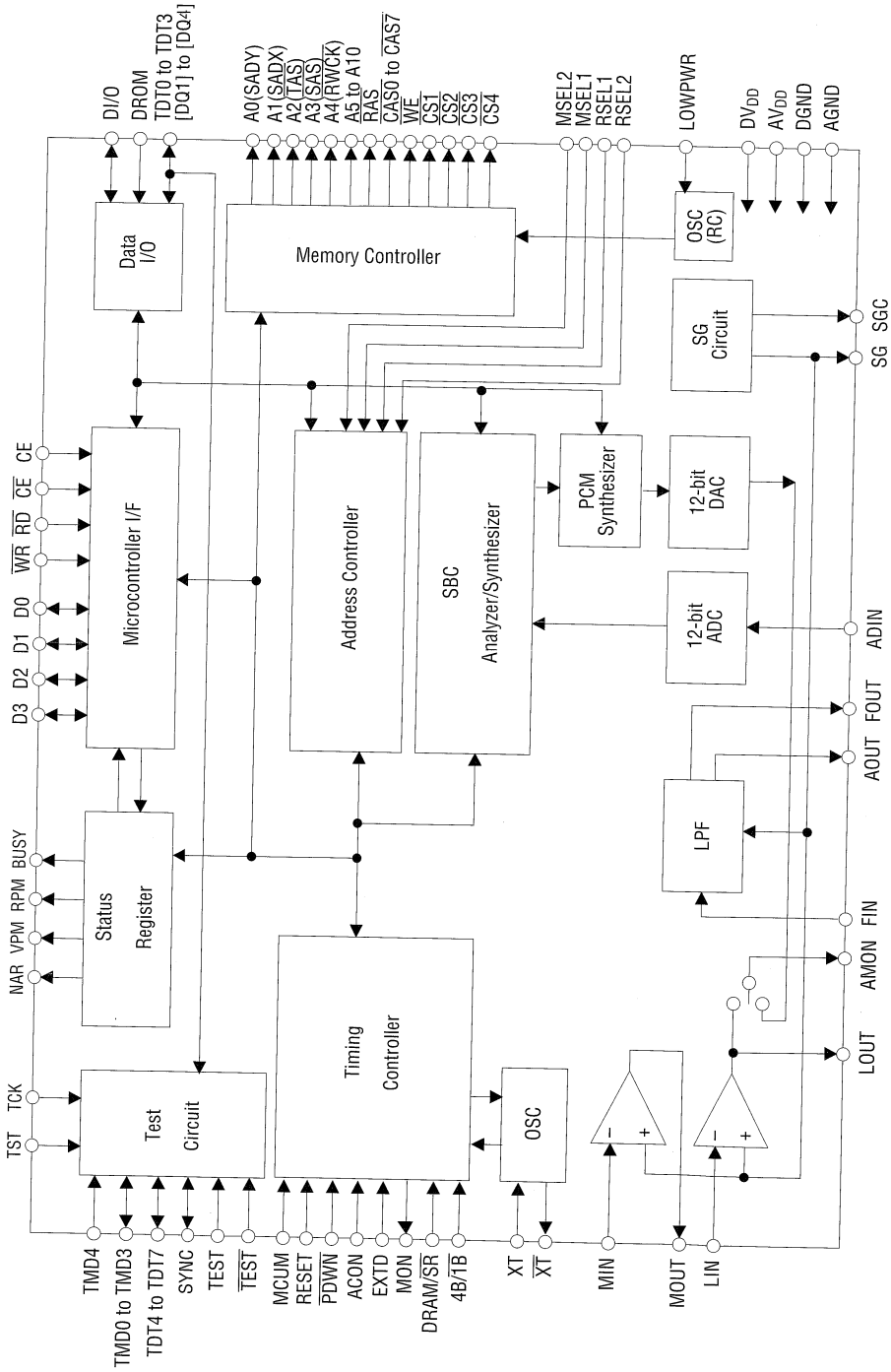
Circuit 8 : Application circuit in stand-alone mode with 4-Mbit serial registers and 2-Mbit serial voice ROMs.

MICROCONTROLLER INTERFACE MODE

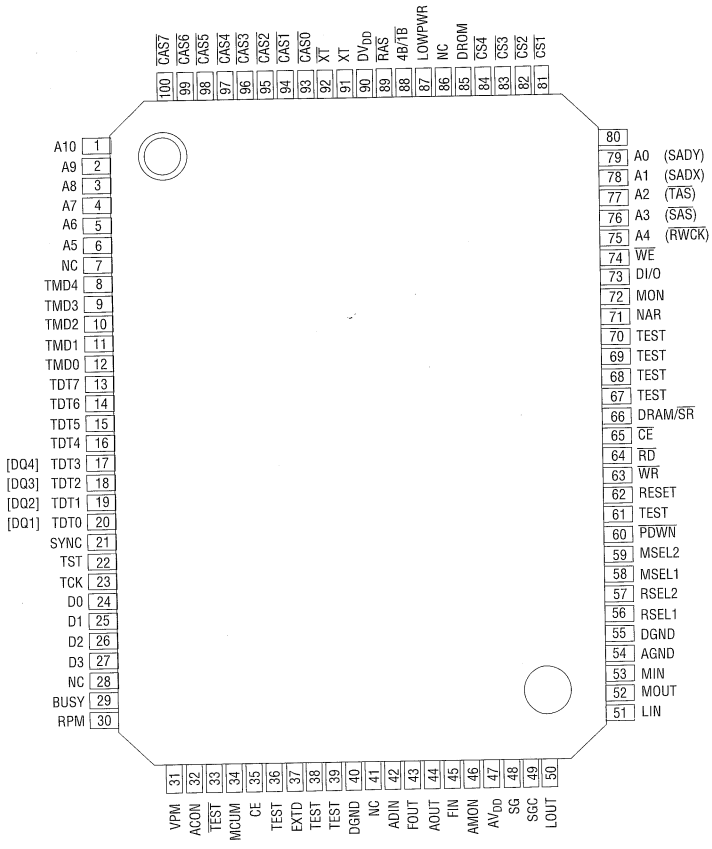
FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  MSM6789A (5 V version)
    General-purpose DRAM, 32 Mbits maximum (for variable messages)
      1-Mbit DRAM : Can be directly driven (MSM514256B, MSM511000B)
      4-Mbit DRAM : Can be directly driven (MSM514400C, MSM514100C)
      16-Mbit DRAM : Can be directly driven (MSM5117400A, MSM5116100A)
    ARAM, 32 Mbits maximum (for variable messages)
      Note: Use the first 64 Kbits with no failed bits for the ARAM.
    Serial register, 32 Mbits maximum (for variable messages)
      4-Mbit serial register : Can be directly driven (MSM6684B)
      8-Mbit serial register : Can be directly driven (MSM6685)
  MSM6789L (3.3 V version)
    Serial register, 16 Mbits maximum (for variable messages)
      4-Mbit serial register: Can be directly driven (MSM66V84B)
  MSM6789A (5 V version) and MSM6789L (3.3 V version)
    Serial voice ROM, 4 Mbits maximum (for fixed messages)
      1-Mbit serial voice ROM : Can be directly driven (MSM6595A)
      2-Mbit serial voice ROM : Can be directly driven (MSM6596A)
      3-Mbit serial voice ROM : Can be directly driven (MSM6597A)
- Bit rate
  10.0, 12.6, 16.0 kbps (at 8 kHz sampling freq.)
  7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)
- Maximum recording time (when one 8-Mbit serial register is connected)
  13.8 minutes (for 10.0 kbps SBC) 18.4 minutes (for 7.5 kbps SBC)
  11.0 minutes (for 12.6 kbps SBC) 14.6 minutes (for 9.5 kbps SBC)
  8.6 minutes (for 16.0 kbps SBC) 11.5 minutes (for 12.0 kbps SBC)
- Number of phrases
  63 phrases for variable messages
  255 phrases for fixed messages
- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Uuvoiced-part elimination function (voice detect level can be set)
- Pausing function
- Master clock frequency: 6.0 MHz to 8.192 MHz
- Power supply voltage:
  MSM6789A: Single 5 V power supply
  MSM6789L: Single 3.3 V power supply
- Package options:
  MSM6789A: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK)
  MSM6789L: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

( ) : Pins for connecting serial voice ROM.
[ ] : Pins for connecting 4-bit × type DRAM.
NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	O	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
66	DRAM/$\overline{SR}$	I	This pin selects whether memory to be connected externally is DRAM or serial register. Low level : Serial register High level : DRAM
88	4B/$\overline{1B}$	I	This pin selects either 1-bit × type DRAM or 4-bit × type DRAM. Low level : 1-bit × type High level : 4-bit × type
79 78	A0 (SADY) A1 (SADX)	O	These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also connect to SAD pin of serial register and serial voice ROM at the time of serial register selection. These pins output leading addresses of read/write.
77	A2 ($\overline{TAS}$)	O	This pin connects to A2 of DRAM at the time of DRAM selection. It also connects to $\overline{TAS}$ pin of serial register and serial voice ROM at the time of serial register selection. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	A3 ($\overline{SAS}$)	O	This pin connects to A3 of DRAM at the time of DRAM selection. It also connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM at the time of serial register selection. Clock pin to write serial addresses.
75	A4 ($\overline{RWCK}$)	O	This pin connects to A4 of DRAM at the time of DRAM selection. It also connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM at the time of serial register selection. Clock pin to read data from and write data into the serial register.
1-6	A10-A5	O	These pins connect to pins A5-A10 of DRAM at the time of DRAM selection. These pins output addresses of read/write.

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

Pin	Symbol	Type	Description
74	$\overline{WE}$	O	**Write Enable.** This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	I/O	**Data I/O.** This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin is used to output write data and inputs read data.
85	DROM	I	**Data ROM.** This pin connects to the DOUT pin of the serial voice ROM.
89	$\overline{RAS}$	O	This is a row address strobe pin of DRAM at the time of DRAM selection.
93-100	$\overline{CAS0}$-$\overline{CAS7}$	O	These are the column address strobe pins of DRAM at the time of DRAM selection. CAS7, an addresss output pin, is connected to pin A11 of DRAM at the time of 16-Mbit DRAM selection.
81 82 83 84	$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	**Chip Slect.** These pins connect $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.
58 59	MSEL1 MSEL2	I I	These pins select the capacity of the memory to be connected externally.
56 57	RSEL1 RSEL2	I I	These pins select the number of DRAMs and serial registers to be connected externallly. • When DRAM is selected (DRAM/$\overline{SR}$ = High level)

MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity
L	L	L	L	1M × 4
L	L	L	H	4M × 1
L	L	H	L	1M × 8
L	L	H	H	1M × 4 + 4M × 1
L	H	L	L	4M × 2
L	H	L	H	4M × 2
L	H	H	L	4M × 3
L	H	H	H	4M × 3
H	L	L	L	4M × 4
H	L	L	H	16M × 1
H	L	H	L	4M × 6
H	L	H	H	4M × 6
H	H	L	L	4M × 8
H	H	L	H	4M × 8
H	H	H	L	16M × 2
H	H	H	H	16M × 2

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>• When serial register is selected (DRAM/$\overline{SR}$ = Low level)
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M × 4</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>8M × 1</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>8M × 2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>8M × 3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>8M × 4</td></tr>
</table></td></tr>
<tr><td>87</td><td>LOWPWR</td><td>I</td><td>This pin selects $\overline{CAS}$-before-$\overline{RAS}$ refresh period of DRAM at the time of power down when DRAM is selected.
Low level : 15 µs max.
High level : 125 µs max.</td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789A to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{PDWN}$</td><td>I</td><td>Power Down. When a low level is input the MSM6789A goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789A to be reset.
When an Low level is applied to this pin during recording operation, the MSM6789A is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low level.
After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>24
25
26
27</td><td>D0
D1
D2
D3</td><td>I/O</td><td>Bidirectional data bus to transfer commands and data to and from an external microcontroller.</td></tr>
<tr><td>63</td><td>$\overline{WR}$</td><td>I</td><td>Write Pulse Input. Inputting a low pulse to $\overline{WR}$ pin causes a command or data to be input via D0 to D3 pins.</td></tr>
<tr><td>64</td><td>$\overline{RD}$</td><td>I</td><td>Read Pulse Input. Inputting a low pulse to $\overline{RD}$ pin causes status bits or data to be output via D0 to D3 pins.</td></tr>
<tr><td>65
35</td><td>$\overline{CE}$
CE</td><td>I</td><td>Chip Enable Input. When the $\overline{CE}$ pin is set to low level and the CE pin is set to a high level, the write pulse ($\overline{WR}$) or read pulse ($\overline{RD}$) can be accepted.
When the $\overline{CE}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{WR}$) and read pulse ($\overline{RD}$) cannot be accepted so that data cannot be communicated via D0 to D3 pins.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

Pin	Symbol	Type	Description
29	BUSY	O	**Busy.** This pin outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0 to D3 pins. The state of this pin is the same as the contents of the BUSY bit of the status register.
30	RPM	O	**RPM.** This pin outputs a high level during recording or playback operation. The state of this pin is the same as the contents of the RPM bit of the status register.
31	VPM	O	**VPM.** This pin outputs a high level during standby for voice incoming after the start of recording by voice triggered starting or unvoiced-part elimination. Also outputs a high level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.
71	NAR	O	**NAR.** This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.
32	ACON	I	**POP Noise Suppression Select.** This pin selects whether the pop noise suppression circuit is used. Low level : the pop noise suppression circuit is not used. High level : the pop noise suppression circuit is used. The DC level is shifted by the LEV command.
37	EXTD	I	**EXTD.** In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
91	XT	I	**Oscillator Connect.** When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.
92	$\overline{XT}$	O	**Oscillator Connect.** When an external clock is uesd, this pin must be left open.
72	MON	O	**MON.** This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
36, 37-39, 61, 67-70	TEST	I	**MSM6789A Test.** Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.
33	$\overline{TEST}$		
9-12	TMD3-TMD0	I/O	**MSM6789A Test.** This pin must be left open.
13-20	TDT7-TDT0		
21	SYNC		
17-20	TDT3-TDT0 [DQ4]-[DQ1]	I/O	Connect these pins to DQ1 to DQ4 of DRAM at the time of 4-bit × type DRAM selection. Otherwise these pins must be left open as they are MSM6789A test pins.
22	TST	I	**MSM6789A Test.** Input a low level.
23	TCK		
8	TMD4		

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	−0.3 ~ V_{DD} +0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.5 to +5.5*3	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5 V*3
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.8×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=−40 µA	V_{DD}−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current*1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current*2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input current*1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
Low input current*2	I_{IL2}	V_{IL}=GND	−20	—	—	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

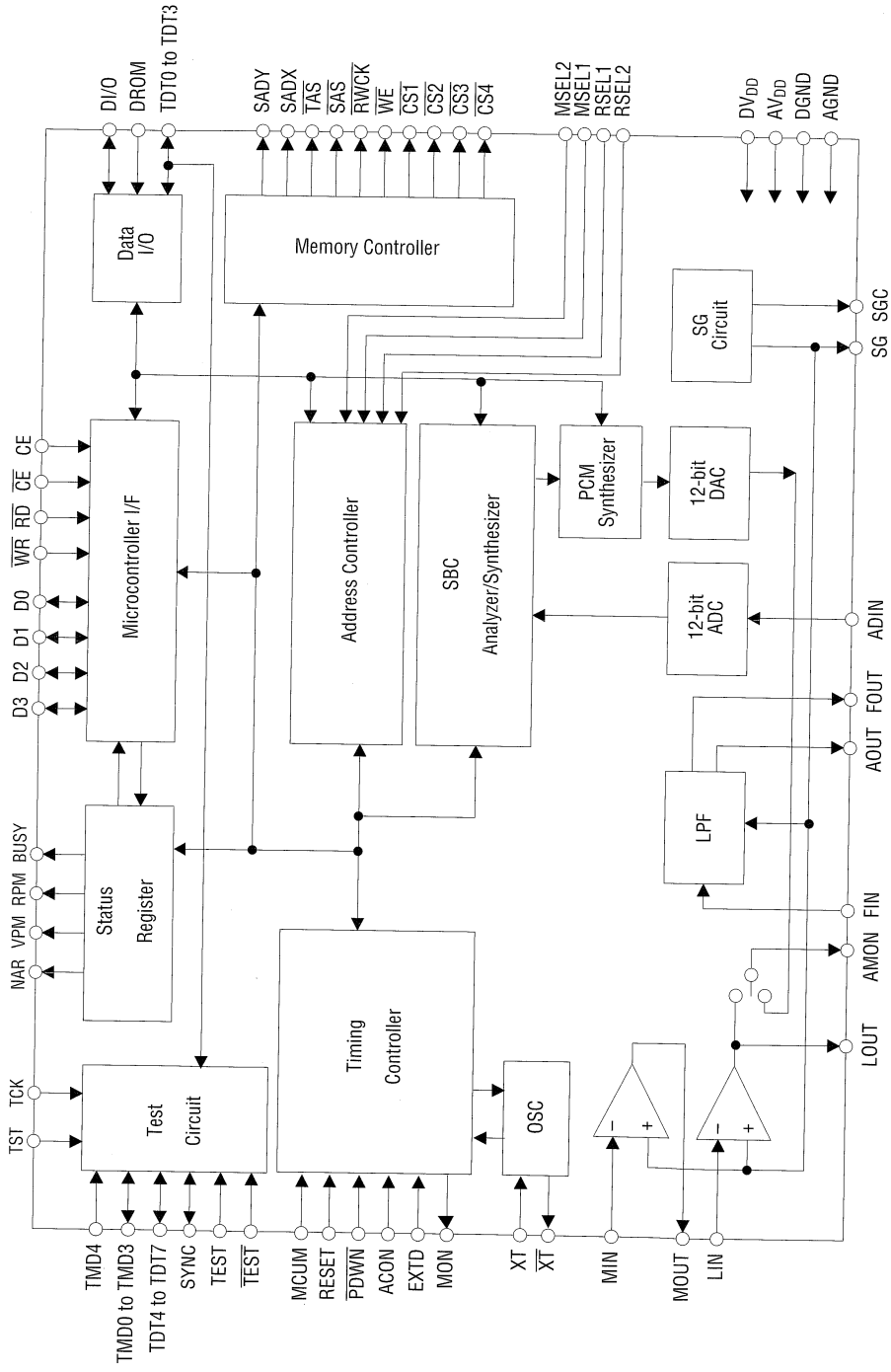
*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.
*3 The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

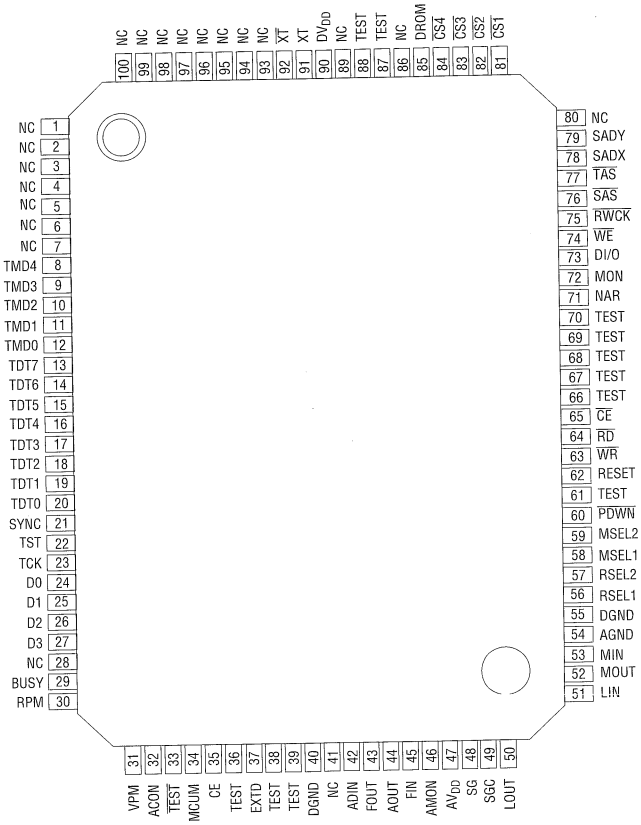
DV_{DD}=AV_{DD}=4.5 to 5.5 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	No load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	V_{DD}–1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
OP-amp open loop gain	G_{OP}	f_{IN}=0 to 4 kHz	40	—	—	dB
OP-amp input impedance	R_{INA}	—	1	—	—	MΩ
OP-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3V Version))



100-Pin Plastic QFP

NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	O	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
79 78	SADY SADX	O	These pins connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write.
77	$\overline{TAS}$	O	This pin connects to $\overline{TAS}$ pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	$\overline{SAS}$	O	This pin connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM. Clock pin to write serial addresses.
75	$\overline{RWCK}$	O	This pin connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM. Clock pin to read data from and write data into the serial register.
74	$\overline{WE}$	O	**Write Enable.** This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	I/O	**Data I/O.** This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin is used to output write data and inputs read data.
85	DROM	I	**Data ROM.** This pin connects to the DOUT pin of the serial voice ROM.
81 82 83 84	$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	**Chip Slect.** These pins connect $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.
58 59	MSEL1 MSEL2	I I	These pins select the capacity of the memory to be connected externally.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>These pins select the number of serial registers to be connected externallly.
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M × 4</td></tr>
</table></td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789L to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{\text{PDWN}}$</td><td>I</td><td>Power Down. When a low level is input the MSM6789L goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789L to be reset.
When an Low level is applied to this pin during recording operation, the MSM6789L is halted, and will be maintained in the power down state while $\overline{\text{PDWN}}$ is low level.
After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>24
25
26
27</td><td>D0
D1
D2
D3</td><td>I/O</td><td>Bidirectional data bus to transfer commands and data to and from an external microcontroller.</td></tr>
<tr><td>63</td><td>$\overline{\text{WR}}$</td><td>I</td><td>Write Pulse Input. Inputting a low pulse to $\overline{\text{WR}}$ pin causes a command or data to be input via D0 to D3 pins.</td></tr>
<tr><td>64</td><td>$\overline{\text{RD}}$</td><td>I</td><td>Read Pulse Input. Inputting a low pulse to $\overline{\text{RD}}$ pin causes status bits or data to be output via D0 to D3 pins.</td></tr>
<tr><td>65
35</td><td>$\overline{\text{CE}}$
CE</td><td>I</td><td>Chip Enable Input. When the $\overline{\text{CE}}$ pin is set to low level and the CE pin is set to a high level, the write pulse ($\overline{\text{WR}}$) or read pulse ($\overline{\text{RD}}$) can be accepted.
When the $\overline{\text{CE}}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{\text{WR}}$) and read pulse ($\overline{\text{RD}}$) cannot be accepted so that data cannot be communicated via D0 to D3 pins.</td></tr>
<tr><td>29</td><td>BUSY</td><td>O</td><td>Busy. This pin outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0 to D3 pins. The state of this pin is the same as the contents of the BUSY bit of the status register.</td></tr>
<tr><td>30</td><td>RPM</td><td>O</td><td>RPM. This pin outputs a high level during recording or playback operation. The state of this pin is the same as the contents of the RPM bit of the status register.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

Pin	Symbol	Type	Description
31	VPM	O	**VPM.** This pin outputs a high level during standby for voice incoming after the start of recording by voice triggered starting or unvoiced-part elimination. Also outputs a high level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.
71	NAR	O	**NAR.** This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.
32	ACON	I	**POP Noise Suppression Select.** This pin selects whether the pop noise suppression circuit is used. Low level : the pop noise suppression circuit is not used. High level : the pop noise suppression circuit is used. The DC level is shifted by the LEV command.
37	EXTD	I	**EXTD.** In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
91	XT	I	**Oscillator Connect.** When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.
92	$\overline{XT}$	O	**Oscillator Connect.** When an external clock is uesd, this pin must be left open.
72	MON	O	**MON.** This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
36, 37-39, 61, 67-70 33	TEST $\overline{TEST}$	I	**MSM6789L Test.** Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.
9-12 13-20 21	TMD3-TMD0 TDT7-TDT0 SYNC	I/O	**MSM6789L Test.** This pin must be left open.
17-20	TDT3-TDT0	I/O	These pins must be left open as they are MSM6789L test pins.
22 23 8	TST TCK TMD4	I	**MSM6789L Test.** Input a low level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	−0.3 ~ V_{DD} +0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=3.0 to 3.6 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.85×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.15×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=−40 µA	V_{DD}−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current*1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current*2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input current*1	I_{IL1}	V_{IL}=GND	−10	—	—	µA
Low input current*2	I_{IL2}	V_{IL}=GND	−20	—	—	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.

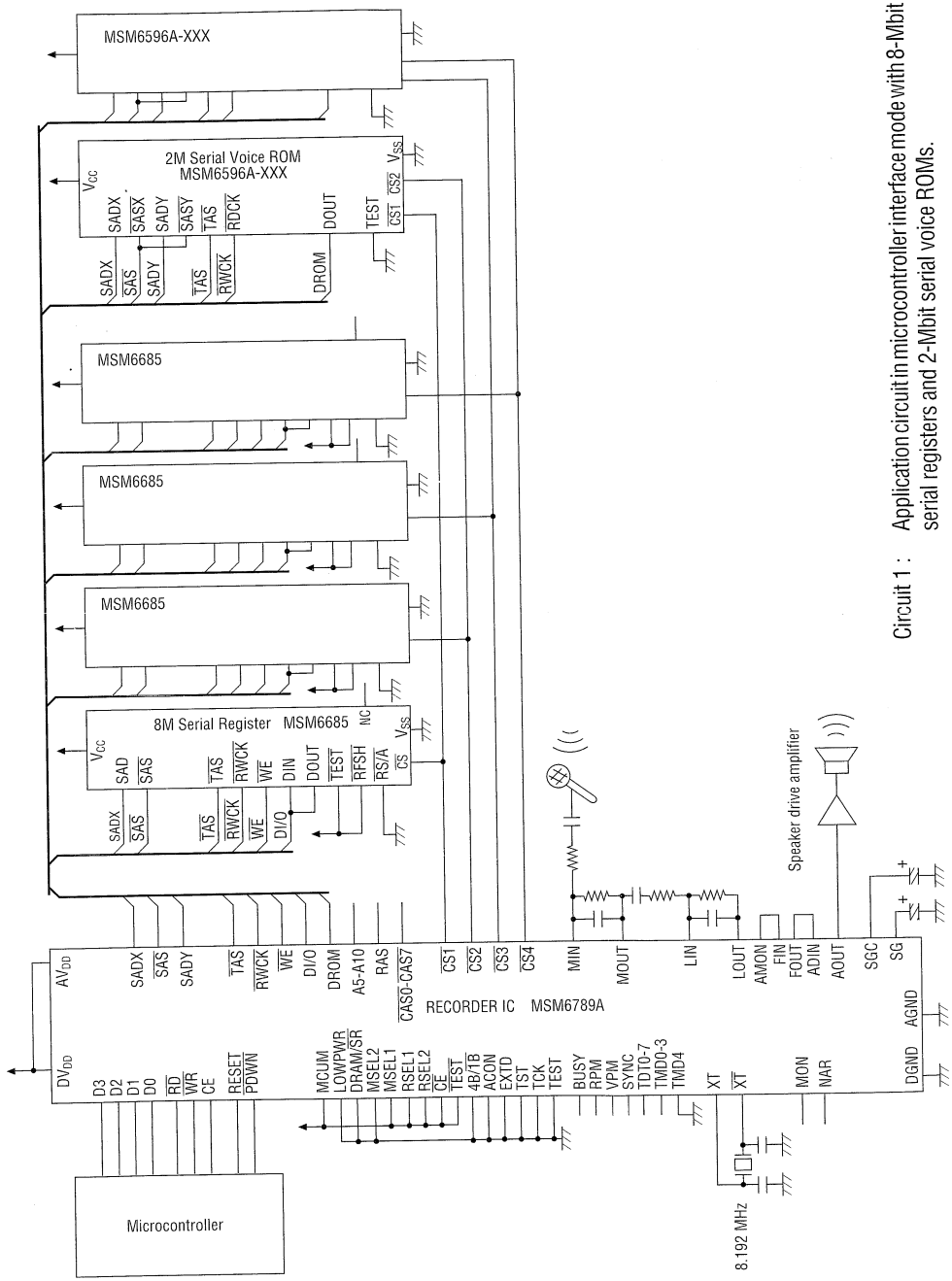
Analog Characteristics

$DV_{DD}=AV_{DD}=3.0$ to 3.6 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	No load	—	—	20	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	$V_{DD}-1$	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
OP-amp open loop gain	G_{OP}	f_{IN}=0 to 4 kHz	40	—	—	dB
OP-amp input impedance	R_{INA}	—	1	—	—	MΩ
OP-amp load resistance	R_{OUTA}	—	400	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	100	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	100	—	—	kΩ

APPLICATION CIRCUITS (for MSM6789A (5 V Version))

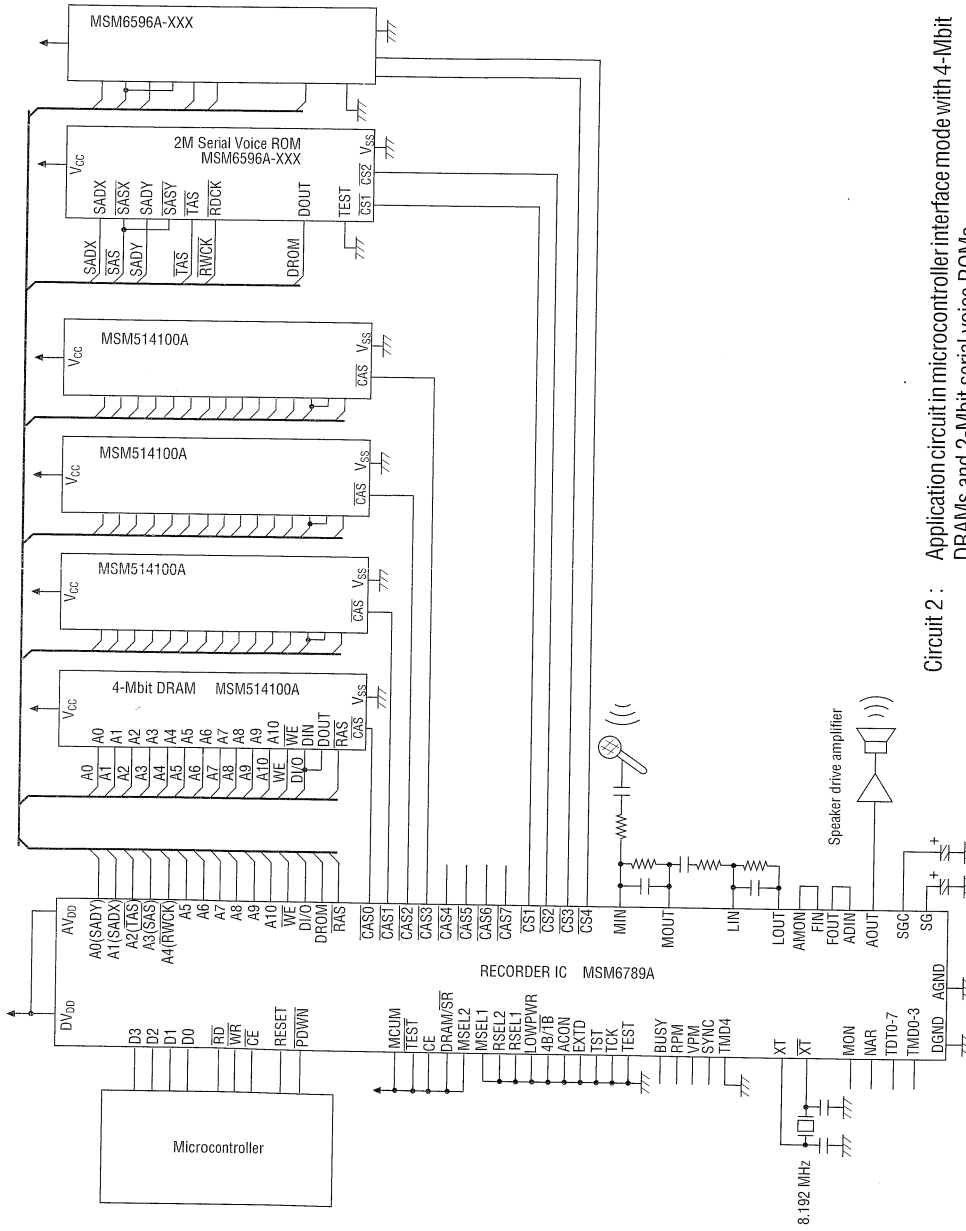
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.



Circuit 1 : Application circuit in microcontroller interface mode with 8-Mbit serial registers and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

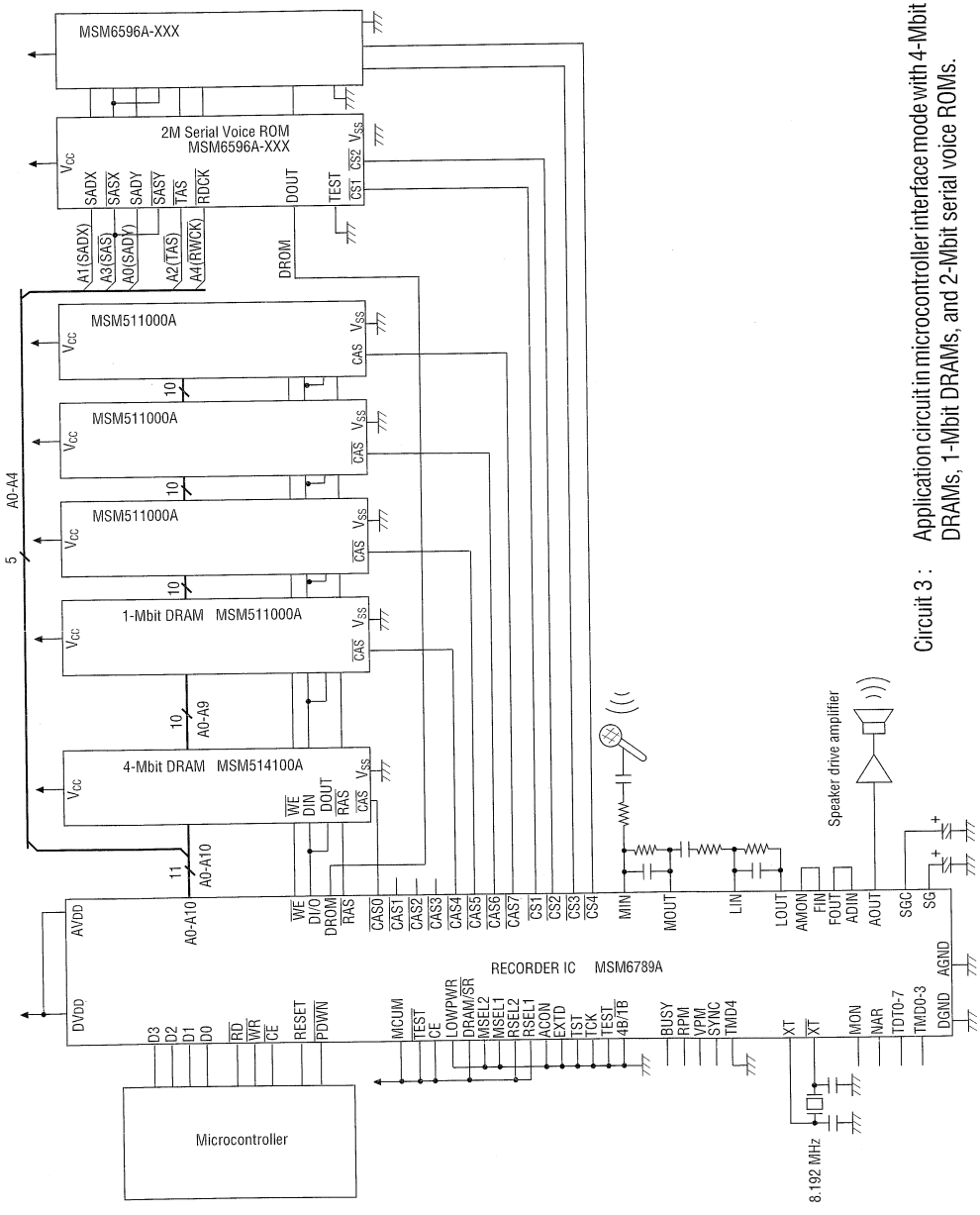
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 2 : Application circuit in microcontroller interface mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

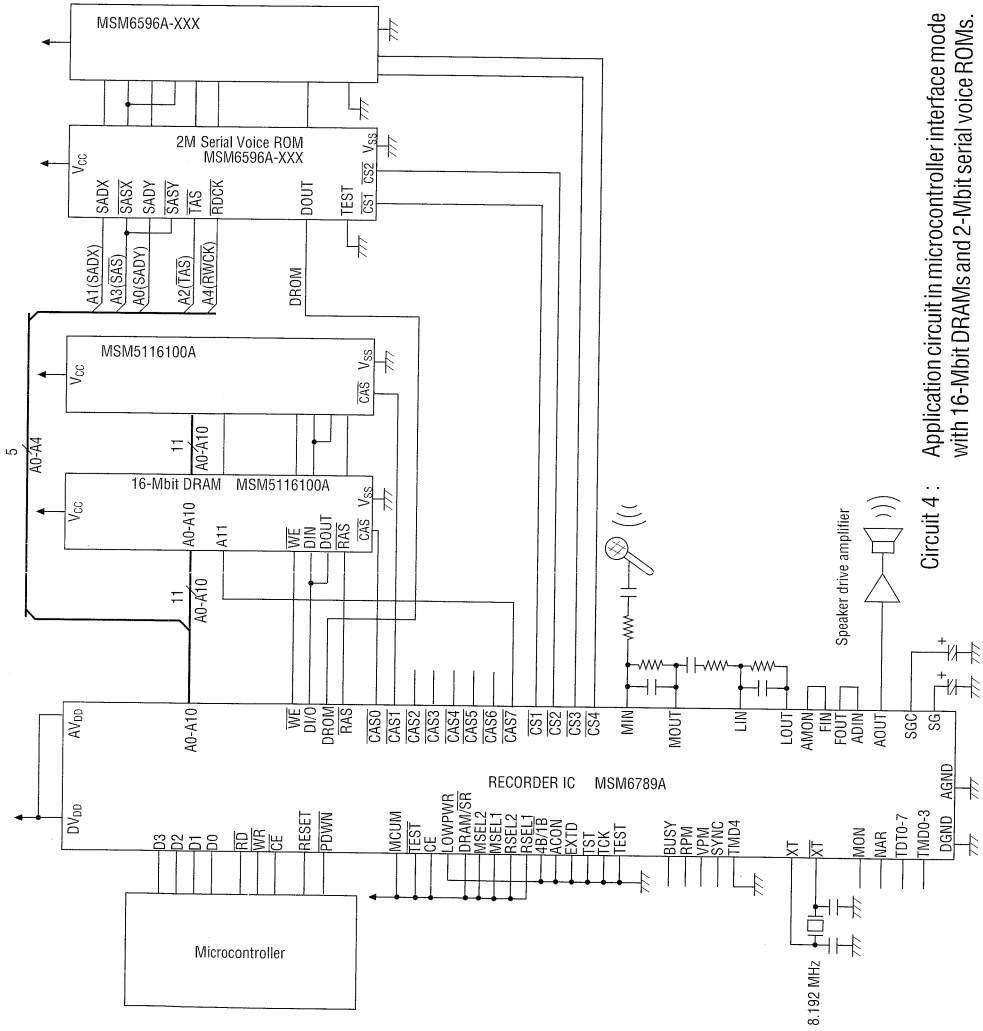
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit × type), and two 2-Mbit serial voice ROMs.



Circuit 3 : Application circuit in microcontroller interface mode with 4-Mbit DRAMs, 1-Mbit DRAMs, and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

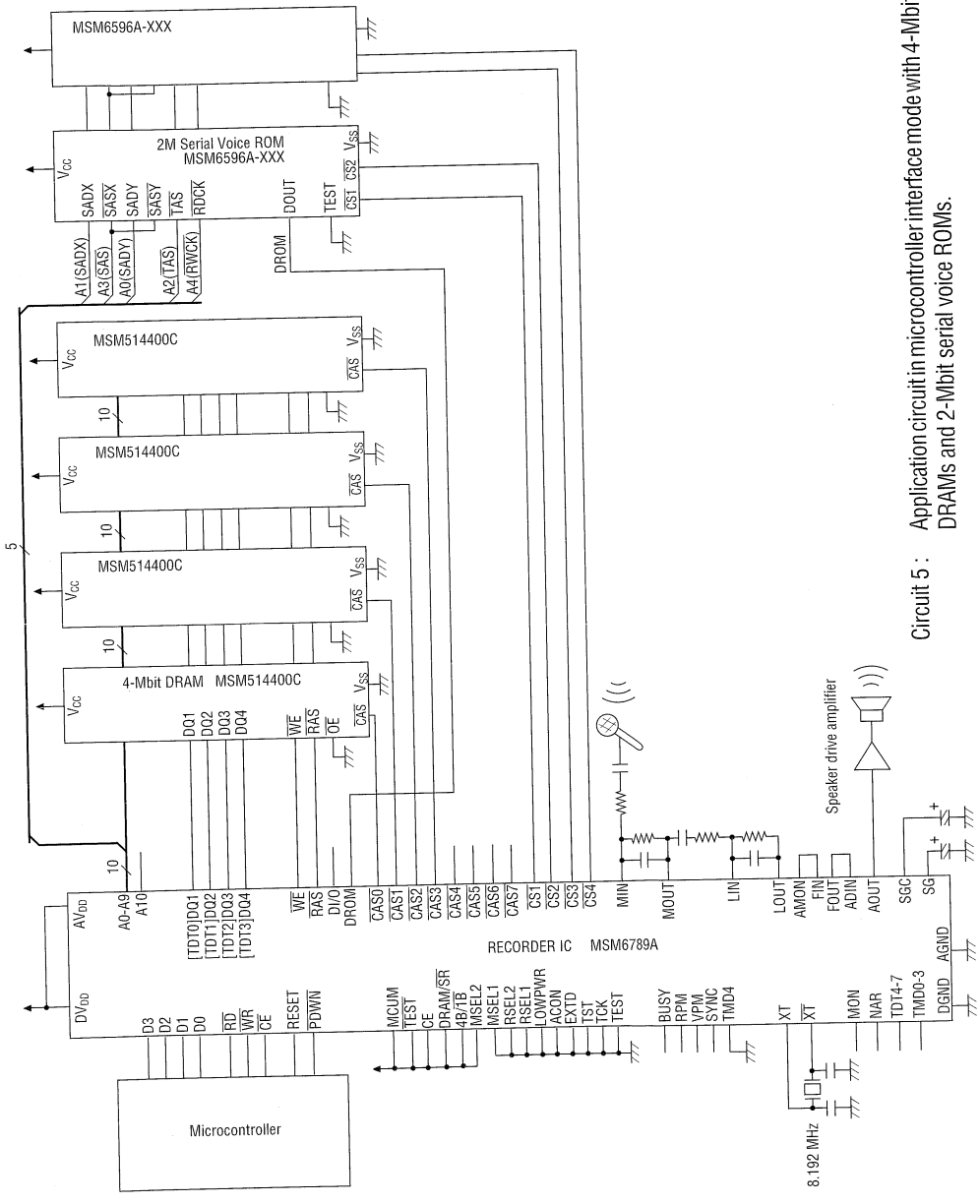
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 4 : Application circuit in microcontroller interface mode with 16-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

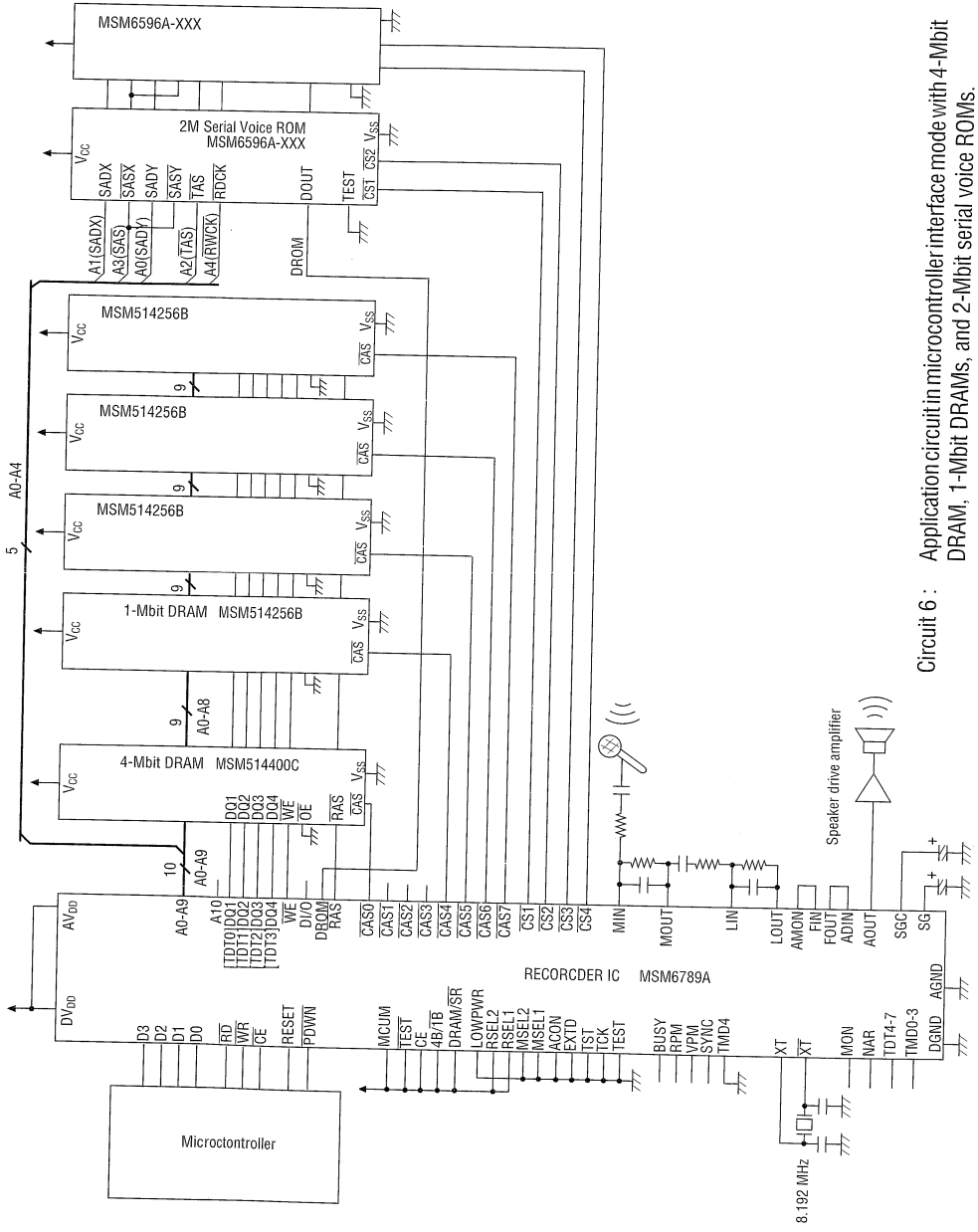
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 5 : Application circuit in microcontroller interface mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

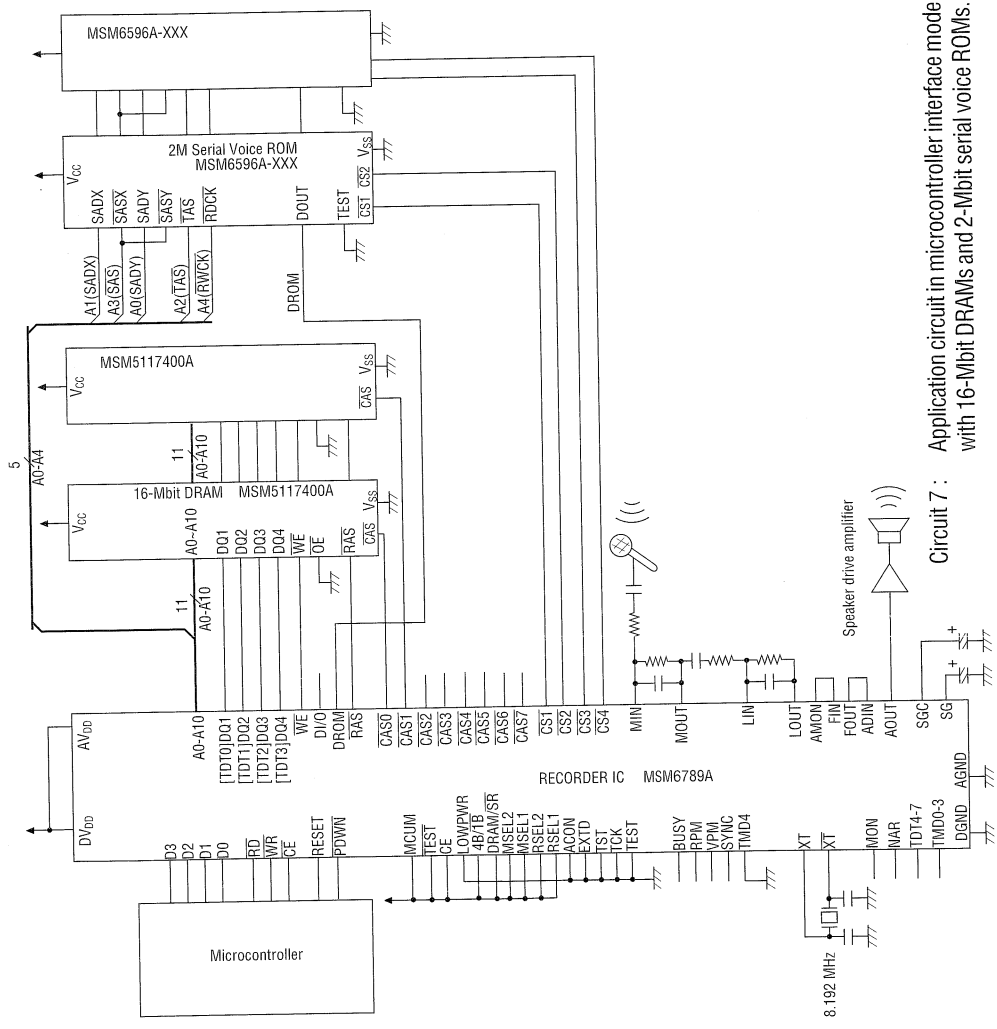
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit × type), and two 2-Mbit serial voice ROMs.



Circuit 6 : Application circuit in microcontroller interface mode with 4-Mbit DRAM, 1-Mbit DRAMs, and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

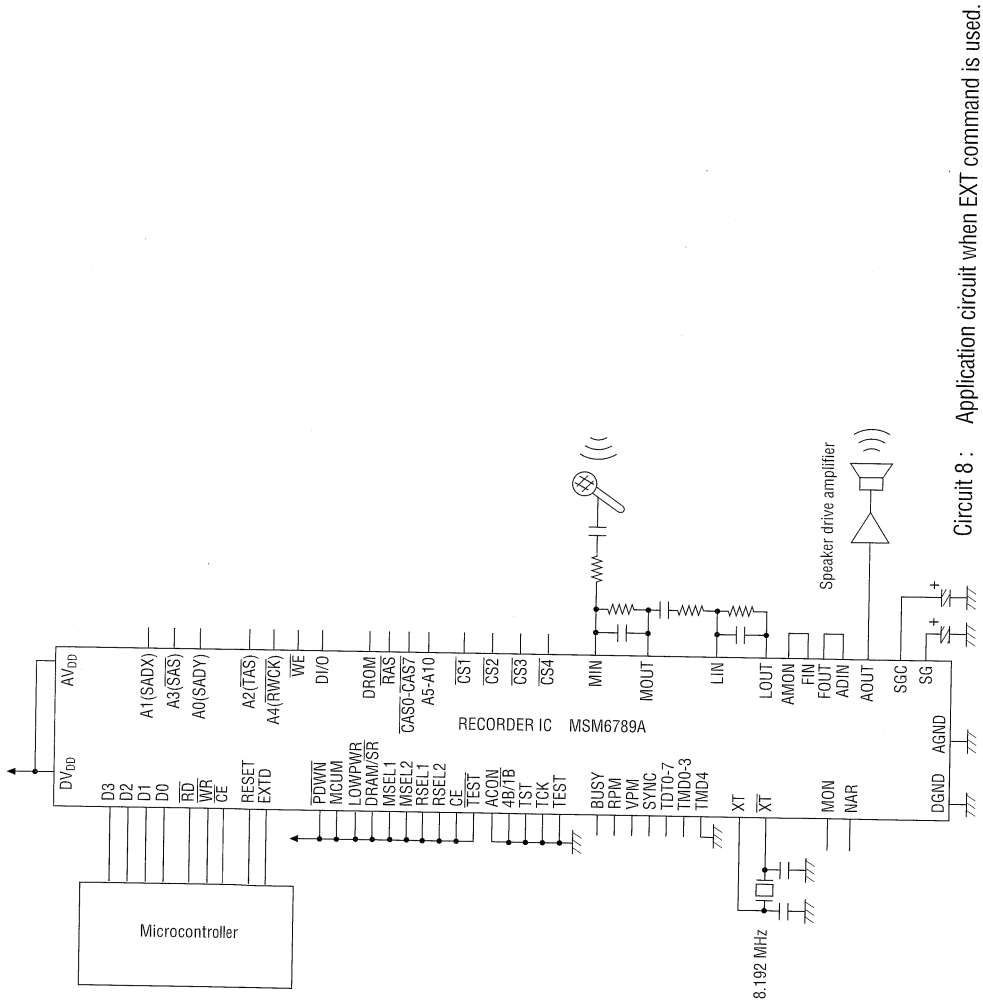
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 7 : Application circuit in microcontroller interface mode with 16-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

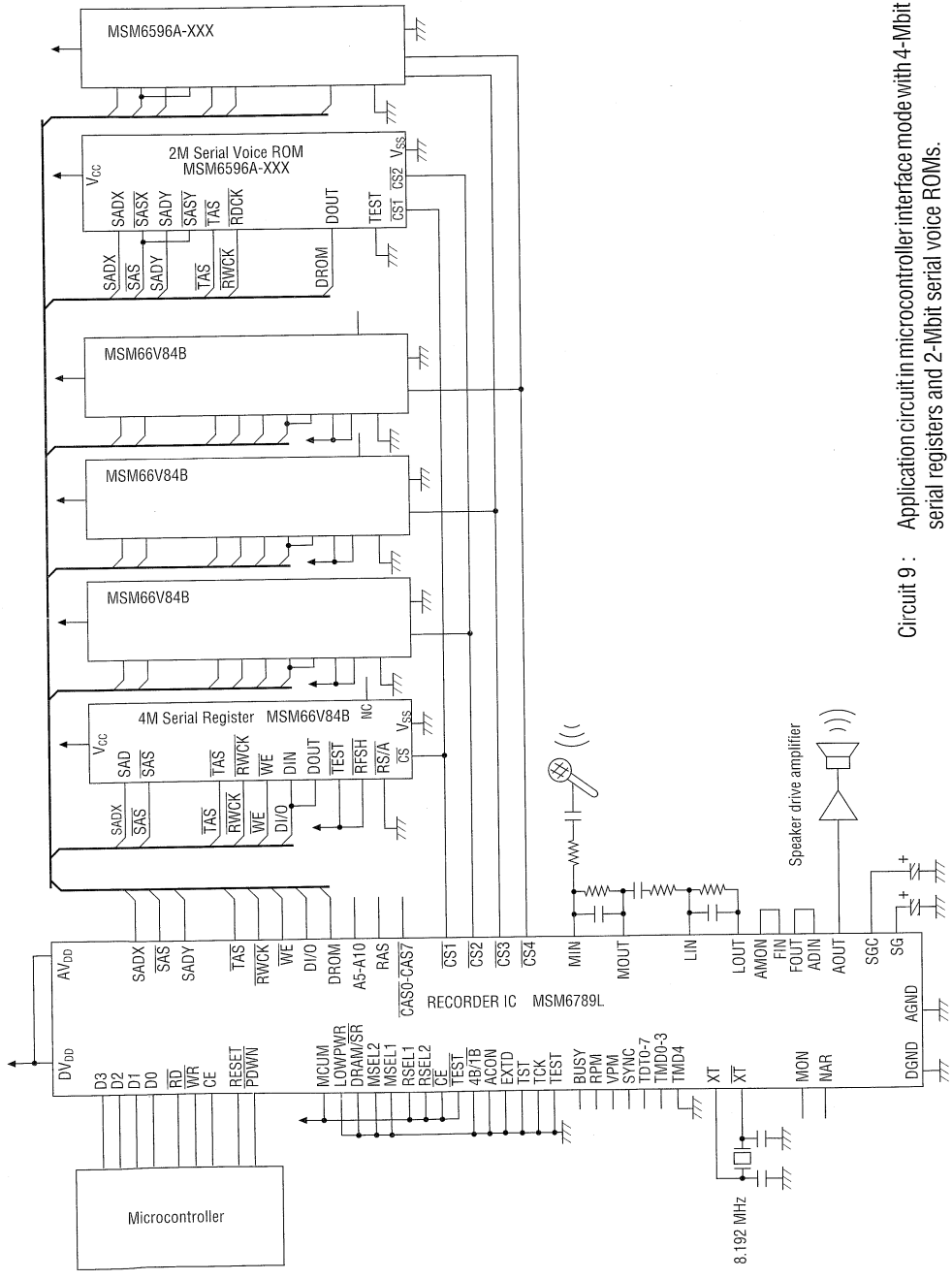
This is an application circuit example when the EXT command is used for recording/playback.



Circuit 8 : Application circuit when EXT command is used.

APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in microcontroller interface mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.



Circuit 9 : Application circuit in microcontroller interface mode with 4-Mbit serial registers and 2-Mbit serial voice ROMs.

Preliminary

OKI Semiconductor

MSM9841

Recording and Playback LSI with Built-in FIFO

GENERAL DESCRIPTION

The MSM 9841 is a recording and playback LSI with built-in FIFO memory.

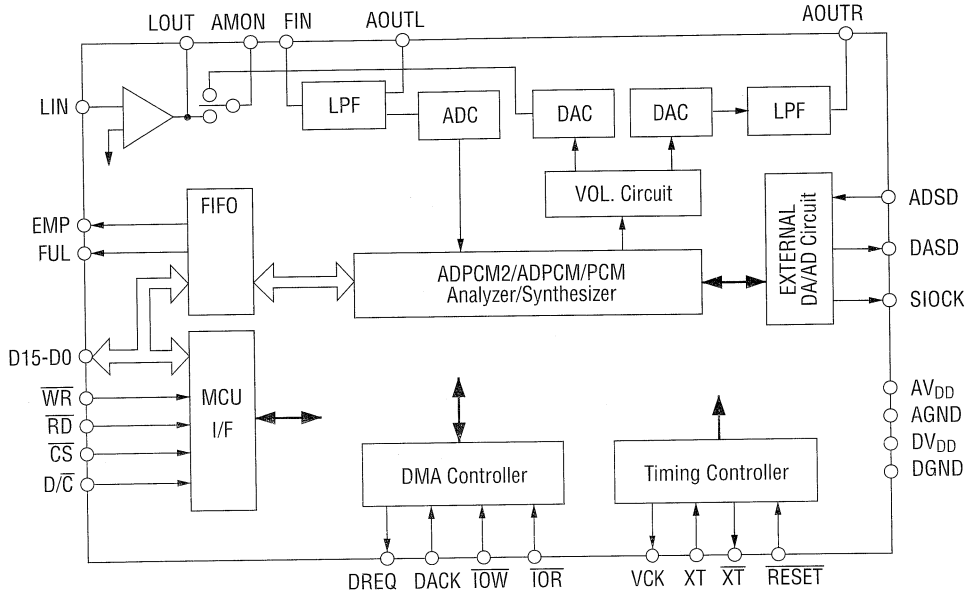
The MSM 9841 is based on the new OKI ADPCM2 system, which implements high sound quality, and recording and playback are controlled by a CPU via a 16/8-bit bus interface.

The MSM 9841 is a voice LSI which is most appropriate for systems which do not use semiconductor memory as the storage medium.

FEATURES

- 16/8-bit bus interface support
- FIFO capacity : 512-bits
  (buffering time of 16 ms when using 8 kHz sampling frequency, 4-bit OKI ADPCM2/ADPCM, and in monaural playback)
- Voice analysis and synthesis system : 4 systems
  4, 5, 6, 7-bit OKI ADPCM2, 4-bit OKI ADPCM, 8, 16-bit PCM, and 8-bit OKI Nonlinear PCM
- Source oscillation frequency : 4.096 MHz
- Sampling frequency
  6.4kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz
- Volume control (8 steps: 0 dB-21dB)
- Built-in 14-bit A/D converter
- Built-in LPF : attenuation factor -40dbm/oct
- Built-in 14-bit D/A converter
- Package:
  56-pin plastic QFP (QFP56-P-910-2K) (Product name: MSM9841GS-2K)

BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbol	Type	Description
D15-D8	I/O	Voice data input/output pins for 8-bit bus Interface For 16-bit interface, these pins are bidirectional data bus to input/output data with external microcontroller and memory.
D7-D0	I/O	Bidirectional data bus to input/output data and output status with external microcontroller and memory
$\overline{WR}$	I	Write pulse input pin. This pin inputs "L" pulse when command or data is input to D15-D0 pins.
$\overline{RD}$	I	Read pulse input pin. This pin inputs "L" pulse when status or data is output to D15-D0 pins.
$\overline{CS}$	I	Accepts write pulse and read pulse when this pin is "L". Does not accept write pulse and read pulse when this pin is "H".
D/$\overline{C}$	I	Inputs/outputs voice data from D15-D0 pins when this pin is "H" Inputs/outputs command and status from D7-D0 pins when this pin is "L"
EMP	O	"H" level indicates that there is no data in FIFO memory. Output conditions can be changed by command.
FUL	O	"H" level indicates that FIFO memory is full. Output conditions can be changed by command.
DREQ	O	DMA transfer request signal when FIFO is FUL (when recording) or EMP (when playback)
DACK	I	DMA transfer enable acceptance signal. Accepts signal of $\overline{IOR}$ pin and $\overline{IOW}$ pin when this pin is "H".
$\overline{IOW}$	I	Signal to write external memory data to MSM 9841 during DMA transfer
$\overline{IOR}$	I	Signal to read data of MSM 9841 for writing external memory during DMA transfer
ADSD	I	16-bit serial data input pin when external ADC is used
DASD	O	16-bit serial data output pin when external DAC is used
SIOCK	O	Synchronizing clock for 16-bit serial data input/output when external ADC or DAC is used
XT $\overline{XT}$	I O	Oscillator connection pin. When external clock is used, input clock from XT pin and leave $\overline{XT}$ pin open.
VCK	O	Outputs sampling frequency selected at recording/playback. This sampling frequency is used as synchronizing signals when external ADC or DAC is used.
$\overline{RESET}$	I	When "L" is input to this pin, LSI is initialized and enters power down status.
LIN	I	Inverting input pin for built-in OP amplifier Noninverting input pin is connected to SG (Signal Ground) internally.
LOUT	O	Output pin of built-in OP amplifier
AMON	O	Connected to LOUT pin when recording, and to built-in DAC output when playback. Connect this pin to input (FIN pin) for built-in LPF.

Symbol	I/O	Description
FIN	I	Input pin for built-in LPF
AOUTL	O	Left side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers.
AOUTR	O	Right side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers.
DV_{DD}	—	Digital power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and DGND pin.
DGND	—	Digital GND pin
AV_{DD}	—	Analog power supply pin. Insert minimum 0.1 μF bypass capacitor between this pin and AGND pin.
AGND	—	Analog GND pin

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	-0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	DGND=AGND=0V	+4.5 to +5.5	V
Operating Temperature	T_{op}	—	-40 to +85	°C
Master Clock Frequencyy	f_{OSC}	—	4.096	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5V, DGND=AGND=0V, Ta=-40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	V_{DD}×0.8	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	V_{DD}×0.2	V
High-level Output Voltage	V_{OH}	I_{OH}=-40μA	V_{DD}-0.3	—	—	V
Low-level Output Voltage	V_{OL}	I_{OL}=2mA	—	—	0.45	V
High-level Input Current (*1)	I_{IH1}	V_{IH}=V_{DD}	—	—	10	μA
High-level Input Current (*2)	I_{IH2}	V_{IH}=GND	—	—	20	μA
Low-level Input Cerrent (*1)	I_{IL1}	V_{IL}=GND	-10	—	—	μA
Low-level Input Current (*2)	I_{IL2}	V_{IL}=GND	-20	—	—	μA
Operating Current	I_{DD}	f_{OSC}=4.096MHz, without load	—	5	10	mA
Standby Current	I_{DDS}	At power down, without load Ta=-40 to +70°C	—	—	10	μA
		At power down, without load Ta=+70 to +85°C	—	—	50	μA

*1 Applies to input pins excluding XT pin.
*2 Applies to XT pin.

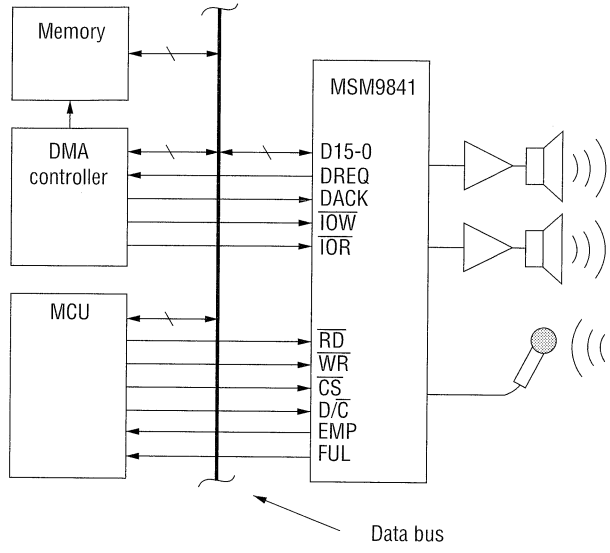
Analog Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5V, DGND=AGND=0V, Ta=-40 to +85°C

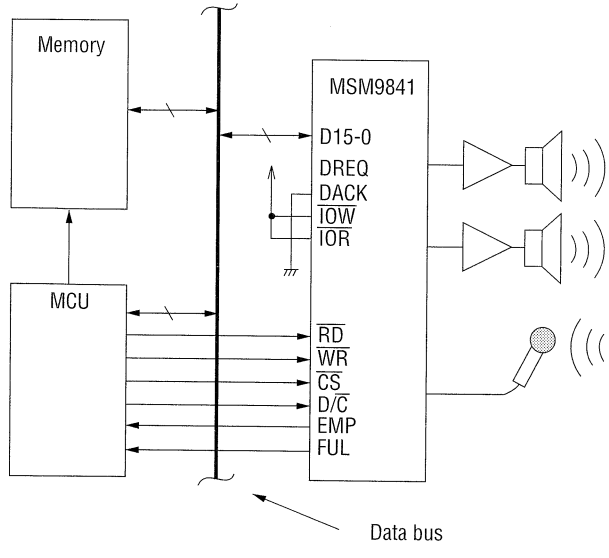
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D/A Output Relative Error	$\lvert V_{DAE} \rvert$	No load	—	—	10	mV
FIN Allowable Input Voltage Range	V_{FIN}	—	1	—	V_{DD}-1	V
FIN Input Impedance	R_{FIN}	—	1	—	—	MΩ
OP Amplifier Open Loop Gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
OP Amplifier Input Impedance	R_{INA}	—	1	—	—	MΩ
OP Amplifier Output Load Resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT Output Load Resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT Output Load Resistance	R_{FOUT}	—	50	—	—	kΩ

CPU INTERFACE EXAMPLE

1) Interface using DMA controller (for 16-bit bus)



2) Interface with MCU and external memory (for 16-bit bus)



OKI Semiconductor

MSM9862

Solid Recording LSI (Internal 512 Kbit E²PROM, for Serial Speech ROM, for Serial Registers)

GENERAL DESCRIPTION

MSM9862 is a solid recording LSI using the ADPCM system, and since a 512 Kbit E²PROM is included, this LSI can record and playback speech in almost the same manner as a tape recorder, by externally connecting a microphone, speaker and speaker drive amplifier.

MSM9862 can select standalone mode or microcomputer interface mode. In standalone mode, recording conditions are set by pins, and recording and playback can be controlled by simple startup timing. In microcomputer interface mode, recording and playback are controlled by command input from a microcomputer, and more abundant functions than standalone mode can be used.

If the serial speech ROM is connected externally, recording and playback with fixed messages can easily be implemented. Since serial registers can be connected externally, recording time and the number of recording messages can be increased.

MSM9862 also includes a DTMF (Dual Tone Multi Frequency) receiver, which implements functions required for telephone answering machines.

FEATURES

- 512 Kbit E²PROM included
  Overwriting : 10000 times
  Data holding : 10 years
  Recording time : 20 seconds (at 6.4 kHz sampling)
- 12 bit AD converter included
- 12 bit DA converter included
- AGC microphone amplifier included
- Low pass filter (LPF) included
  Attenuation characteristics: -40 dB/oct
- DTMF receiver included
  (Microcomputer interface mode only)
- External registers
  1Mbit serial register (MSM6389C) : can directly activate 4 chips
  512 Kbit serial register (MSM6587) : can directly activate 1 chip (microcomputer interface mode only)
- External ROM
  1Mbit serial speech ROM (MSM6595A-XXX)
  2Mbit serial speech ROM (MSM6596A-XXX)
  3Mbit serial speech ROM (MSM6597A-XXX)
- Maximum recording time: 262 seconds
  (Serial register is used, 3 bit ADPCM, 5.3 kHz sampling)
- Sound activation
- Pulse function
- Original oscillation frequency: 4.096 MHz

- Power supply voltage: 5V single
- Package:
  80-pin plastic QFP (QFP 80-P-1420-BK) (Product name: MSM9862GS-BK)

1. Features in standalone mode

- 3-bit ADPCM
- Sampling frequency
  5.3 kHz, 8.0 kHz (at 4.096 MHz)
  10.6 kHz, 16.0 kHz (at 8.192 MHz)
- Number of recorded words
  1, 2, 4 or 8 words

2. Features in microcomputer interface mode

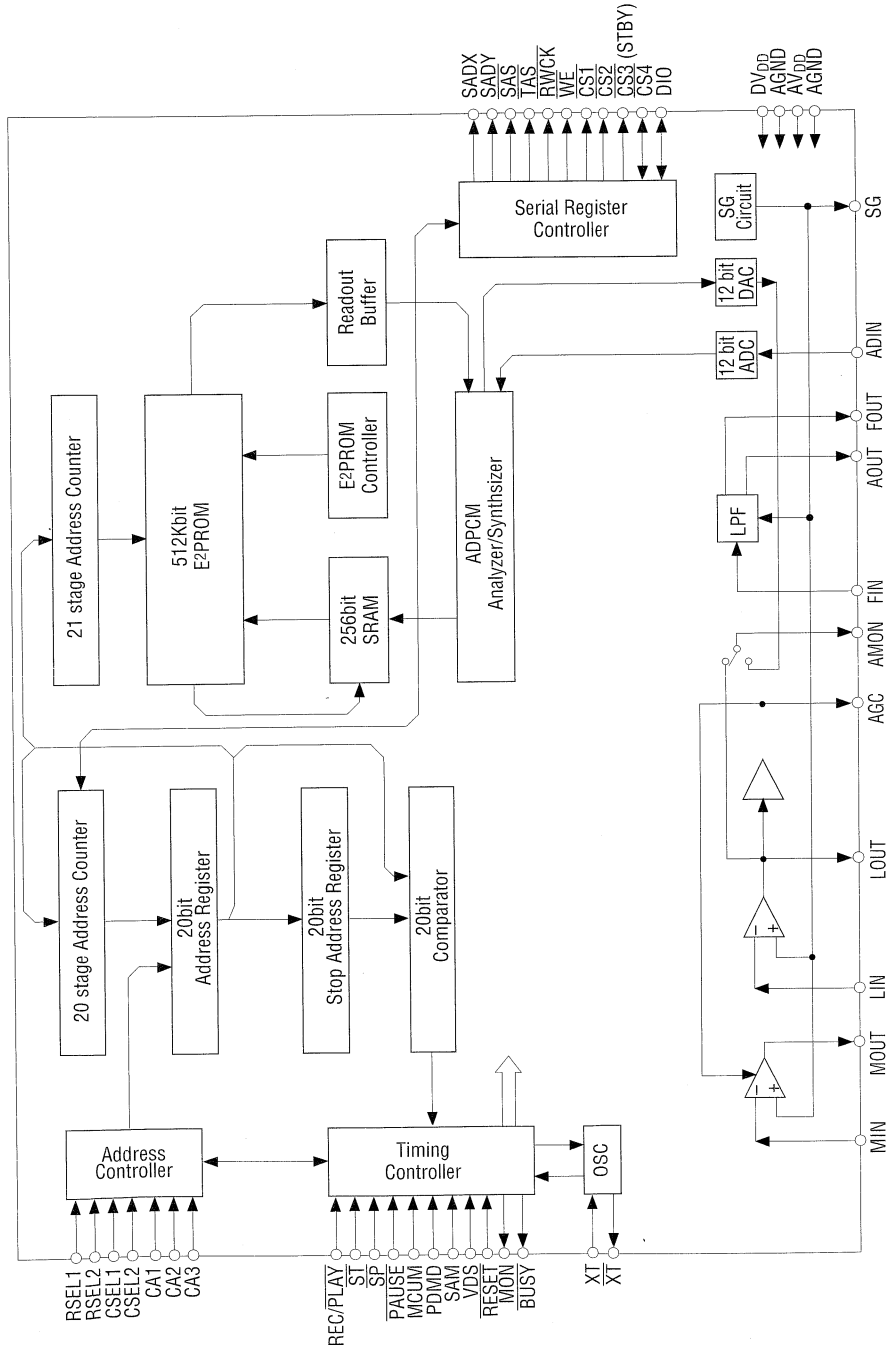
- 3-bit/4-bit ADPCM
- Sampling frequency
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz (at 4.096 MHz)
- 15 types of commands control condition setting, activation and stop of recording and playback
- Arbitrary data of built-in E^2PEOM can be written into or read out

3. Features of DTMF receiver

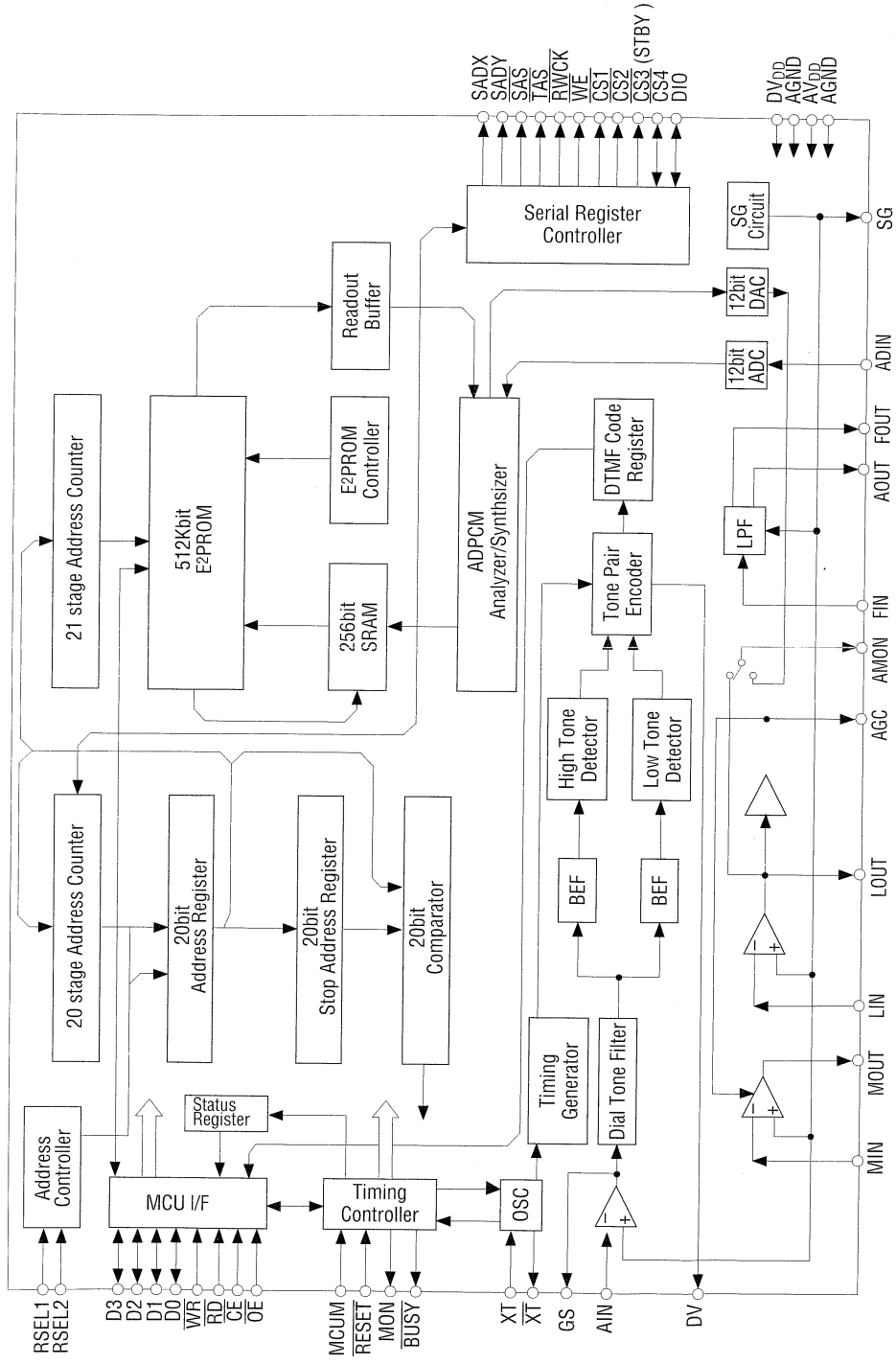
- Impression level can be adjusted
- 4 types of signal detection time can be selected
- Reflection prevention filter included in signal input area

BLOCK DIAGRAM

1. Standalone Mode

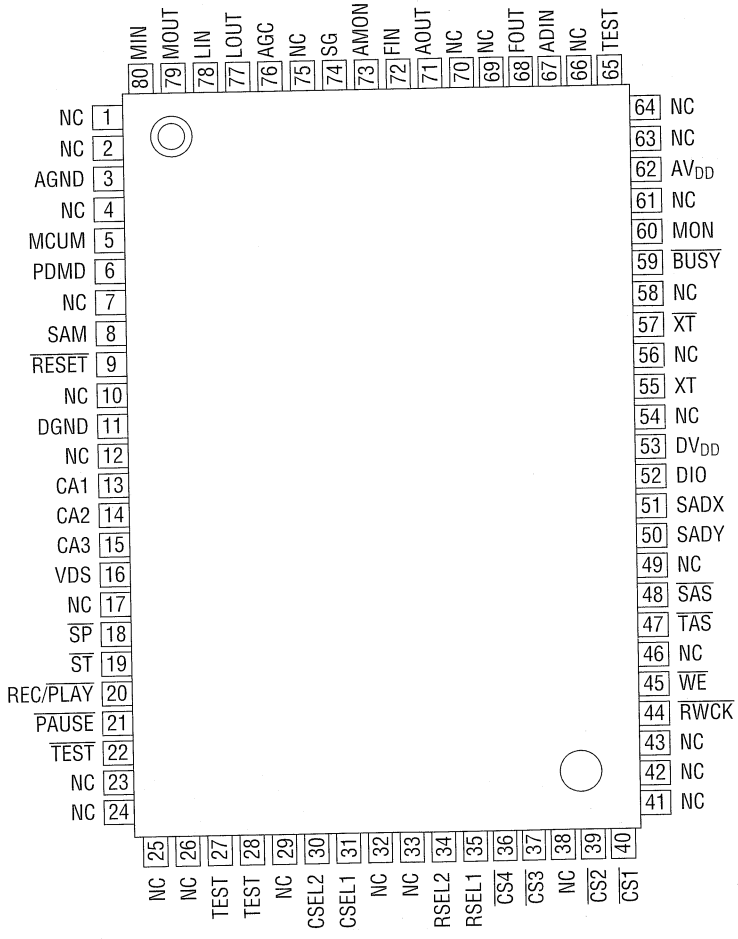


2. Microcomputer Interface Mode



PIN CONFIGURATION (TOP VIEW)

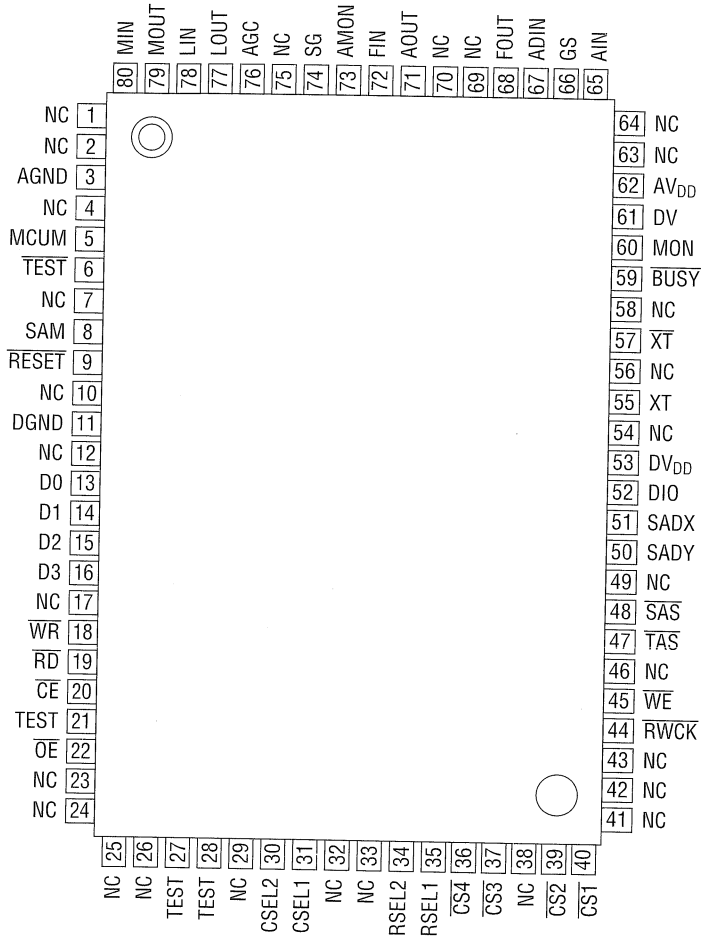
1. Standalone Mode



80-Pin Plastic QFP

NC: No-connection pin

2. Microcomputer Interface Mode



80-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTION

1. Common for Standalone Mode and Microcomputer Interface Mode

Pin Name	Type	Description
DV_{DD}	I	This is a digital power supply pin.
AV_{DD}	I	This is an analog power supply pin.
DGND	I	This is a digital GND pin.
AGND	I	This is an analog GND pin.
SG	O	This is an output pin for analog circuit reference voltage (signal ground).
MIN	I	This is a microphone input pin.
MOUT	O	This is an amplifying output for MIN input pin.
LIN	I	This is a reverse input pin for an internal OP amplifier. Non-reverse input pins are connected to SG internally.
LOUT	O	This is an amplifying output for LIN input pin.
AGC	O	This is a pin to control gain between MIN and MOUT, which hold the peak value of LOUT output voltage and feeds back this voltage to the input of MIN-MOUT amplifier.
AMON	O	This pin is connected to LOUT pin in recording mode, and to D/A converter output in playback mode. Connect this pin to the input of internal LPF (FIN pin).
FIN	I	This is an input pin for internal LPF.
FOUT	O	This is an output pin for internal LPF. Connect this pin to the input of A/D converter (ADIN pin).
ADIN	I	This is an input pint for internal 12-bit A/D converter.
AOUT	O	This is an output pin for internal LPF. Since this is an output pin for playback waveforms, connect amplifier for speaker drive.
SADX	O	(Serial address data) Connect this pin to SADX pin of serial voice ROM. This is a pin to output first address of read/write.
SADY	O	(Serial address strobe) Connect this pin to SADY pin of serial register. This is a pin to output first address of read/write.
$\overline{SAS}$	O	(Serial address data) Connect this pin to $\overline{SAS}$ pin of serial register. This is a clock to write serial address.
$\overline{TAS}$	O	(Transfer address strobe) Connect this pin to $\overline{TAS}$ pin of serial register. This is a pin to set serial address being input from SADX and SADY pins to address counter inside serial register.
$\overline{RWCK}$	O	(Read/write clock) Connect this pin to $\overline{RWCK}$ pin of serial register. This is a block pin to read and write data from/to serial register.
$\overline{WE}$	O	(Write enable) Connect this pin to $\overline{WE}$ pin of serial register. This is a pin to select read mode or write mode.
DIO	I/O	(Data I/O) Connect this pin to DIN pin and DOUT pin of serial register. This is a pin to output write data and to load read data.

Pin Name	Type	Description
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ (STBY) $\overline{CS4}$	O O O O	(Chip select) Connect these pins to $\overline{CS}$ pin of serial registers. Function of $\overline{CS3}$ pin changes depending on the number of serial registers to be connected. Select the number of registers by RSEL1 and RSEL2 pins. $\overline{CS3}$ (STBY) pin becomes $\overline{CS3}$ when 4 serial registers are used. Otherwise, $\overline{CS3}$ pin becomes STBY pin to output "H" level in power down status.

RSEL2	L	L	H	H
RSEL1	L	H	L	H
$\overline{CS3}$ (STBY)	STBY	STBY	STBY	$\overline{CS3}$

MCUM	I	This is a pin to select standalone mode or microcomputer interface mode. "L" level: standalone mode "H" mode: microcomputer interface mode
$\overline{RESET}$	I	When "L" level if input to this pin, LSI enters initial status and power down status.
$\overline{BUSY}$	O	This is a pin to output BUSY status, which outputs "L" level in BUSY status.
XT	I	This is a pin to connect oscillator. When external clock is used, clock is input from this pin. Input GND level when power is down.
$\overline{XT}$	O	This is a pin to connect oscillator. Leave this pin OPEN when external clock is input.
TEST $\overline{TEST}$	I	This is a pin for testing LSI. Input "L" level to TEST pin and "H" level to TEST pin

2. Standalone Mode

Pin Name	Type	Description
REC/$\overline{PLAY}$	I	This is a pin to select recording or playback. Recording mode is selected when "H" level is input to this pin.
$\overline{ST}$	I	When "L" pulse is input to this pin. recording or playback starts. This pin is pulled up internally.
$\overline{SP}$	I	When "L" pulse is input to this pin, recording or playback stops. This pin is pulled up internally.
$\overline{PAUSE}$	I	When "L" pulse is input to this pin, recording or playback pauses. This pin is pulled up internally.
CSEL1 CSEL2	I I	These pins select the number of recorded words and control mode. When the number of recorded words is "1", select flex mode and fix to ch0.

CSEL2	L	L	H	H
CSEL1	L	H	L	H
Number of recorded words	8 words	4 words	2 words	8 words
Control mode	Fix			Flex

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>CA1
CA2
CA3</td><td>I
I
I</td><td>These are pins to specify channel. (For specification method, see channel specification in operation in case of standalone mode.)</td></tr>
<tr><td>SAM</td><td>I</td><td>This is a pin to select sampling frequency. Relationship between original oscillation frequency (fosc) and sampling frequency (fsamp) is as follows.
( ): at f_{OSC}=4.096 NHz
<table>
<tr><th>SAM</th><th>L</th><th>H</th></tr>
<tr><td>fsamp</td><td>$\frac{fosc}{768}$
(5.3kHz)</td><td>$\frac{fosc}{512}$
(8.0kHz)</td></tr>
</table></td></tr>
<tr><td>RSEL2
RSEL1</td><td>I
I</td><td>(Register select) These are pins to select memory to be used and number of registers to be connected externally.
<table>
<tr><td>CSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>CSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Memory</td><td>Internal E^2PROM</td><td>1Mbit one serial register</td><td>1Mbit two serial registers</td><td>1Mbit four serial registers</td></tr>
</table></td></tr>
<tr><td>PDMD</td><td>I</td><td>This is a pin to select entry of power down status.
"L" level : Automatically enters into power down status, except during recording and playback.
"H" level : Enters standby status, not power down status, except during recording and playback.
RESET pin is used to enter power down status.
Use this mode when internal LPF is used for external circuit</td></tr>
<tr><td>VDS</td><td>I</td><td>This is a pin to select sound activation, where recording starts when speech input becomes specified for at higher amplitude.
Sound activation circuit is operated by inputting "H" level to this pin.</td></tr>
<tr><td>MON</td><td>O</td><td>This pin outputs "H" level during recording and playback.</td></tr>
</table>

3. Microcomputer Interface Mode

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D0
D1
D2
D3</td><td>I
I
I
I</td><td>These pins are a bi-directional data bus, which input/output commands and data to/from external microcomputer.</td></tr>
<tr><td>$\overline{WR}$</td><td>I</td><td>This is a write pulse input pin, which inputs "L" pulse when command or data is input to D0~D3 pins.</td></tr>
<tr><td>$\overline{RD}$</td><td>I</td><td>This is a read pulse input pin, which inputs "L" pulse when status or data is output from D0~D3 pins.</td></tr>
<tr><td>$\overline{CE}$</td><td>I</td><td>If "H" level is input to this pin, write pulse ($\overline{WR}$), read pulse ($\overline{RD}$) and DTMF code read pulse ($\overline{OE}$) are not accepted, and data is not input/output via D0~D3 pins.</td></tr>
<tr><td>MON</td><td>O</td><td>This pin outputs "H" level during recording and playback. This pin also outputs clock for synchronization during recording and playback by EXT command</td></tr>
<tr><td>RSEL1
RSEL2</td><td>I
I</td><td>These are pins to select the number of serial registers connected externally.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Number of serial registers</td><td>512 Kbit one serial register</td><td>1Mbit one serial register</td><td>1Mbit two serial registers</td><td>1Mbit four serial registers</td></tr>
</table></td></tr>
<tr><td>$\overline{OE}$</td><td>I</td><td>This is a pin to input read pulse to read detection code of DTMF receiver. "L" pulse is input to this pin when DTMF code is output from D0~D3 pins.</td></tr>
<tr><td>DV</td><td>O</td><td>This is an output pin to indicate that DTMF receiver detected valid code. This pin outputs "H" level when DTMF receiver detects valid code.</td></tr>
<tr><td>AIN</td><td>I</td><td>This is a pin to input DTMF signal of DTMF receiver.
Since this is a reverse input pin of internal OP amplifier, this pin creates reverse amplifier with GS pin and adjusts impression level. Non-reverse input pins of OP amplifier are internally connected to SG.</td></tr>
<tr><td>GS</td><td>O</td><td>This is the amplifying output of AIN input pin.</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	DGND=AGND=0V	+4.5 to +5.5	V
Operating Temperature	T_{op}	Ta=25°C	−10 to +70	°C
Original Oscillation Frequency	f_{osc}	—	4.096	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5V
DGND=AGND=0V, Ta=−10 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	V_{DD}×0.8	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	V_{DD}×0.2	V
"H" Output Voltage	V_{OH}	I_{OH}=−40µA	V_{DD}−0.3	—	—	V
"L" Output Voltage	V_{OL}	I_{OL}=2mA	—	—	0.45	V
"H" Input Current (Note 1)	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
"H" Input Current (Note 2)	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
"L" Input Current (Note 3)	I_{IL1}	V_{IL}=GND	−10	—	—	µA
"L" Input Current (Note 2)	I_{IL2}	V_{IL}=GND	−20	—	—	µA
"L" Input Current (Note 4)	I_{IL3}	V_{IL}=GND	−400	—	−20	µA
Operating Current Consumption (1)	I_{DD1}	For using E²PROM in microcomputer interface mode	—	TBD	TBD	mA
Operating Current Consumption (2)	I_{DD2}	For using E²PROM in standalone mode	—	TBD	TBD	mA
Operating Current Consumption (3)	I_{DD3}	For using serial register in microcomputer interface mode	—	TBD	TBD	mA
Operating Current Consumption (4)	I_{DD4}	For using serial register in standalone mode	—	TBD	TBD	mA
Operating Current Consumption (5)	I_{PD}	When power is down	—	—	10	µA

Notes: 1. Applied to input pins, excluding XT pin.
2. Applied to XT pin.
3. Applied to input pins without pullup resistance, excluding XT pin.
4. Applied to input pins with pullup resistance, excluding XT pin.

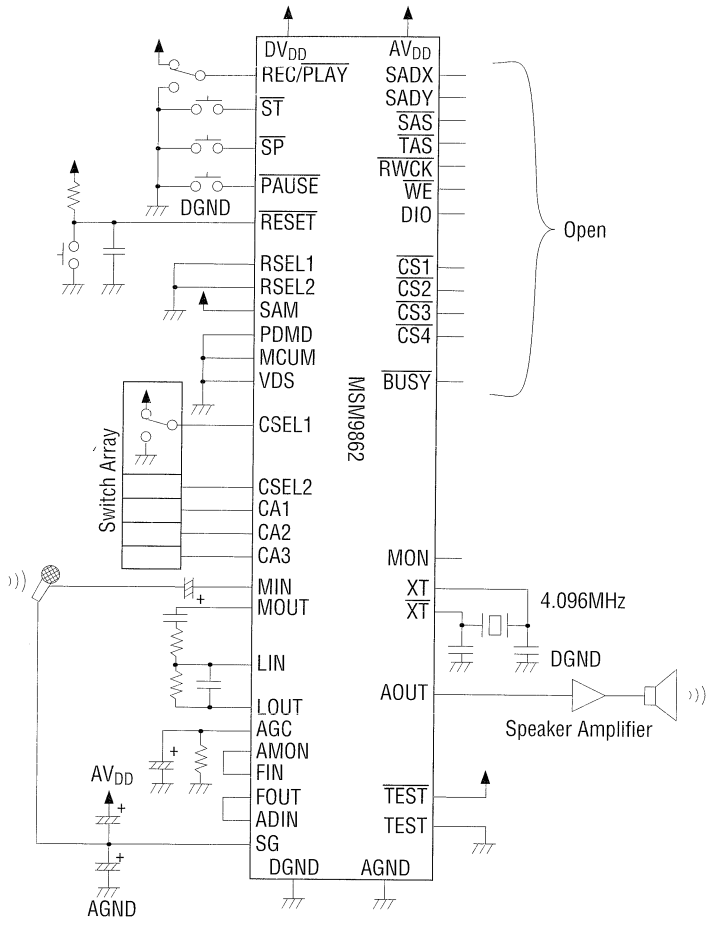
Analog Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5V
DGND=AGND=0V, Ta=−10 to +70°C

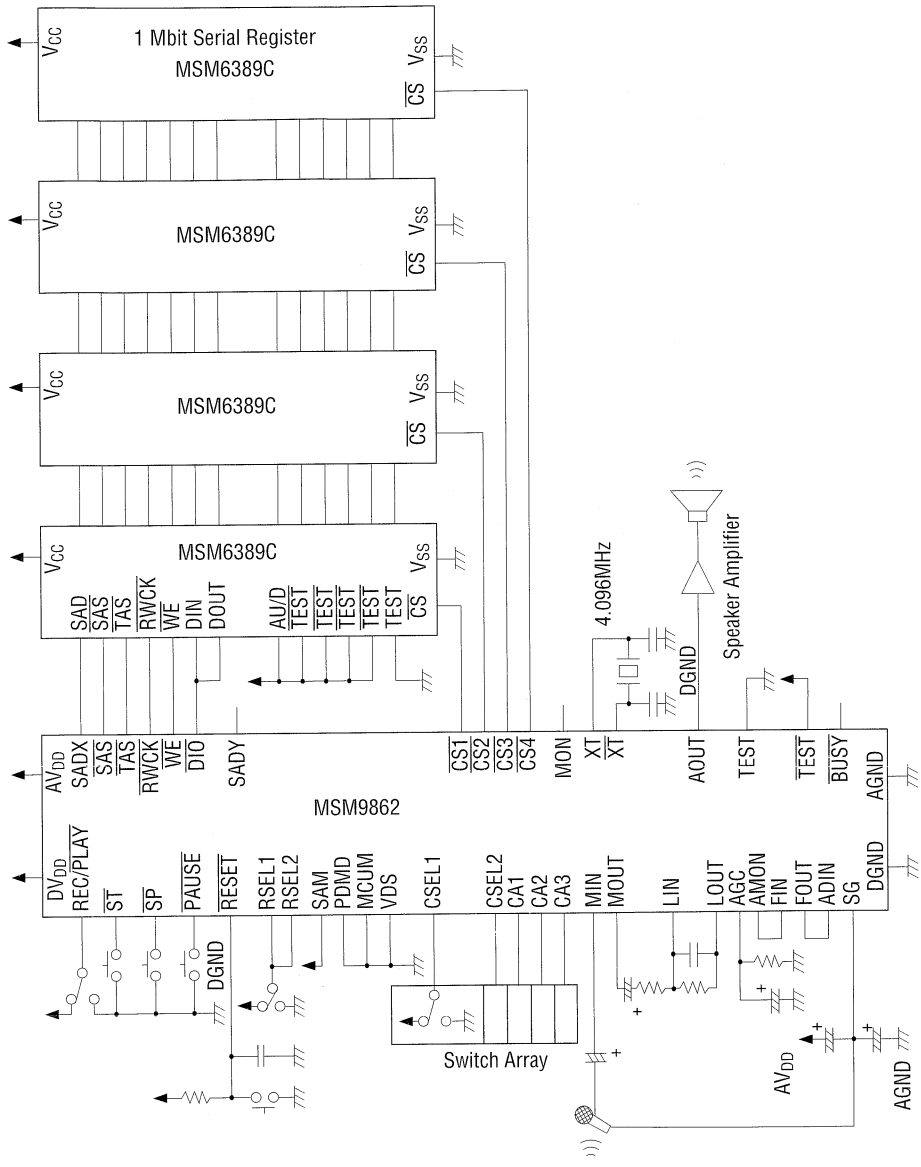
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D/A Output Relative Error.	$\|V_{DAE}\|$	No Load	—	—	10	mV
FIN Permissible Input Voltage Range	V_{FIN}	—	1	—	V_{DD}−1	V
MIN Input Impedance	R_{MIN}	—	—	10	—	kΩ
MIN-MOUT Voltage Gain (1)	G_{M1}	AV_{DD}–AGC=2V	—	25	—	dB
MIN-MOUT Voltage Gain (2)	G_{M2}	AV_{DD}–AGC=1V	—	—	5	dB
MOUT Output Load Resistance	R_{MOUT}	—	2	—	—	kΩ
AGC Source Output Current	I_{AGC}	AGC=AV_{DD}−1V	—	—	−10	mA
LIN-LOUT Open Loop Gain	G_{OPL}	f_{IN}=0 to 4kHz	40	—	—	dB
LIN Input Impedance	R_{LIN}	—	1	—	—	MΩ
LOUT Output Load Resistance	R_{LOUT}	—	200	—	—	kΩ
AOUT Output Load Resistance	R_{AOUT}	—	50	—	—	kΩ
FIN Input Impedance	R_{FIN}	—	1	—	—	MΩ
FOUT Output Load Resistance	R_{FOUT}	—	50	—	—	kΩ
AIN Input Impedance	R_{AIN}	—	1	—	—	MΩ
GS Output Load Resistance	R_{AOUT}	—	50	—	—	kΩ
AIN-GS Open Loop Gain	G_{OPA}	f_{IN}=0 to 4kHz	40	—	—	dB

APPLICATION CIRCUIT EXAMPLE

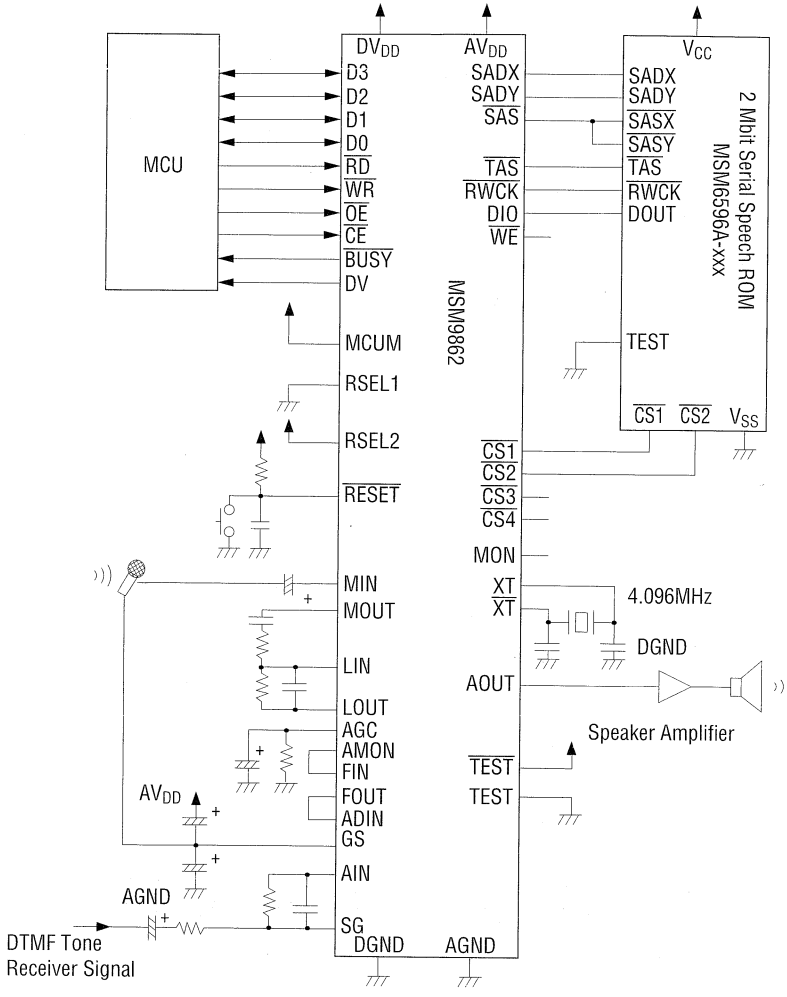
- Circuit diagram 1 shows an application circuit example when MSM9862 is used in standalone mode and recording/playback is performed by internal E^2PROM.
- Circuit diagram 2 shows an application circuit example when MSM9862 is used in standalone mode and recording/playback is performed by internal E^2PROM and external serial register.
- Circuit diagram 3 shows an application circuit example when MSM9862 is used in microcomputer interface mode, recording/playback is performed by internal E^2PROM, playback is performed by serial speech ROM with a channel index, and the DTMF receiver is used.
- Circuit diagram 4 shows an application circuit example when MSM9862 is used in microcomputer interface mode, recording/playback is performed by internal E^2PROM and external serial register, playback is performed by serial speech ROM without a channel index, and the DTMF receiver is used.
- Circuit diagram 5 shows an application circuit example when recording/playback is performed by the EXT command and the DTMF receiver is not used.



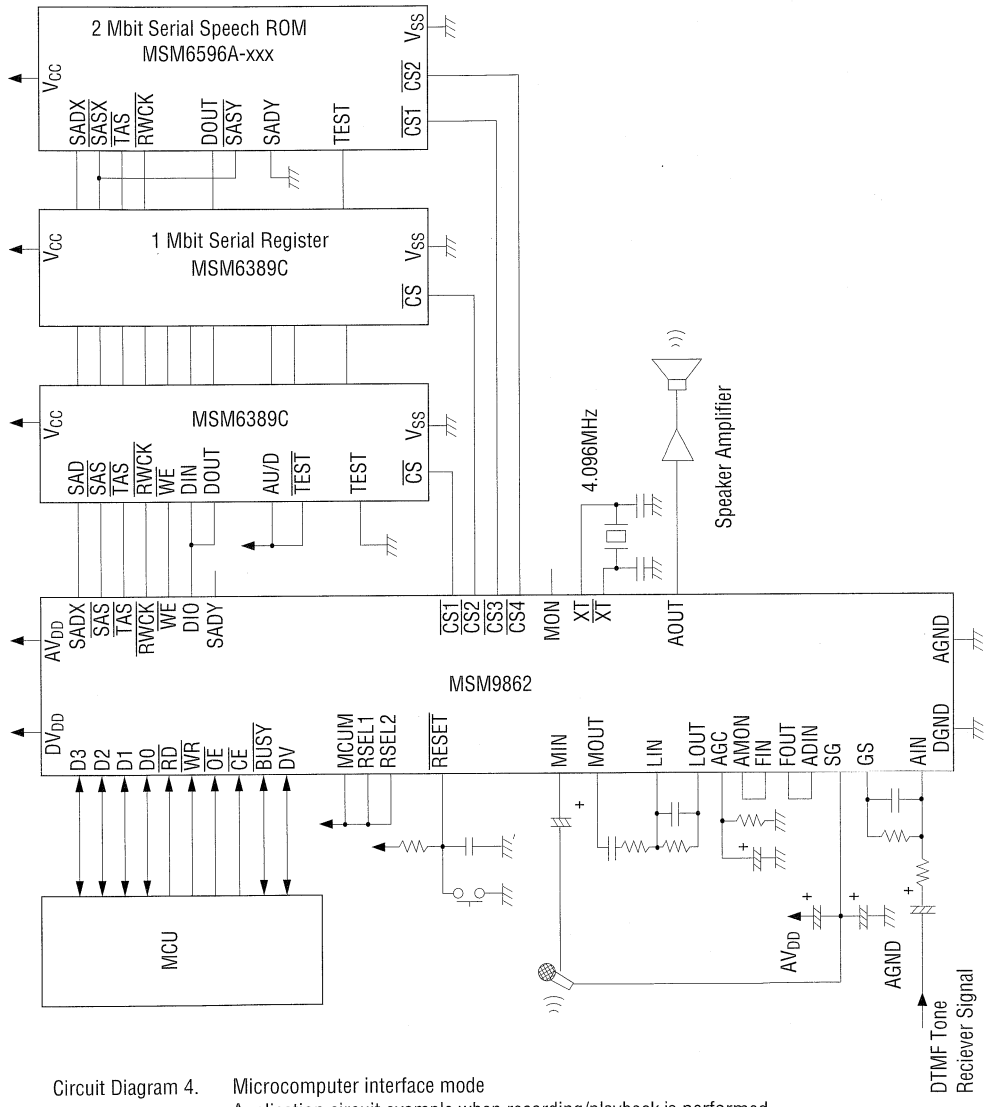
Circuit Diagram 1. Standalone mode
Application circuit example when recording/playback is performed by internal E²PROM.



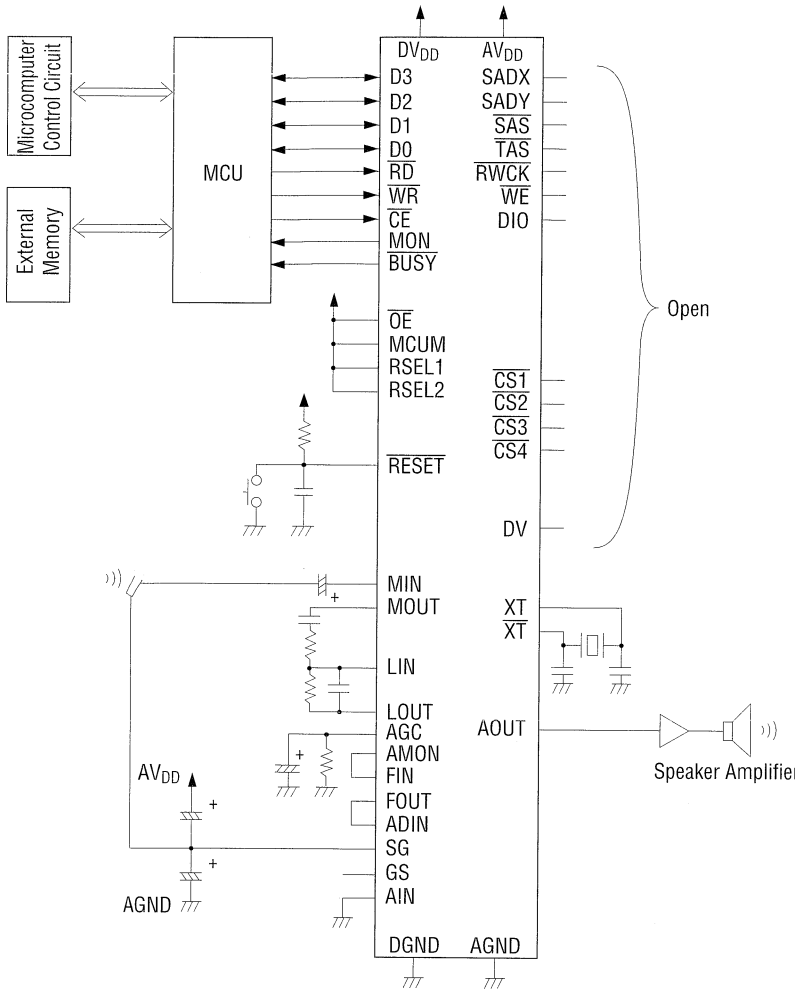
Circuit Diagram 2. Standalone mode
Application circuit example when recording/playback is performed by internal E²PROM and external serial register.



Circuit Diagram 3. Microcomputer interface
Application circuit example when recording/playback is performed by internal E²PROM, playback is performed by serial speech ROM with channel index, and DTMF receiver is used.



Circuit Diagram 4. Microcomputer interface mode
Application circuit example when recording/playback is performed by internal E²PROM and external serial register, playback is performed by serial speech ROM without channel index, and DTMF receiver is used.



Circuit Diagram 5. Application circuit example when recording/playback is performed by EXT command and DTMF receiver is not used.

DATA SHEET 3 VOICE REGISTERS/ROMs

OKI Semiconductor

MSM6586

262,144-Word x 1-Bit Serial Register

GENERAL DESCRIPTION

The MSM6586 is a serial register in 262,144 words x 1 bit configuration featuring medium speed operation with low power consumption.

The MSM6586 has a built-in internal address generator circuit allowing continuous serial read/write operation by external clock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

A refresh timer and refresh counter are built in to eliminate the need of the external refresh circuit and to realize low power consumption.

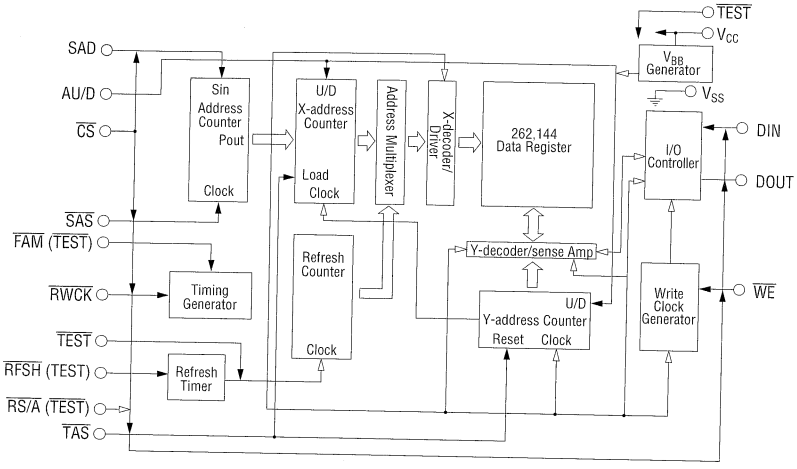
18-pin plastic QFJ (PLCC) is used as the package and the operating temperature range is between 0°C and 70°C.

The MSM6586 is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be constructed in combination with OKI's voice synthesizer ICs, MSM6388 and MSM6588.

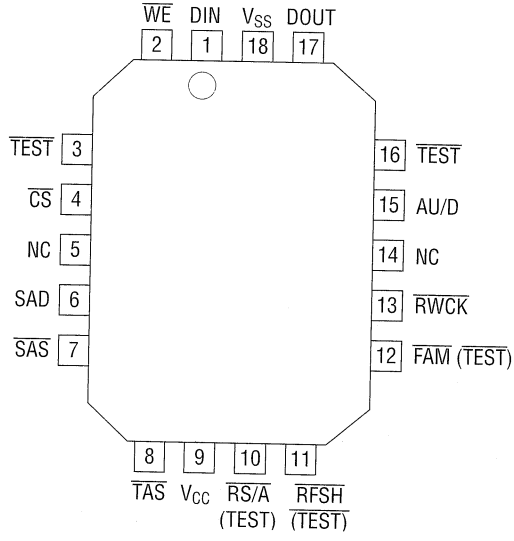
FEATURES

- Configuration : 262,144 x 1 bit
- Serial access operation
  - Serial access time : 1.5 µs (3.0 µs)
  - Serial read/write cycle time : 2.0 µs (4.0 µs)
  - Fast mode read/write cycle time : 0.4 µs (0.4 µs)
  - Times in parentheses indicate ones in self-refresh mode.
- Low current consumption : 100 µA max. (for data holding, V_{CC} = 4.0 V)
- Wide operating supply voltage range : Single 3.5 to 5.5 V
- Auto-refresh/self-refresh changeable
- Package:
  - 18-pin plastic QFJ (PLCC) (QFJ18-P-R290) (Product name : MSM6586JS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



18-Pin Plastic QFJ

PIN DESCRIPTIONS

Pin	Description
1	Data input
2	Write enable
3	Test input
4	Chip select
5	No connection
6	Serial address data
7	Serial address strobe
8	Transfer address strobe
9	Power supply (+5V)
10	Self-refresh/auto-refresh select (Test input)
11	Refresh clock input
12	Fast access mode select (Test input)
13	Read/write clock
14	No connection
15	Address up/down select
16	Test input
17	Data output
18	Ground (0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Terminal Voltage	V_T	Ta = 25°C, relative to V_{SS}	−1.0 to +7.0	V
Output Short-Circuit Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{OP}	—	0 to +70	°C
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" Input Voltage	V_{IL}	−0.5	0	0.5	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 3.5V to 5.5V, Ta = 0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH} = −0.5mA	V_{CC} − 0.5	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 0.5mA	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V to V_{CC}	−1	1	µA
Output Leakage Current	I_{LO}	V_O = 0V to V_{CC}	−1	1	µA
Supply Current (in operating state)	I_{CC1}	V_{CC} = 4V, t_{RC} = 2µs	—	5	mA
Supply Current (in standby state)	I_{CC2}	V_{CC} = 4V	—	100	µA
Supply Current (FAM)	I_{CC3}	V_{CC} = 4V, t_{RC} = 0.4µs	—	15	mA

OKI Semiconductor

MSM6587

524,288-Word x 1-Bit Serial Register

GENERAL DESCRIPTION

The MSM6587 is a serial register in 524,288 words x 1 bit configuration featuring medium speed operation with low-power consumption.

The MSM6587 has a built-in internal address generator circuit allowing continuous serial read/write operation by external clock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

A refresh timer and refresh counter are built in to eliminate the need of the external refresh circuit and to realize low power consumption.

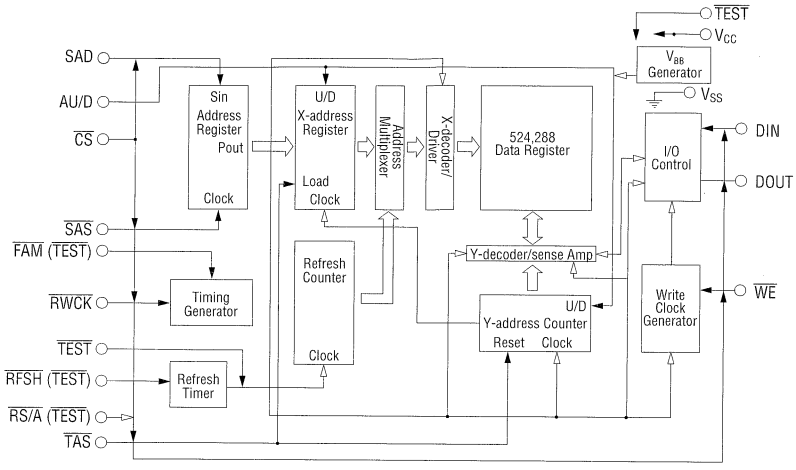
18-pin plastic QFJ (PLCC) is used as the package and the operating temperature range is between 0°C and 70°C.

The MSM6587 is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be constructed in combination with OKI's voice synthesizer ICs.

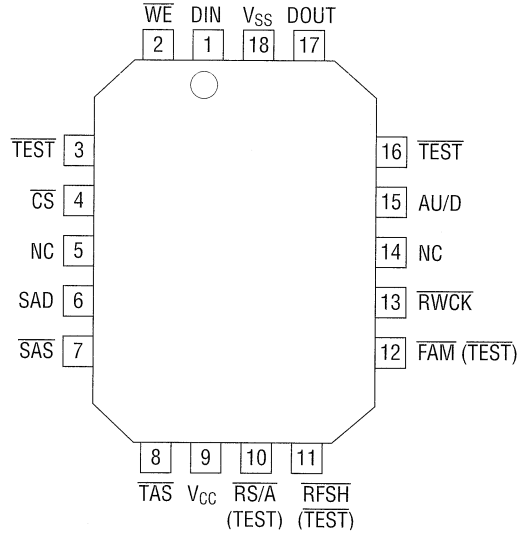
FEATURES

- Configuration : 524,288 x 1 bit
- Serial access operation
  - Serial access time : 1.5 µs (3.0 µs)
  - Serial read/write cycle time : 2.0 µs (4.0 µs)
  - Fast mode read/write cycle time : 0.4 µs (0.4 µs)
  - Times in parentheses indicate ones in self-refresh mode.
- Low current consumption : 100 µA max. (for data holding, Vcc=4.0 V)
- Wide operating supply voltage range : Single 3.5 to 5.5 V
- Auto-refresh/self-refresh changeable
- Package:
  - 18-pin plastic QFJ (PLCC) (QFJ18-P-R290) (Product name : MSM6587JS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

18-Pin Plastic QFJ

PIN DESCRIPTIONS

Pin	Description
1	Data input
2	Write enable
3	Test input
4	Chip select
5	No connection
6	Serial address data
7	Serial address strobe
8	Transfer address strobe
9	Power supply (+5V)
10	Self-refresh/auto-refresh select (Test input)
11	Refresh clock input
12	Fast access mode select (Test input)
13	Read/write clock
14	No connection
15	Address up/down select
16	Test input
17	Data output
18	Ground (0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Terminal Voltage	V_T	Ta = 25°C, relative to V_{SS}	−1.0 to +7.0	V
Output Short-Circuit Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{op}	—	0 to +70	°C
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" Input Voltage	V_{IL}	−0.5	0	0.5	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 3.5V to 5.5V, Ta = 0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH} = −0.5mA	V_{CC} − 0.5	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 0.5mA	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V to V_{CC}	−1	1	µA
Output Leakage Current	I_{LO}	V_O = 0V to V_{CC}	−1	1	µA
Supply Current (in operating state)	I_{CC1}	V_{CC} = 4V, t_{RC} = 4µs	—	5	mA
Supply Current (in standby state)	I_{CC2}	V_{CC} = 4V	—	100	µA
Supply Current (FAM)	I_{CC3}	V_{CC} = 4V, t_{RC} = 0.4µs	—	15	mA

OKI Semiconductor

MSM6389C

1,048,576-Word x 1-Bit Solid-State Recorder Data Register

GENERAL DESCRIPTION

The MSM6389C is a solid-state recorder data register in 1,048,576 words x 1 bit configuration.

The MSM6389C has a built-in internal address generator circuit allowing continuous serial read/write operation by single external clock input. The internal address is automatically incremented by one by read/write operation.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

The built-in refresh timer and refresh counter have eliminated the need of an external refresh circuit and realized a low power consumption.

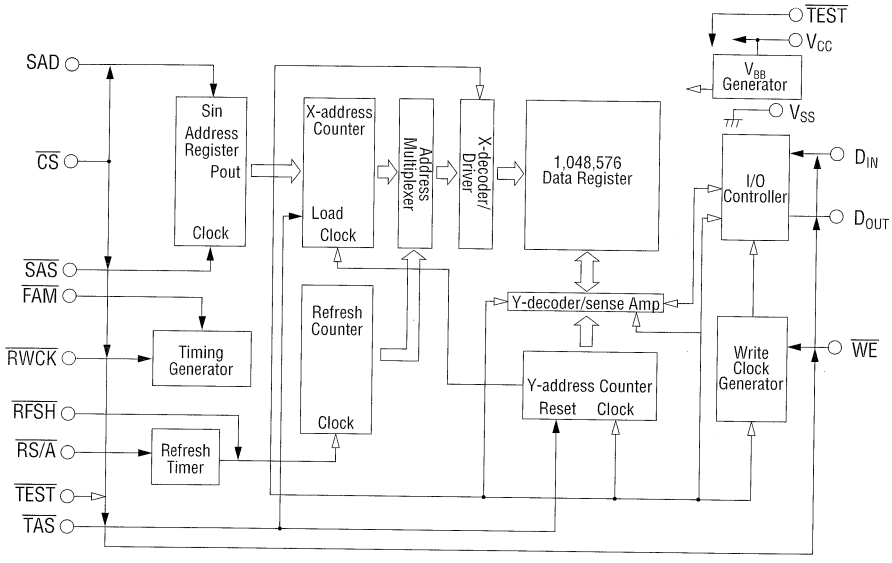
18-pin plastic QFJ is used as the package and the operating temperature range is between 0°C and 70°C.

The MSM6389C is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be constructed in combination with OKI's voice synthesizer ICs.

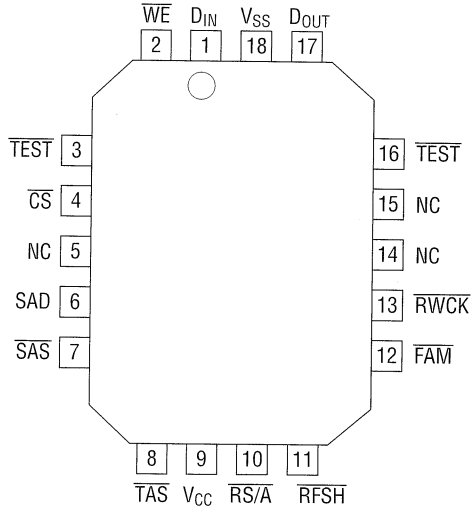
FEATURES

- Configuration: 1,048,576 x 1 bit
- Serial access operation:
  - Serial access time 1.5µs (3.0µs)
  - Serial read/write cycle time 2.0µs (4.0µs)
  - Fast mode read/write cycle time 0.4µs (0.4µs)
  - Times in parentheses indicate ones in self-refresh mode.
- Low current consumption: 100 µA max. (for data holding, V_{CC}=4.0V)
- Wide operating supply voltage range: Single 3.5 to 5.5V
- Auto-refresh/self-refresh changeable
- Packages: 18-pin plastic QFJ (QFJ18-P-R290)
  (Product name: MSM6389CJS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



18-Pin Plastic QFJ

NC: No-connection pin

PIN DESCRIPTIONS

Pin Name	Description
D_{IN}	Data Input
$\overline{WE}$	Write Enable
$\overline{TEST}$	Test Input
$\overline{CS}$	Chip Select
NC	No Connection
SAD	Serial Address Data
$\overline{SAS}$	Serial Address Strobe
$\overline{TAS}$	Transfer Address Strobe
V_{CC}	Power Supply (+5 V)
$\overline{RS/A}$	Auto-Refresh/Self-Refresh Select (Test Input)
$\overline{RFSH}$	Refresh Clock Input
$\overline{FAM}$	Fast Access Mode Select (Test Input)
$\overline{RWCK}$	Read/Write Clock
D_{OUT}	Data Output
V_{SS}	Ground (0 V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Terminal Voltage	V_T	Ta = 25°C, relative to V_{SS}	−1.0 to +7.0	V
Output Short-Circuit Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{op}	—	0 to +70	°C
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.5	4.5	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" Input Voltage	V_{IL}	−0.5	0	0.5	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 3.5 V to 5.5 V, Ta = 0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH} = −0.5 mA	V_{CC} − 0.5	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 0.5 mA	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0 V to V_{CC}	−1	1	µA
Output Leakage Current	I_{LO}	V_O = 0 V to V_{CC}	−1	1	µA
Supply Current (in operating state)	I_{CC1}	V_{CC} = 4 V, t_{RC} = 4 µs	—	5	mA
Supply Current (in standby state)	I_{CC2}	V_{CC} = 4 V	—	100	µA
Supply Current (FAM)	I_{CC3}	V_{CC} = 4 V, t_{RC} = 0.4 µs	—	15	mA

OKI Semiconductor

MSM63V89C

1,048,576-Word x 1-Bit Solid-State Recorder Data Register

GENERAL DESCRIPTION

The MSM63V89C is a solid-state recorder data register in 1,048,576 words x 1 bit configuration.

The MSM63V89C has a built-in internal address generator circuit allowing continuous serial read/write operation by single external clock input. The internal address is automatically incremented by one by read/write operation.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

The built-in refresh timer and refresh counter have eliminated the need of an external refresh circuit and realized a low power consumption.

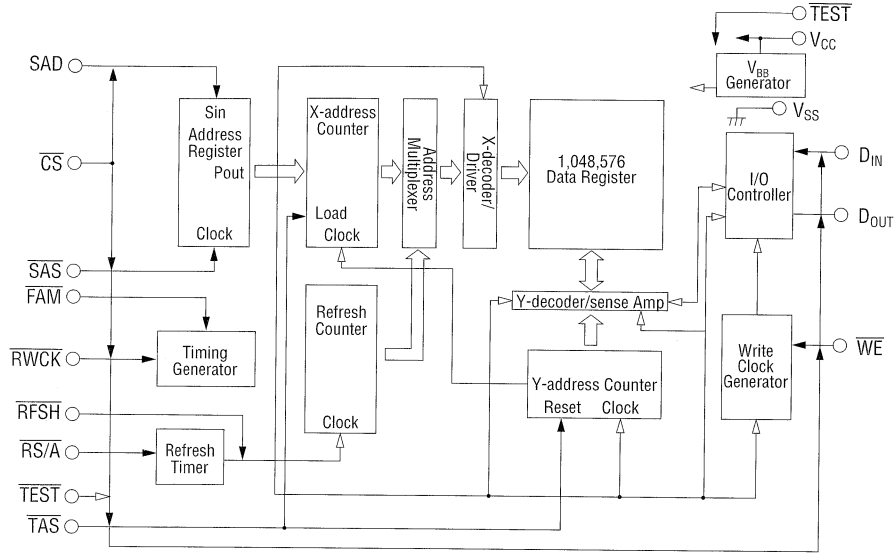
26/20-pin plastic TSOP is used as the package and the operating temperature range is between 0°C and 70°C.

The MSM63V89C is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be constructed in combination with OKI's voice synthesizer ICs.

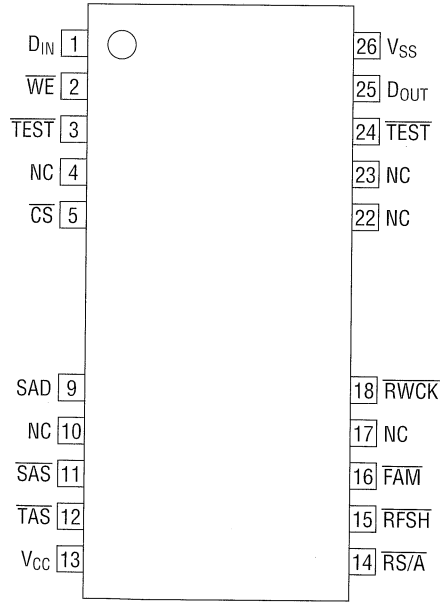
FEATURES

- Configuration: 1,048,576 x 1 bit
- Serial access operation:
  - Serial access time 1.5µs (3.0µs)
  - Serial read/write cycle time 2.0µs (4.0µs)
  - Fast mode read/write cycle time 0.4µs (0.4µs)
  - Times in parentheses indicate ones in self-refresh mode.
- Low current consumption: 50 µA max. (for data holding, V_{CC}=3.0 V)
- Wide operating supply voltage range: Single 2.7 to 3.6V
- Auto-refresh/self-refresh changeable
- Packages: 26/20-pin plastic TSOP (TSOP26/20-P-300-K)
  (Product name: MSM63V89CTS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC :No-connection pin

26/20-pin plastic TSOP

PIN DESCRIPTIONS

Pin Name	Description
D_{IN}	Data Input
$\overline{WE}$	Write Enable
$\overline{TEST}$	Test Input
$\overline{CS}$	Chip Select
NC	No Connection
SAD	Serial Address Data
$\overline{SAS}$	Serial Address Strobe
$\overline{TAS}$	Transfer Address Strobe
V_{CC}	Power Supply (3.3 V)
$\overline{RS/A}$	Auto-Refresh/Self-Refresh Select (Test Input)
$\overline{RFSH}$	Refresh Clock Input
$\overline{FAM}$	Fast Access Mode Select (Test Input)
$\overline{RWCK}$	Read/Write Clock
D_{OUT}	Data Output
V_{SS}	Ground (0 V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Terminal Voltage	V_T	Ta = 25°C, relative to V_{SS}	−1.0 to +7.0	V
Output Short-Circuit Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{op}	—	0 to +70	°C
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" Input Voltage	V_{IL}	−0.5	0	0.5	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH} = −0.5 mA	V_{CC} − 0.5	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 0.5 mA	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0 V to V_{CC}	−1	1	µA
Output Leakage Current	I_{LO}	V_O = 0 V to V_{CC}	−1	1	µA
Supply Current (in operating state)	I_{CC1}	V_{CC} = 3 V, t_{RC} = 4 µs	—	3	mA
Supply Current (in standby state)	I_{CC2}	V_{CC} = 3 V	—	50	µA
Supply Current (FAM)	I_{CC3}	V_{CC} = 3 V, t_{RC} = 0.4 µs	—	10	mA

OKI Semiconductor

MSM6684B

4,194,304-word x 1-bit Serial Register

GENERAL DESCRIPTION

MSM6684B is a serial register organized as 4,194,304 words x one bit, characterized by medium-speed, low power consumption operation.

This device has a built-in internal address generation circuit. Triggered off by a single external clock pulse, it provides serial, continuous read/write operations.
Read/write operation causes the internal address to be incremented automatically by +1.

External address input enables addressing in units of 1024 words. Furthermore, a refresh timer and a refresh address counter are installed, which makes an external refresh circuit unnecessary. In addition, this configuration allows lower power consumption.

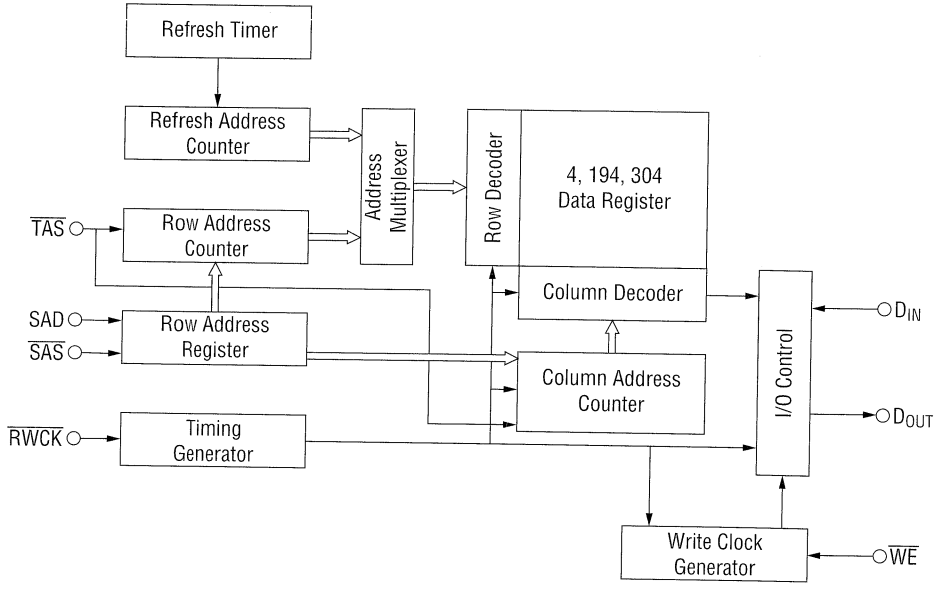
The device is packaged in 26/20-pin SOJ having a width of 300 mil.

It is well adapted for storing much data by means of a battery backup. Its combination with our recording and playback LSI enables the easy implementation of a solid recording and playback system.

FEATURES

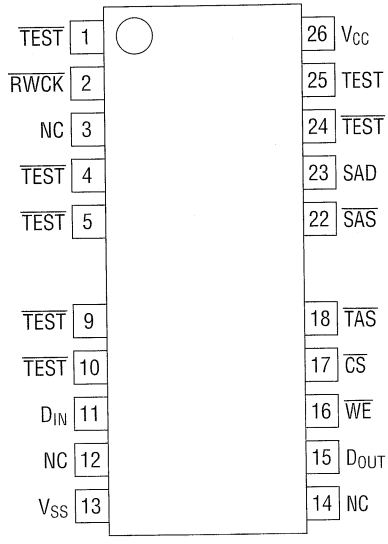
- Configuration
  4,194,304 x 1 bit
- Serial access operation
  Serial access time : 1.5 µs
  Serial read/write time : 2.5 µs
- Low current drain
  150 µA max. (V_{CC} = 4 V with data stored and under standard conditions)
- Refresh operation
  A self-refresh function is supported.
- Wide operation voltage range
  Single 3.5 to 5.5 V
- Addressing
  Units of 1024 words
- Process
  0.45 µm double well CMOS process
- Package
  26/20-pin plastic SOJ (SOJ26/20-P-300)
  (Product name : MSM6684BJS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

26/20-pin plastic SOJ



Note: Leave the NC pin open.

PIN DESCRIPTION

Pin name	Description
TEST	Test input
$\overline{\text{TEST}}$	Test input
$\overline{\text{RWCK}}$	Read/write clock
NC	Not connected
D_{IN}	Data input
V_{SS}	Ground (0 V)
D_{OUT}	Data output
$\overline{\text{WE}}$	Write enable
$\overline{\text{CS}}$	Chip select
$\overline{\text{TAS}}$	Transfer address strobe
$\overline{\text{SAS}}$	Serial address strobe
SAD	Serial address data
V_{CC}	Power supply (5 V)

Note : All $\overline{\text{TEST}}$ pins are to be connected to the power supply.
The TEST pin is to be referenced to the ground level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Pin Voltage	V_T	Against V_{SS} at Ta = 25 °C	−1.0 to +7.0	V
Output Short-Circuit Current	I_{OS}	Ta = 25 °C	50	mA
Power Dissipation	P_D	Ta = 25 °C	1	W
Operating Temperature	T_{op}	—	0 to +50	°C
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.5	4.5	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.2	V
"L" Input Voltage	V_{IL}	−0.2	0	0.5	V

ELECTRICAL CHARACTERISTICS

DC characteristics

(V_{CC}=3.5 V to 5.5 V, Ta=0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH}=−0.5 mA	V_{CC} − 0.5	—	V
"L" Output Voltage	V_{OL}	I_{OL}=0.5 mA	—	0.4	V
Input Leakage Current	I_{IL}	V_I=0 V to V_{CC}	−1	1	µA
Output Leakage Current	I_{OL}	V_O=0 V to V_{CC}	−1	1	µA
Supply Current (Operation)	I_{CC1}	V_{CC}=4 V, t_{RWC}=1 µs	—	20	mA
Supply Current (Standby)	I_{CC2}	V_{CC}=4 V	—	150	µA

OKI Semiconductor

MSM66V84B

4,194,304-word x 1-bit Serial Register

GENERAL DESCRIPTION

MSM66V84B is a serial register organized as 4,194,304 words x one bit, characterized by medium-speed, low power consumption operation.

This device has a built-in internal address generation circuit. Triggered off by a single external clock pulse, it provides serial, continuous read/write operations.
Read/write operation causes the internal address to be incremented automatically by +1.

External address input enables addressing in units of 1024 words. Furthermore, a refresh timer and a refresh address counter are installed, which makes an external refresh circuit unnecessary. In addition, this configuration allows lower power consumption.

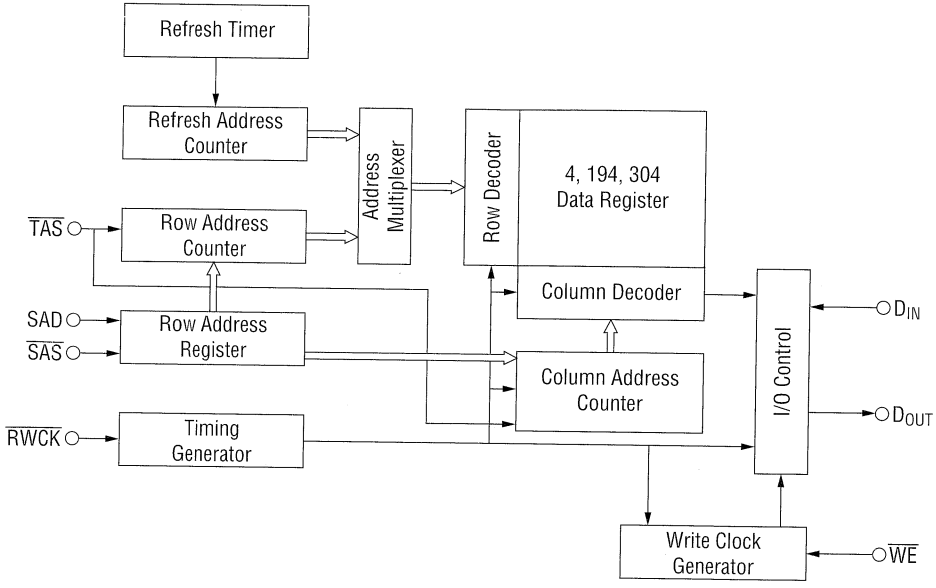
The device is packaged in 26/20-pin SOJ or 26/20 TSOP having a width of 300 mil.

It is well adapted for storing much data by means of a battery backup. Its combination with our recording and playback LSI enables the easy implementation of a solid recording and playback system.

FEATURES

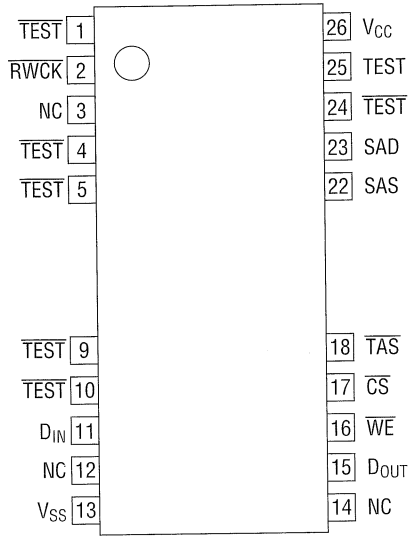
- Configuration
  4,194,304 x 1 bit
- Serial access operation
  Serial access time : 1.5 µs
  Serial read/write time : 2.5 µs
- Low current drain
  100 µA max. (V_{CC} = 3.6 V with data stored and under standard conditions)
- Refresh operation
  A self-refresh function is supported.
- Wide operation voltage range
  Single 2.7 to 3.6 V
- Addressing
  Units of 1024 words
- Process
  0.45 µm double well CMOS process
- Package
  26/20-pin plastic SOJ (SOJ26/20-P-300) (Product name : MSM66V84BJS)
  26/20-pin plastic TSOP (TSOP26/20-P-300-K) (Product name : MSM66V84BTS-K)

BLOCK DIAGRAM

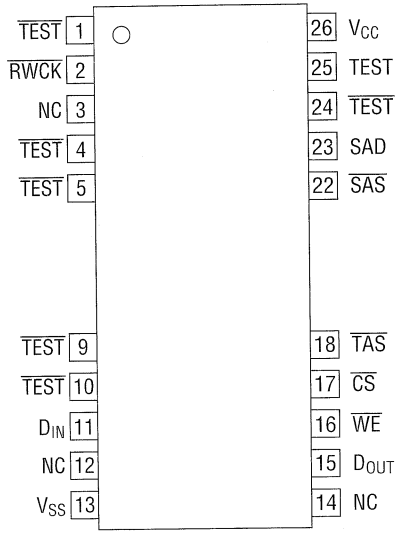


PIN CONFIGURATION (TOP VIEW)

26/20-pin plastic SOJ



26/20-pin plastic TSOP (K type)



Note: Leave the NC pin open.

PIN DESCRIPTION

Pin name	Description
TEST	Test input
$\overline{\text{TEST}}$	Test input
$\overline{\text{RWCK}}$	Read/write clock
NC	Not connected
D_{IN}	Data input
V_{SS}	Ground (0 V)
D_{OUT}	Data output
$\overline{\text{WE}}$	Write enable
$\overline{\text{CS}}$	Chip select
$\overline{\text{TAS}}$	Transfer address strobe
$\overline{\text{SAS}}$	Serial address strobe
SAD	Serial address data
V_{CC}	Power supply (2.7 V to 3.6 V)

Note : All $\overline{\text{TEST}}$ pins are to be connected to the power supply.
The TEST pin is to be referenced to the ground level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Pin Voltage	V_T	Against V_{SS} at Ta = 25 °C	−0.5 to +4.6	V
Output Short-Circuit Current	I_{OS}	Ta = 25 °C	50	mA
Power Dissipation	P_D	Ta = 25 °C	1	W
Operating Temperature	T_{op}	—	0 to +70	°C
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	V_{CC} − 0.3	V_{CC}	V_{CC} + 0.2	V
"L" Input Voltage	V_{IL}	−0.2	0	0.5	V

ELECTRICAL CHARACTERISTICS

DC characteristics

(V_{CC}=2.7 V to 3.6 V, Ta=0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH}=−0.1 mA	V_{CC} − 0.5	—	V
"L" Output Voltage	V_{OL}	I_{OL}=0.1 mA	—	0.4	V
Input Leakage Current	I_{IL}	V_I=0 V to V_{CC}	−1	1	µA
Output Leakage Current	I_{OL}	V_O=0 V to V_{CC}	−1	1	µA
Supply Current (Operation)	I_{CC1}	V_{CC}=3.6 V, t_{RWC}=2.5 µs	—	10	mA
Supply Current (Standby)	I_{CC2}	V_{CC}=3.6 V	—	100	µA

OKI Semiconductor

MSM6685

8,388,608-Word x 1-Bit Serial Register

GENERAL DESCRIPTION

The MSM6685 is a serial register composed of 8,388,608 words x one bit, characterized by medium-speed, low power consumption operation.

This device has a built-in internal address generation circuit. Triggered off by a single external clock pulse, it provides serial, continuous read/write operations. Read/write operation causes the internal address to be incremented automatically by +1.

External address input enables addressing in units of 1024 words. Furthermore, a refresh timer and a refresh address counter are installed, which makes an external refresh circuit unnecessary. In addition, this configuration allows lower power consumption.

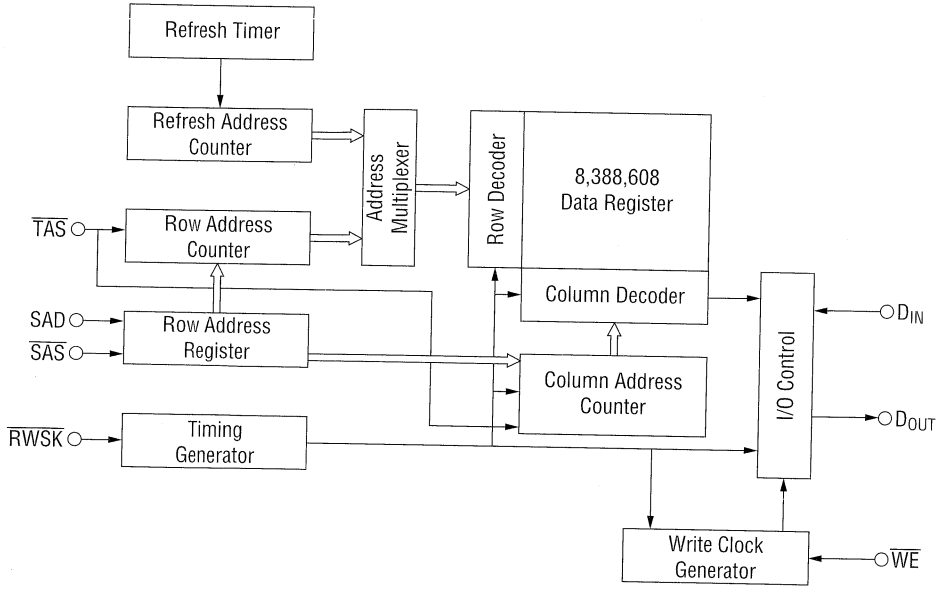
The device is packaged in 26-pin SOJ having a width of 300 mil.

It is well adapted for storing much data by means of a battery backup. Its combination with OKI's recording and playback IC enables the easy implementation of a solid recording and playback system.

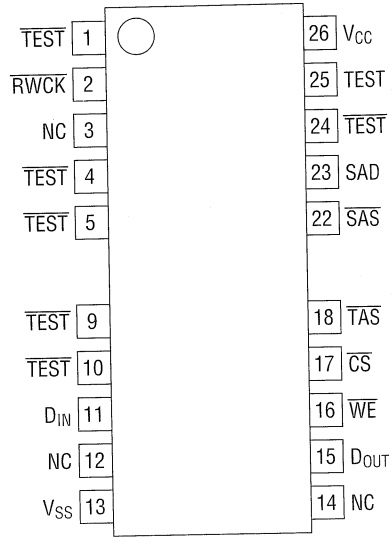
FEATURES

- Configuration : 8,388,608 × 1 bit
- Serial access operation
  - Serial access time : 1.5 µs
  - Serial read/write time : 2.5 µs
- Low current drain : 200 µA max. (V_{CC} = 4 V, at refresh operation, with data stored and under standard conditions)
- Refresh operation
  - A self-refresh function is supported.
- Wide range of operating voltage : Single 3.5 to 5.5 V supply
- Addressing : In units of 1024 words
- Process : 0.5 µm double well CMOS process
- Package:
  - 26/20-pin plastic SOJ (SOJ26/20-P-300) (Product name : MSM6685JS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



26/20-Pin Plastic SOJ

Note: Leave the NC pin open.

PIN DESCRIPTION

Symbol	Description
TEST	Test input
$\overline{\text{TEST}}$	Test input
$\overline{\text{RWCK}}$	Read/write clock
NC	Not connected
D_{IN}	Data input
V_{SS}	Ground (0 V)
D_{OUT}	Data output
$\overline{\text{WE}}$	Write enable
$\overline{\text{CS}}$	Chip select
$\overline{\text{TAS}}$	Transfer address strobe
$\overline{\text{SAS}}$	Serial address strobe
SAD	Serial address data
V_{CC}	Power supply (5 V)

Note : All $\overline{\text{TEST}}$ pins are to be connected to the power supply.
The TEST pin is to be referenced to the ground level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Pin Voltage	V_T	Against V_{SS} at Ta = 25 °C	−1.0 to +7.0	V
Short-circuit Output Current	I_{OS}	Ta = 25 °C	50	mA
Power Dissipation	P_D	Ta = 25 °C	1	W
Operating Temperature	T_{op}	—	0 to 70	°C
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.5	4.5	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.2	V
"L" Input Voltage	V_{IL}	−0.2	0	0.5	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC}=3.5V to 5.5V, Ta=0 to +70°C)

Parameter	Symbol	Condition	Min	Max	Unit
"H" Output Voltage	V_{OH}	I_{OH}=−0.5 mA	V_{CC} − 0.5	—	V
"L" Output Voltage	V_{OL}	I_{OL}=0.5 mA	—	0.4	V
Input Leakage Current	I_{IL}	V_I=0 V to V_{CC}	−1	1	µA
Output Leakage Current	I_{OL}	V_O=0 V to V_{CC}	−1	1	µA
Supply Current (Operation)	I_{CC1}	V_{CC}=4 V, t_{RWC}=1 µs	—	20	mA
Supply Current (Standby)	I_{CC2}	V_{CC}=4 V	—	200	µA

MSM6595A-xxx

1-Mbit Serial Voice ROM

GENERAL DESCRIPTION

The MSM6595A is a MSM6595 short TAT process version.
The MSM6595A is a serial voice ROM with a 1,048,576-word × 1-bit configuration.
The MSM6595A has a built-in internal address-generating circuit. A single, external clock input allows continuous, serial read operations. The internal addresses are automatically incremented by 1 by read operation. 1024 words in X direction and 1024 words in Y direction can be addressed by inputting external serial addresses. A read and playback device with predetermined messages can easily be configured by storing voice data into the MSM6595A and by combining it with one of Oki's recording ICs and a serial register IC.

A serial register is required to drive the MSM6595A by the MSM6388 or MSM6588. (The MSM6595A does not operate without a serial register.)

The major differences between the MSM6595A and MSM6595 are shown below.

MSM6595A DC Characteristics

V_{DD}=3.5 to 5.5 V, Ta=–40 to +85°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Current consumption (1)	I_{DD}	t_{RDC}=2.5 µs		—	9	20	mA
Current consumption (2)	I_{DS}	$\overline{CS}$= V_{DD}–0.2 V	Ta=–40 to +70°C	—	—	10	µA
			Ta=–40 to +85°C	—	—	50	

Typical values are at V_{DD}=5.0 V, Ta=25°C.

MSM6595 DC Characteristics

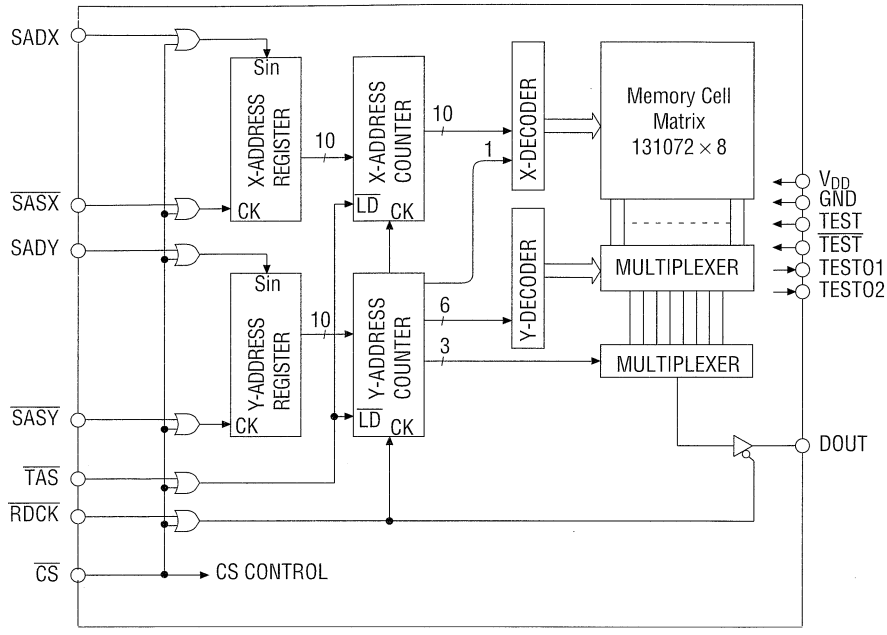
V_{DD}=3.5 to 5.5 V, Ta=–40 to +85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current consumption (1)	I_{DD}	t_{RDC}=2.5 µs	—	—	15	mA
Current consumption (2)	I_{DS}	$\overline{CS}$=V_{DD}–0.2 V	—	—	10	µA

FEATURES

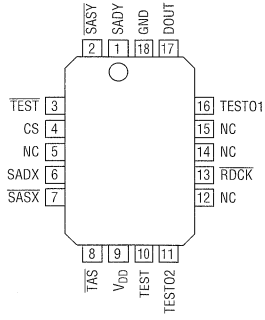
- Configuration : 1,048,576 words × 1 bit
- Serial access : Read cycle time of 2.5 ms
- Shorter-TAT processing
- Power-supply voltage : V single supply
- Package options : 18-pin plastic QFJ (QFJ18-P-R290)
  (Product Name : MSM6595A-xxxJS)
  24-pin plastic SOP (SOP24-P-430-K)
  (Product Name : MSM6595A-xxxGS-K)
  18-pin plastic DIP (DIP18-P-300)
  (Product name : MSM6595A-xxxRS)
  xxx indicates the code number

BLOCK DIAGRAM



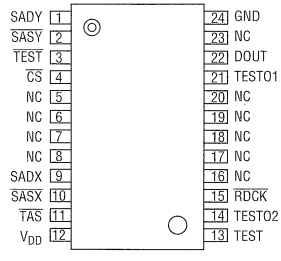
PIN CONFIGURATIONS (TOP VIEW)

MSM6595A-xxxJS



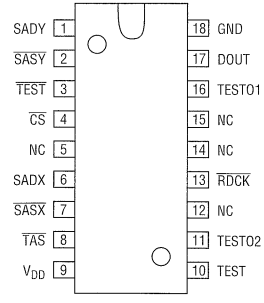
18-Pin Plastic LCC

MSM6595A-xxxGS-K



24-Pin Plastic SOP

MSM6595A-xxxRS



18-Pin Plastic DIP

PIN DESCRIPTIONS

Symbol	Type	Description
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and the GND pin.
GND	—	Ground pin
SADX	I	(SERIAL ADDRESS) This pin inputs the starting X address of a read operation. Addressing in units of 1024 words is possible. The 1024-word address data can be input as 10-bit (AX0 - AX9) serial data via the SADX pin.
SADY	I	(SERIAL ADDRESS) This pin inputs the starting Y address of a read operation. Addressing in units of 1024 words is possible. The 1024-word address data can be input as 10-bit (AY0 - AY9) serial data via the SADY pin.
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) This is the clock input pin which is used to store the serial address data of the X address into the device's internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROBE) This is the clock input pin to store the serial address data of the Y address into the device's internal register.
$\overline{TAS}$	I	(ADDRESS TRANSFER STROBE) This is the input pin for loading the serial address data into the internal address counter. The X and Y addresses are stored at the falling edge of $\overline{TAS}$.
$\overline{RDCK}$	I	(READ CLOCK) This is the clock input pin for reading information out of the data register. Internal operation starts at the falling edge of $\overline{RDCK}$. The information in the data register is output on the DOUT pin. The internal address counter is automatically incremented at the falling edge of $\overline{RDCK}$.
DOUT	O	(DATA OUT) The data output pin is always kept in a high-impedance state when $\overline{RDCK}$ or $\overline{CS}$ is kept at "H". This pin reflects the "H" or "L" level data being read, and the current data is held until $\overline{RDCK}$ is asserted High.
$\overline{CS}$	I	(CHIP SELECT) Setting this pin to "H" disables all input and output pins. This pin enables parallel use of multiple serial voice ROMs by connecting the data output pins.
TEST $\overline{TEST}$	I	Pins for testing. Apply a "L" level to the TEST pin and "H" level to the $\overline{TEST}$ pin.
TEST01 TEST02	O	Pins for testing. Leave these pins open.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	GND=0 V	+3.5 to +5.5	V
Operating Temperature	T_{op}	—	−40 to +85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

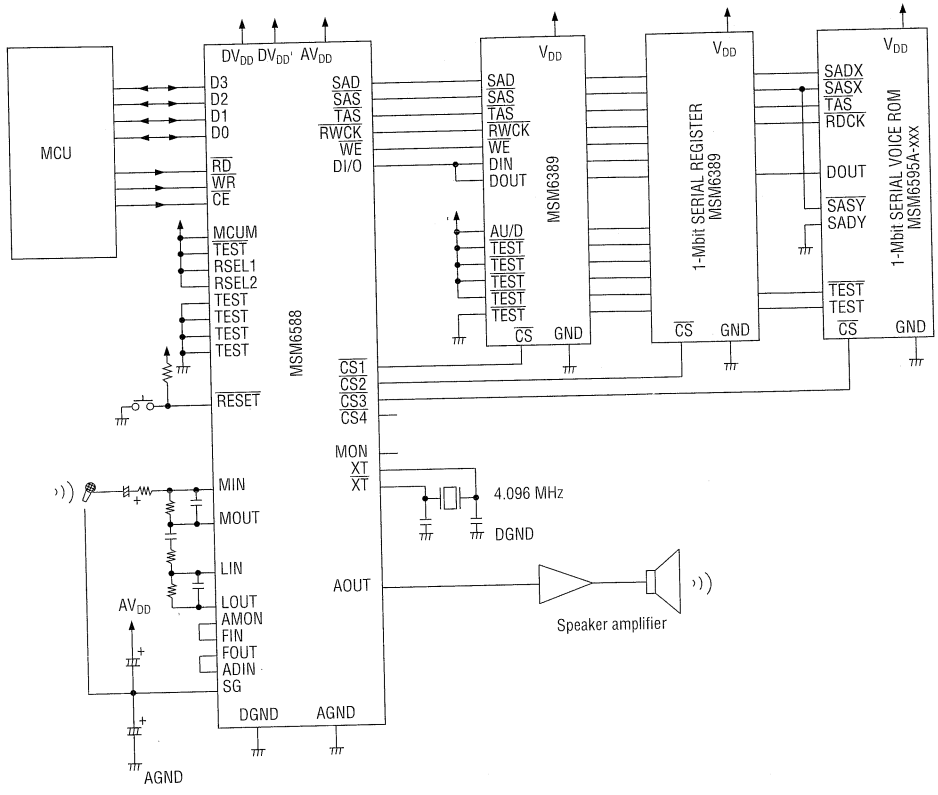
V_{DD}=3.5 to 5.5 V, Ta=−40 to +85°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
"H" Level Input Voltage	V_{IH}	—		0.8xV_{DD}	—	—	V
"L" Level Input Voltage	V_{IL}	—		—	—	0.8	V
"H" Level Output Voltage	V_{OH}	I_{OH}=−40 µA		V_{DD}−0.3	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL}=2 mA		—	—	0.45	V
"H" Level Input Current	I_{IH}	V_{IH}=V_{DD}		—	—	10	µA
"L" Level Input Current	I_{IL}	V_{IL}=GND		−10	—	—	µA
Current Consumption (1)	I_{DD}	t_{RDC}=2.5 µs		—	9	20	mA
Current Consumption (2)	I_{DS}	$\overline{CS}$= V_{DD}−0.2 V	Ta=−40 to +70°C	—	—	10	µA
			Ta=−40 to +85°C	—	—	50	

Typical values are at V_{DD} = 5.0 V, Ta = 25°C.

APPLICATION CIRCUIT

Operation with the MSM6588



Note: When the MSM6595A is driven by the MSM6388 or MSM6588, a serial register is required. (The MSM6595A does not operate without it.) The MSM6389 is being used as the serial register in the above example.

MSM6596A-xxx

2-Mbit Serial Voice ROM

GENERAL DESCRIPTION

The MSM6596A is the shorter-TAT processing version of the MSM6596.
The MSM6596A is a serial voice ROM with a 1,048,576-word × 1-bit × 2-bank configuration.
The MSM6596A has a built-in internal address-generating circuit. A single, external clock input allows continuous, serial read operations. The internal addresses are automatically incremented by 1 by read operation. 1024 words in X direction and 1024 words in Y direction can be addressed by inputting external serial addresses. Banks are switched with $\overline{CS1}$ and $\overline{CS2}$.
A read and playback device with predetermined messages can easily be configured by storing a voice data into the MSM6596A and or combining it with one of OKI's recording ICs and serial register IC.

A serial register is required to drive the MSM6596A by the MSM6388 or MSM6588. (The MSM6596A does not operate without a serial register.)

The major functional differences between the MSM6596A and MSM6596 are shown below.

MSM6596A DC Characteristics

V_{DD}=3.5 to 5.5 V, Ta=–40 to +85°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD}	t_{RDC}=2.5 µs		—	9	20	mA
Current consumption (2)	I_{DS}	$\overline{CS1}$=$\overline{CS2}$=V_{DD}–0.2 V	Ta=–40 to +70°C	—	—	10	µA
			Ta=–40 to +85°C	—	—	50	

Typical values are at V_{DD}=5.0 V, Ta=25°C.

MSM6596 DC Characteristics

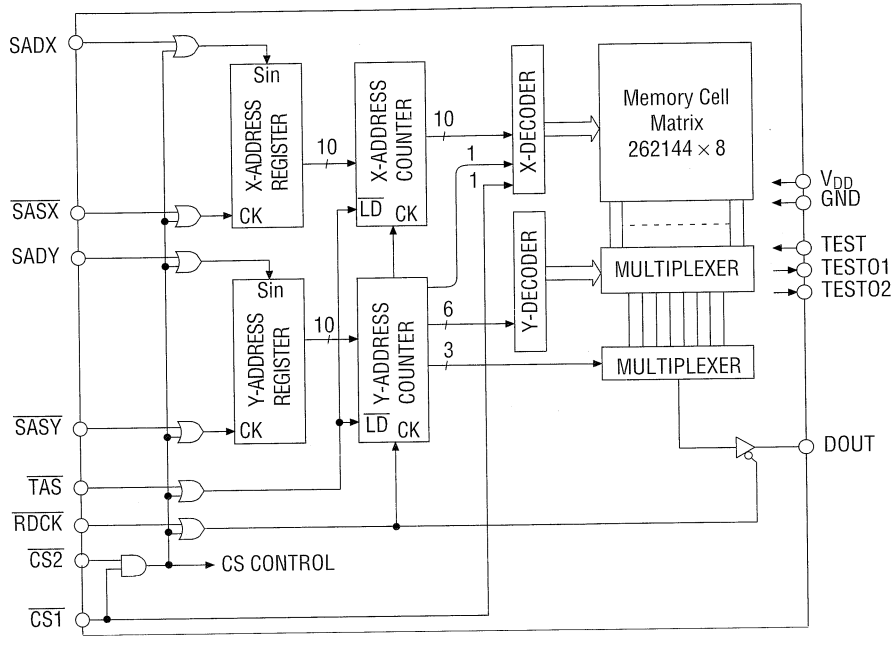
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD}	t_{RDC}=2.5 µs	—	—	15	mA
Current consumption (2)	I_{DS}	$\overline{CS1}$=$\overline{CS2}$=V_{DD}–0.2 V	—	—	10	µA

Typical values are at V_{DD}=5.0 V, Ta=25°C.

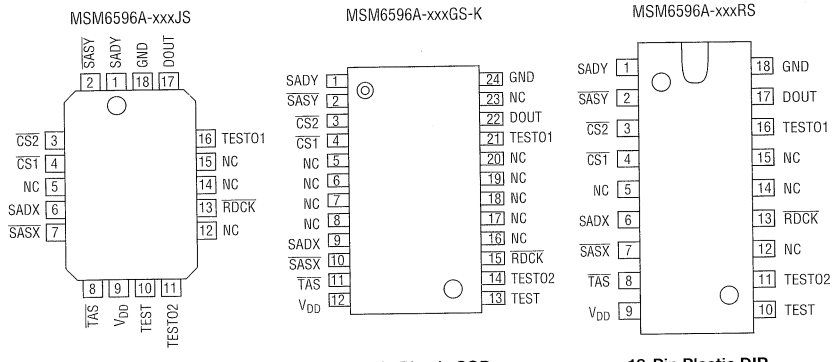
FEATURES

- Configuration : 1,048,576 words × 1 bit × 2 banks
- Serial access : Read cycle time of 2.5 µs
- Shorter-TAT processing
- Power-supply voltage : 5 V single supply
- Package options : 18-pin plastic QFJ (QFJ18-P-R290)
  (Product Name : MSM6596A-xxxJS)
  24-pin plastic SOP (SOP24-P-430-K)
  (Product Name : MSM6596A-xxxGS-K)
  18-pin plastic DIP (DIP18-P-300)
  (Product name : MSM6596A-xxxRS)

BLOCK DIAGRAM



PIN CONFIGURATIONS (TOP VIEW)



18-Pin Plastic LCC | 24-Pin Plastic SOP | 18-Pin Plastic DIP

PIN DESCRIPTIONS

Symbol	Type	Description
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and the GND pin.
GND	—	Ground pin
SADX	I	(SERIAL ADDRESS) This pin inputs the starting X address of a read operation. Addressing in units of 1024 words is possible. The 1024-word address data can be input as 10-bit (AX0 - AX9) serial data via the SADX pin.
SADY	I	(SERIAL ADDRESS) This pin inputs the starting Y address of a read operation. Addressing in units of 1024 words is possible. The 1024-word address data can be input as 10-bit (AY0 - AY9) serial data via the SADY pin.
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) This is the clock input pin which is used to store the serial address data of the X address into the device's internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROBE) This is the clock input pin which is used to store the serial address data of the Y address into the device's internal register.
$\overline{TAS}$	I	(TRANSFER ADDRESS STROBE) This is the input pin for loading the serial address data into the internal address counter. The X and Y addresses are stored at the falling edge of $\overline{TAS}$.
$\overline{RDCK}$	I	(READ CLOCK) This is the clock input pin for reading information out of the data register. Internal operation starts at the falling edge of $\overline{RDCK}$. The information in the data register is output on the DOUT pin. The internal address counter is automatically incremented at the falling edge of $\overline{RDCK}$.
DOUT	O	(DATA OUT) The data output pin is always kept in a high-impedance state when $\overline{RDCK}$ or $\overline{CS}$ is kept "H". This pin reflects the "H" or "L" level data being read, and the current data is hold until $\overline{ROCK}$ is asserted "H".
$\overline{CS1}$ $\overline{CS2}$	I	(CHIP SELECT) When CS1 is set to "L", bank 1 is selected. When CS2 is set to "L", bank 2 is selected. Setting both CS1 and CS2 to "H" disables all input and output pins. These pins enable parallel use of multiple serial voice ROMs by connecting the data output pins.
TEST	I	Pin for testing. Apply a "L" level.
TEST01 TEST02	O	Pins for testing. Leave these pins open.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	GND=0 V	+3.5 to +5.5	V
Operating Temperature	T_{op}	—	−40 to +85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

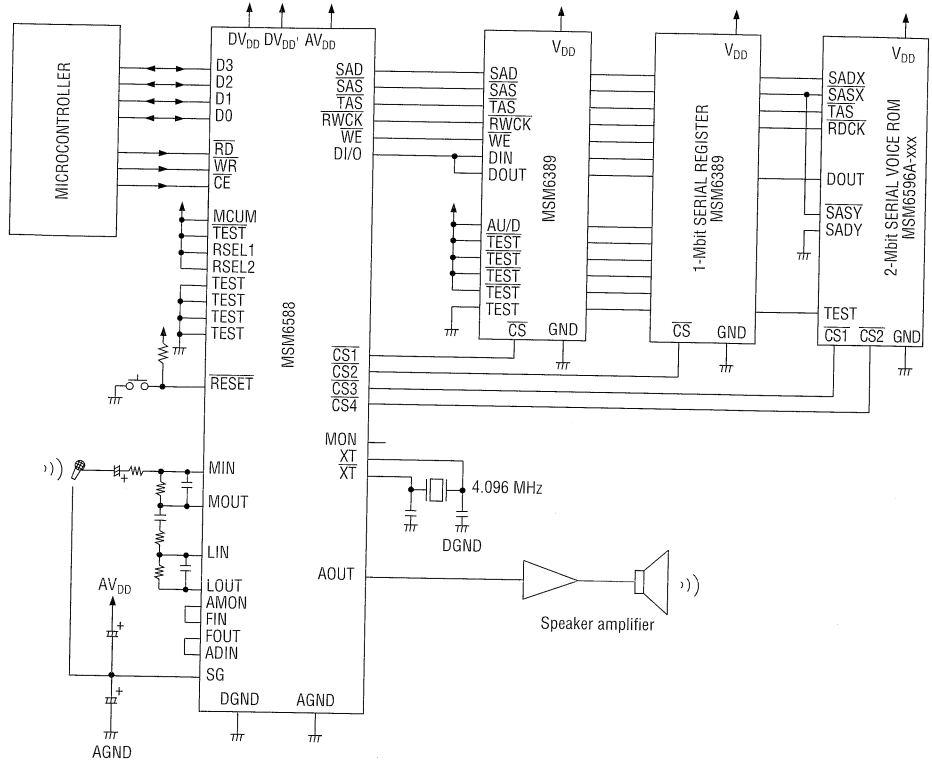
V_{DD}=3.5 to 5.5 V, Ta=−40 to +85°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
"H" Level Input Voltage	V_{IH}	—		0.8xV_{DD}	—	—	V
"L" Level Input Voltage	V_{IL}	—		—	—	0.8	V
"H" Level Output Voltage	V_{OH}	I_{OH}=−40 µA		V_{DD}−0.3	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL}=2 mA		—	—	0.45	V
"H" Level Input Current	I_{IH}	V_{IH}=V_{DD}		—	—	10	µA
"L" Level Input Current	I_{IL}	V_{IL}=GND		−10	—	—	µA
Current Consumption (1)	I_{DD}	t_{RDC}=2.5 µs		—	9	20	mA
Current Consumption (2)	I_{DS}	$\overline{CS1}$=$\overline{CS2}$=V_{DD}−0.2 V	Ta=−40 to +70°C	—	—	10	µA
			Ta=−40 to +85°C	—	—	50	

Typical values are at V_{DD}=5.0 V, Ta=25°C.

APPLICATION CIRCUIT

MSM6588 Playback Storage Example



Note: When the MSM6596A is driven by the MSM6388 or MSM6588, a serial register is required. (The MSM6596A does not operate without it.) The MSM6389 is being used as the serial register in the above example.

MSM6597A-xxx

3-Mbit Serial Voice ROM

GENERAL DESCRIPTION

The MSM6597A is a MSM6597 short TAT process version.
The MSM6597A is a serial voice ROM with a 1,048,576-word × 1-bit × 3-bank configuration.
The MSM6597A has a built-in internal address-generating circuit. A single, external clock input allows continuous, serial read operations. The internal addresses are automatically incremented by 1 by read operation. 1024 words in X direction and 1024 words in Y direction can be addressed by inputting external serial addresses. Banks are switched with $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$.
A read and playback device with predetermined messages can easily be configured by storing voice data into the MSM6597A and by combining it with one of Oki's recording ICs and with one of Oki's serial registers.

A serial register is required to drive the MSM6597A when used with the MSM6388 or MSM6588. (The MSM6597A does not operate without a serial register.)

The major differences between the MSM6597A and MSM6597 are shown below.

MSM6597A DC Characteristics

V_{DD}=3.5 to 5.5 V, Ta=–40 to +85°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Current Consumption (1)	I_{DD}	t_{RDC}=2.5 µs		—	9	20	mA
Current Consumption (2)	I_{DS}	$\overline{CS1}$=$\overline{CS2}$=$\overline{CS3}$ =V_{DD}–0.2 V	Ta=–40 to +70°C	—	—	10	µA
			Ta=–40 to +85°C	—	—	50	

MSM6597 DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption (1)	I_{DD}	t_{RDC}=2.5 µs	—	—	15	mA
Current Consumption (2)	I_{DS}	$\overline{CS1}$=$\overline{CS2}$=$\overline{CS3}$=V_{DD}–0.2 V	—	—	10	µA

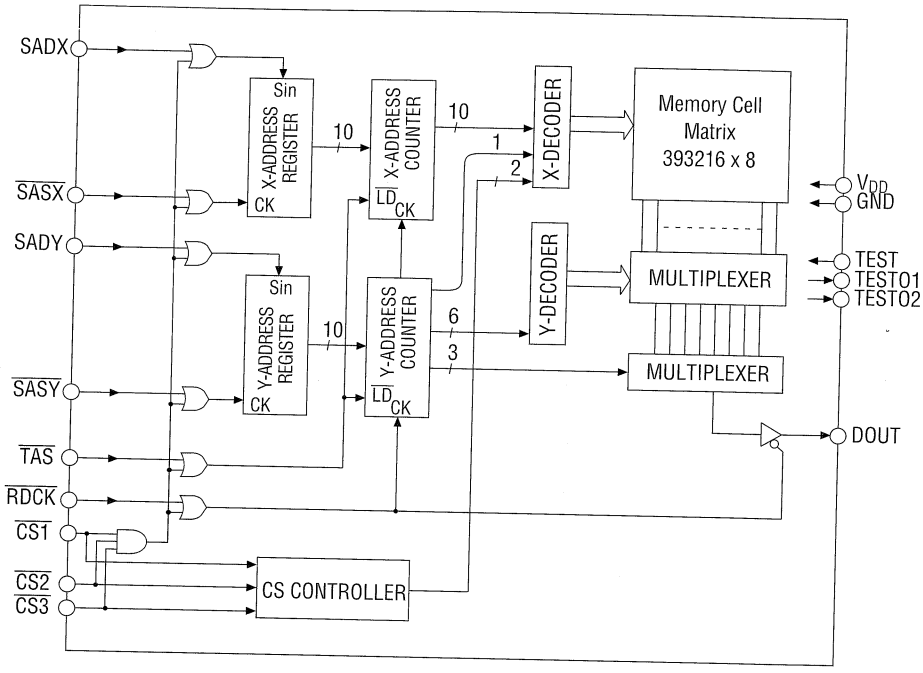
Typical values are at V_{DD} = 5.0 V, Ta = 25°C

For other detailes, refer to individual sections in this data sheet.

FEATURES

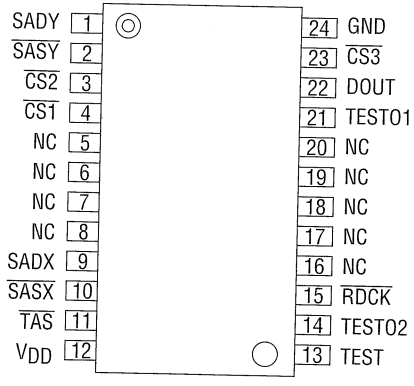
- Configuration : 1,048,576 words × 1 bit × 3 banks
- Serial access : Read cycle time of 2.5 µs
- Shorter-TAT processing
- Power-supply voltage : 5 V single supply
- Package:
  24-pin plastic SOP (SOP24-P-430-K) (Product name : MSM6597A-xxxGS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

MSM6597A-xxxGS-K



24-Pin Plastic SOP

NC: No-connection pin

PIN DESCRIPTIONS

Symbol	Type	Description
V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 µF or more between this pin and the GND pin.
GND	—	Ground pin
SADX	I	(SERIAL ADDRESS) This pin inputs the starting X address of a read operation. Addressing in units of 1024 words is possible. The 1024-word address data can be input as 10-bit (AX0 - AX9) serial data via the SADX pin.
SADY	I	(SERIAL ADDRESS) This pin inputs the starting Y address of a read operation. Addressing in units of 1024 words is possible. The 1024-word address data can be input as 10-bit (AY0 - AY9) serial data via the SADY pin.
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) This is the clock input pin which is used to store the serial address data of the X address into the device's internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROBE) This is the clock input pin which is used to store the serial address data of the Y address into the device's internal register.
$\overline{TAS}$	I	(ADDRESS TRANSFER STROBE) This is the input pin for loading the serial address data into the internal address counter. The X and Y addresses are stored at the falling edge of $\overline{TAS}$.
$\overline{RDCK}$	I	(READ CLOCK) This is the clock input pin for reading information out of the data register. Internal operation starts at the falling edge of $\overline{RDCK}$. The information in the data register is output on the DOUT pin. The internal address counter is automatically incremented by 1 at the falling edge of $\overline{RDCK}$.
DOUT	O	(DATA OUT) The data output pin is always kept in a high-impedance state when $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ are all kept "H" or when $\overline{RDCK}$ is kept "H". This pin reflects the "H" or "L" level data being read, and the current data is hold until $\overline{RDCH}$ is asserted High.
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$	I	(CHIP SELECT) When either $\overline{CS1}$, $\overline{CS2}$, or $\overline{CS3}$ is "L", bank 1, bank 2, or bank 3 is selected, respectively. Setting all three signals "H" disables all input and output pins. These pins enable parallel use of multiple serial voice ROMs by connecting the data output pins.
TEST	I	Pin for testing. Apply "L" level.
TEST01 TEST02	O	Pins for testing. Leave these pins open.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	−0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	−0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	GND=0V	+3.5 to +5.5	V
Operating Temperature	T_{op}	—	−40 to +85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

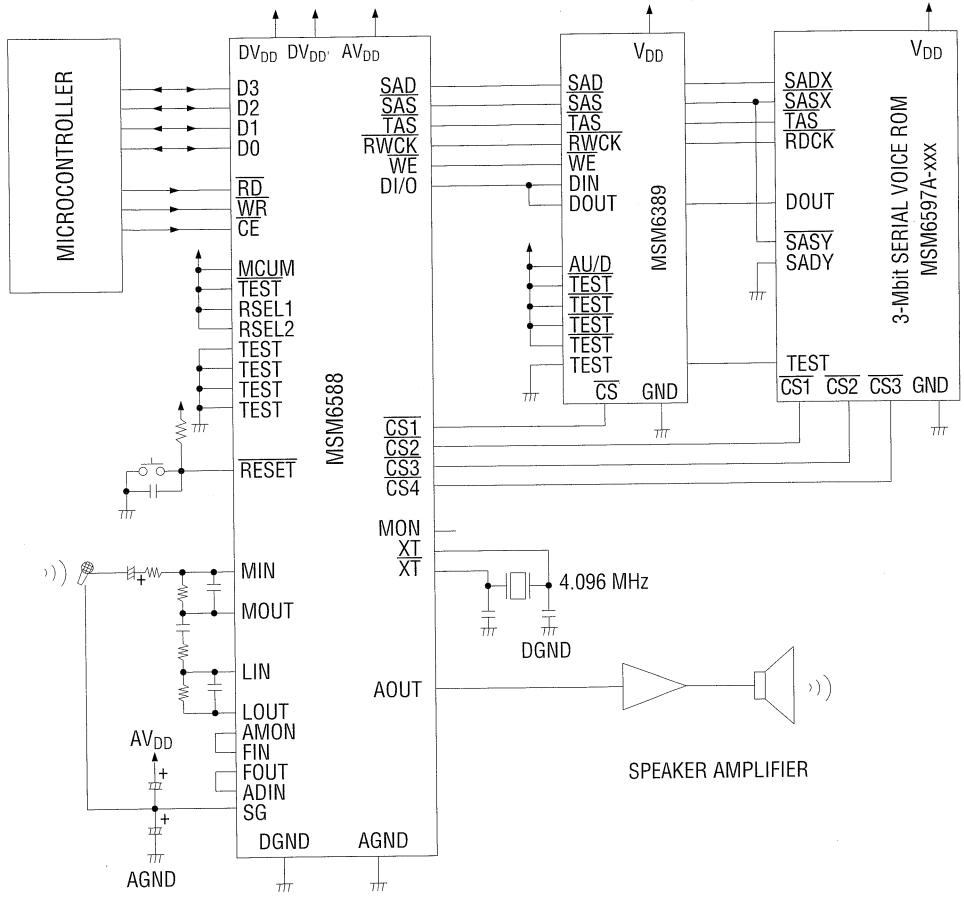
V_{DD}=3.5 to 5.5 V, Ta=−40 to +85°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
"H" Level Input Voltage	V_{IH}	—		0.8xV_{DD}	—	—	V
"L" Level Input Voltage	V_{IL}	—		—	—	0.8	V
"H" Level Output Voltage	V_{OH}	I_{OH}=−40 µA		V_{DD}−0.3	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL}=2 mA		—	—	0.45	V
"H" Level Input Current	I_{IH}	V_{IH}=V_{DD}		—	—	10	µA
"L" Level Input Current	I_{IL}	V_{IL}=GND		−10	—	—	µA
Current Consumption (1)	I_{DD}	t_{RDC}=2.5 µs		—	9	20	mA
Current Consumption (2)	I_{DS}	$\overline{CS1}$=$\overline{CS2}$=$\overline{CS3}$ =V_{DD}−0.2 V	Ta=−40 to +70°C	—	—	10	µA
			Ta=−40 to +85°C	—	—	50	

Typical values are at V_{DD}=5.0 V, Ta=25°C

APPLICATION CIRCUIT

MSM6588 Playback Storage Example



Note: When the MSM6597A is driven by the MSM6388 or MSM6588, a serial register is required. (The MSM6597A does not operate without it.)

DATA SHEET 4 INTERFACE ICs

OKI Semiconductor

MSM6690

ROM Interface IC

GENERAL DESCRIPTION

The MSM6690 can drive three devices of 131,072 x 8-bit EPROM or Mask ROM.

The MSM6690 contains a built-in internal address generator circuit and one external clock input that enables contiued serial read operations. The internal address counter is automatically incremented by one each read operation. The external serial address input allows 1,024 words to be addressed in the X-direction, and 1,024 words in the Y-direction.

* ROM is selected through $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ pins.

FEATURES

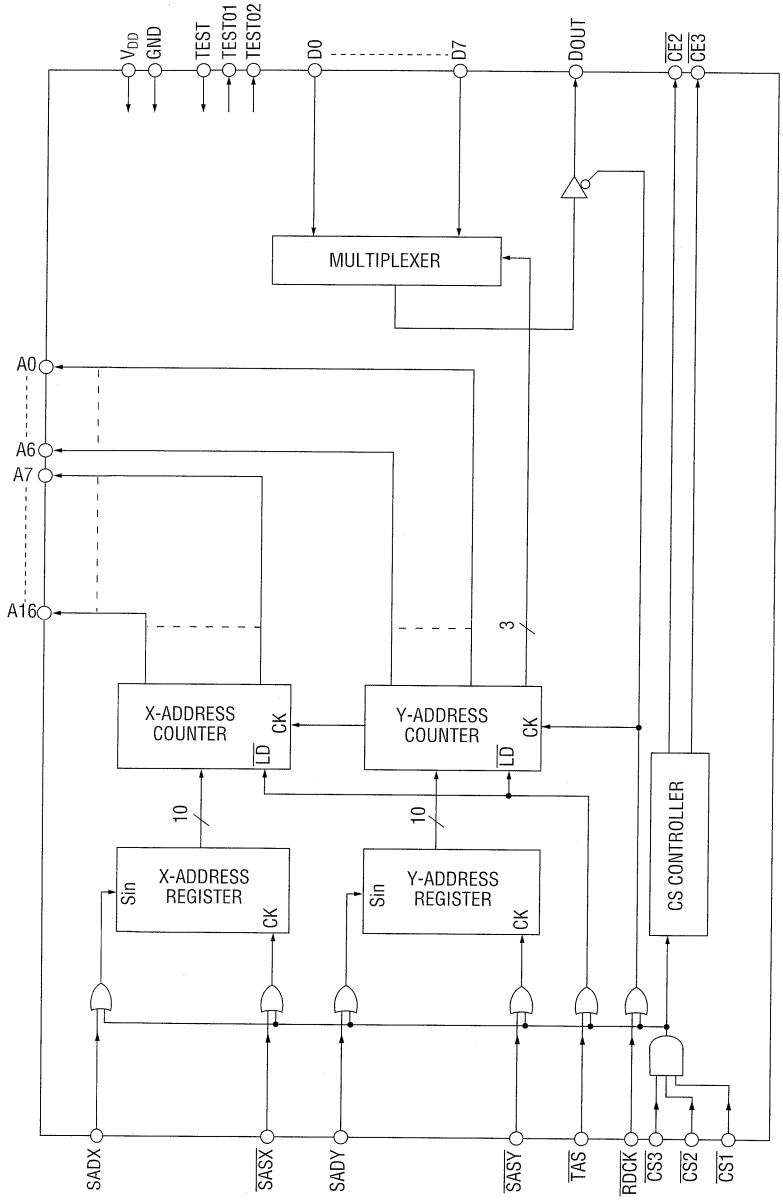
- Capable of driving three devices of 1 Mbit EPROM
- Capable of driving three devices of 1 Mbit Mask ROM
- Supply voltage : Single 5 V
- Package options : 42-pin plastic DIP (DIP42-P-600) (Product name: MSM6690RS)
  44-pin plastic QFP (QFP44-P-910-2K) (Product name: MSM6690GS-2K)

* Available combinations

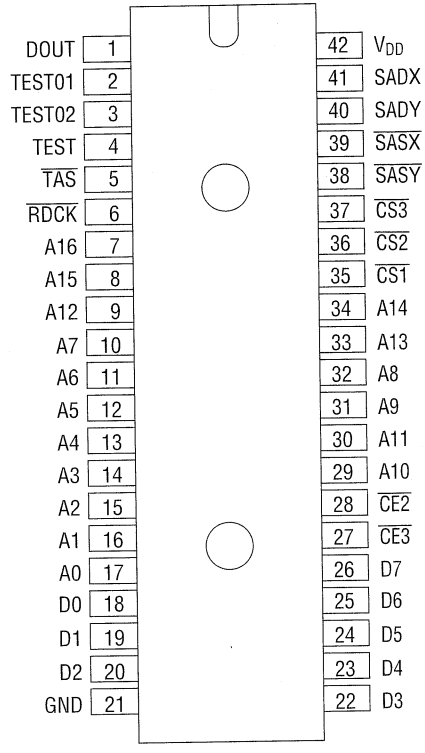
MSM6388/6588	MSM6688/6788/6789A
+	+
MSM6389/6587/6586	(MSM6684/6685)
+	+
MSM6690	MSM6690
+	+
ROM	ROM

Note: When driving the MSM6690 with the MSM6388 or the MSM6588, a serial register (MSM6389, MSM6688 or MSM6586) is required.
In the case of the MSM6688, MSM6788 and MSM6789A, a playback system can be constructed without a serial register (MSM6684 or MSM6685).

BLOCK DIAGRAM



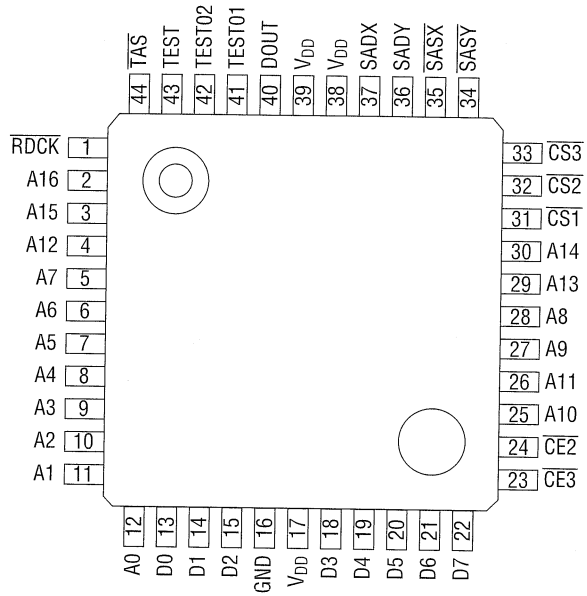
PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

5

PIN CONFIGURATION (TOP VIEW) (Continued)



44-Pin Plastic QFP

5

PIN DESCRIPTIONS

Symbol	Type	Description
V_{DD}	—	Power Supply
GND	—	Ground
SADX	I	(SERIAL ADDRESS) Starting X address. 1024 words are addressed, and 1024 address data can be input as serial data of 10 bit (AX0 to AX9) via SADX pin.
SADY	I	(SERIAL ADDRESS) Starting Y address. 1024 words are addressed, and 1024 address data can be input as serial data of 10 bit (AY0 to AY9) via SADY pin.
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) Clock to load X address's serial address data to internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROBE) Clock to load Y address's serial address data to internal register.
$\overline{TAS}$	I	(TRANSFER ADDRESS STROBE) Serial address data loaded in address register, to internal address counter. X address and Y address data are loaded at fall of $\overline{TAS}$ pin.
$\overline{RDCK}$	I	(READ CLOCK) Clock to read data in data register. Internal operation starts on falling edge of $\overline{RDCK}$, and data in the data register is output via DOUT pin. And internal address counter is automatically incremented by one due to the falling of $\overline{RDCK}$.
DOUT	O	(DATA OUT) In case $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are all at "H" level, or $\overline{RDCK}$ is at "H" level data output pin is always at high impedance state. When "H" level data or "L" level data is read out, output pin is set to "H" level or "L" level and its read data is kept until $\overline{RDCK}$ turns to "H" level.
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$	I	(CHIP SELECT) Three ROMS selection. $\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CE2}$ $\overline{CE3}$ L — — H H H L — L H H H L H L H H H H H When $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are all set to "H" level, all input/output pins become disabled. By use of these pins, three ROM data output pins can be connected in parallel.
$\overline{CE2}$ $\overline{CE3}$	O	(CHIP ENABLE) ROM enable. Connect it to ROM's $\overline{CE}$.
A0 - A16	O	(ADDRESS OUT) ROM address.
D0 - D7	I	(DATA IN) ROM data.
TEST	I	IC test. Input "L" level data.
TEST01 TEST02	O	IC test. Set to open.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C Typical: GND = 0 V	−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{DD}+0.3	V
Output Voltage	V_O		−0.3 to V_{DD}+0.3	V
Input Current	I_I		−10 to +10	mA
Output Current	I_O		−20 to +20	mA
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{DD}	+3.0 to +6.0	V
Operating Temperature	T_{op}	−40 to +85	°C

5

ELECTRICAL CHARACTERISTICS

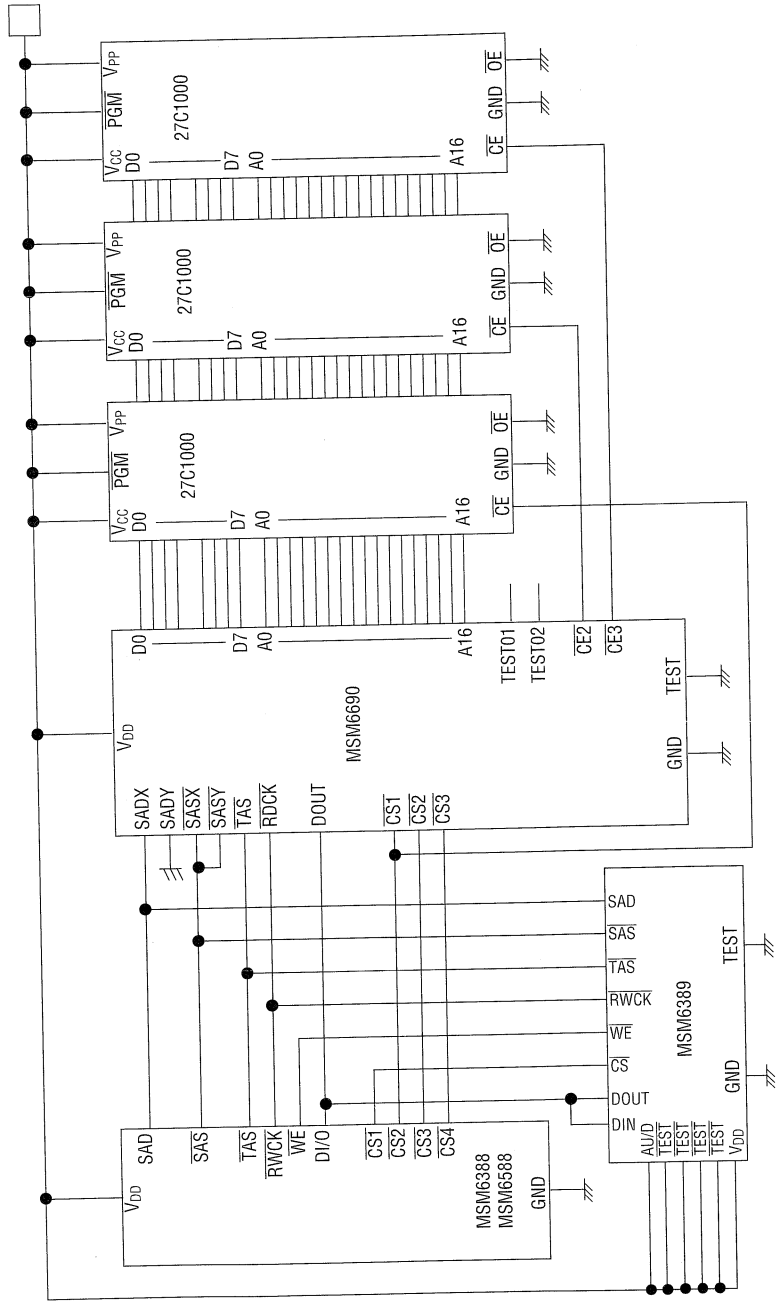
DC Characteristics

(V_{DD} = 5.0 V ± 10%, GND = 0 V, Ta = −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.*	Max.	Unit
"H" level Input Voltage	V_{IH}	CMOS level input	3.5	—	V_{DD}+0.3	V
"L" level Input Voltage	V_{IL}	CMOS level input	−0.3	—	1.5	V
"H" level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.01	10	µA
"L" level Input Current	I_{IL}	V_{IL} = GND	−10	−0.01	—	µA
3-state Output Leak Current (with open drain output)	I_{OZH}	$V_{OH} = V_{DD}$	—	0.01	10	µA
	I_{OZL}	V_{OL} = GND	−10	−0.01	—	
"H" level Output Voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	4.2	V_{DD}	V
"L" level Output Voltage	V_{OL}	I_{OL} = 5.0 mA	GND	0.24	0.5	V
Supply Current at Standby	I_{DS}	Output open $V_{IH} = V_{DD}$ V_{IL} = GND	—	0.1	100	µA
Supply Current at Operating	I_{DD}	—	—	—	2	mA

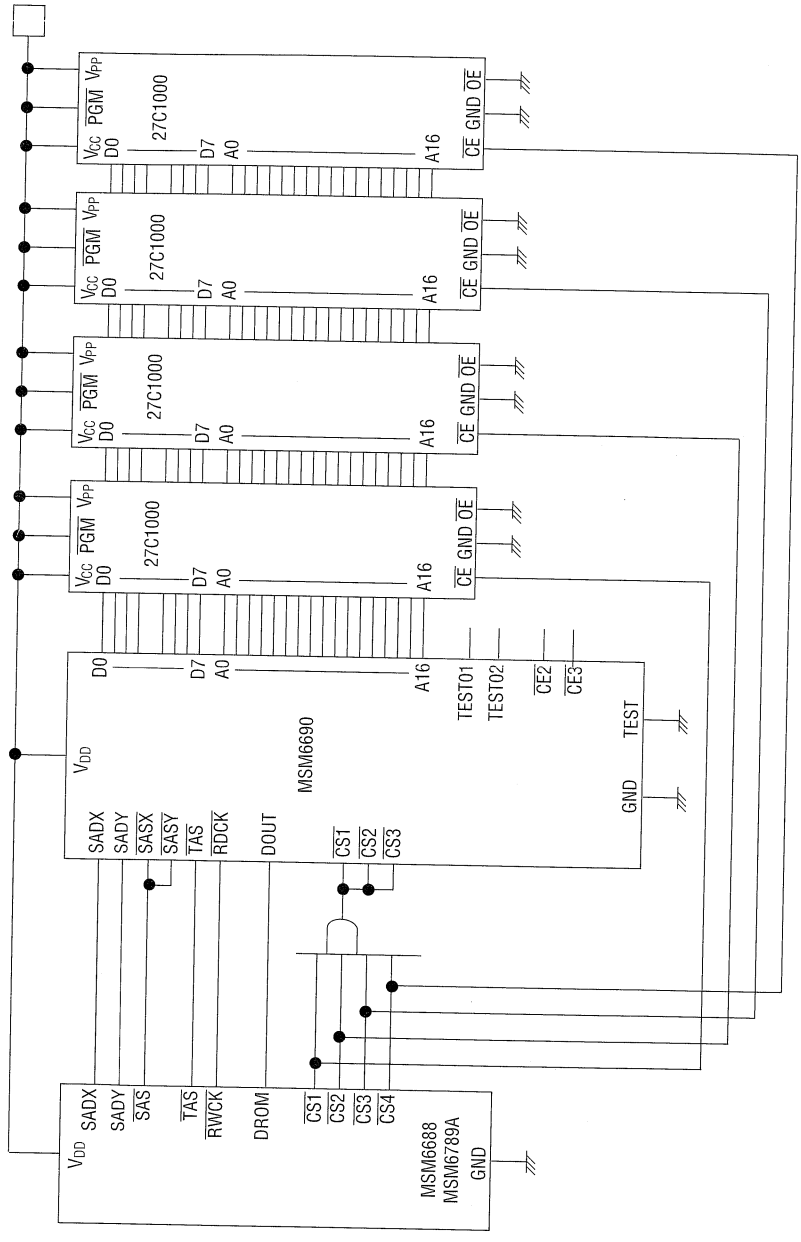
* Typical operation is with V_{DD} = 5.0 V, Ta = 25°C

APPLICATION CIRCUITS



Example of application circuit where MSM6388/6588,a 1-Mbit serial register, and three 1-Mbit EPROMs are connected.

APPLICATION CIRCUITS (Continued)



Example of application circuit where MSM6688/6789A and four 1-Mbit EPROMs are connected.

OKI Semiconductor

MSM6691

DRAM Interface IC

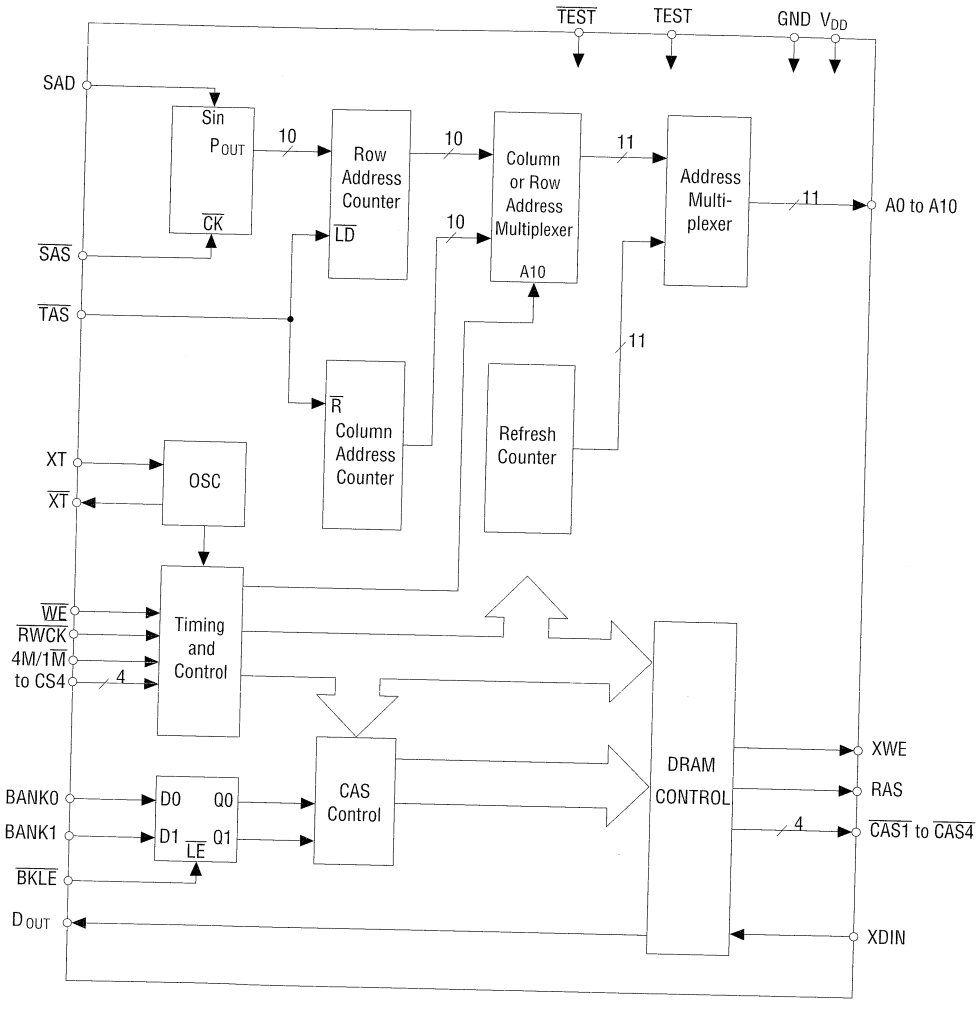
GENERAL DESCRIPTION

DRAMs can be used for voice storage by connecting the MSM6691 with OKI's integrate R/W (Read/Write) ICs, the MSM6388, and the MSM6588. The MSM6691 translates the signals associated with the dedicated serial register interface of the MSM6388 and MSM6588 driver interface when used in a stand-alone mode.

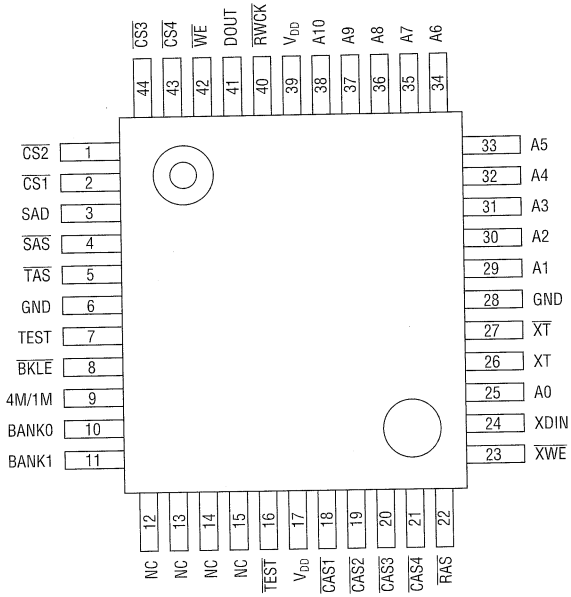
FEATURES

- DRAM (× 1-bit configuration)
- 1-Mbit DRAM (M 51100A, M511001A) : Four units can be used.
- 4-Mbit DRAM (M 514100A, M514101A) : Four units can be used.
- Power voltage : 5V single
- Built-in refresh circuit (RAS only refresh)
- Oscillation frequency : 8MHz (during refresh)
- Sampling frequency
- 4 kHz to 32 kHz when MSM6388 is connected.
- 4 kHz to 16 kHz when MSM6588 is connected.
- Package : 44-pin plastic QFP (QFP44-P-910-2K) (Product name : MSM6691GS-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

NC: No-connection pin

5

PIN DESCRIPTIONS

Symbol	Type	Description
V_{DD}	I	Power
GND	I	GND
XT	I	Oscillator
$\overline{XT}$	O	Oscillator
TEST	I	IC test. Set to "L".
$\overline{TEST}$	I	IC test. Set to "H".
SAD	I	Initial address of R/W
$\overline{SAS}$	I	Clock to input serial address data to internal register
$\overline{TAS}$	I	Load serial data, input to address register, and reset to internal address counter.
$\overline{RWCK}$	I	Clock to read and write data register information. At $\overline{RWCK}$ fall, internal operation starts. In read mode data input to XDIN is latched and output the DOUT terminal. In write mode, DIN (D I/O) output data MSM6388 (MSM6588) is input to the DIN pin of DRAM. At $\overline{RWCK}$ the fall internal address counter automatically increments, and address data is output from A_0 to A_{10}.
$\overline{WE}$	I	Select R/W modes
$\overline{XWE}$	O	Control DRAM
A0 to A10	O	Address control DRAM
$\overline{RAS}$	O	Control DRAM
$\overline{CAS1}$ $\overline{CAS2}$ $\overline{CAS3}$ $\overline{CAS4}$	O	Control DRAM
XDIN	I	Write data
DOUT	O	Read data
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	I	Chip select when 1-M DRAM is connected. Because input terminal to select most significant address when 4-M DRAM is connected.
4M/$\overline{1M}$	I	Select 4-M DRAM or 1-M DRAM for connection. "L" 1M DRAM connected; 4-M DRAM connected
BANK0 BANK1	I	Chip select data when 4-M DRAM is connedted. Terminal is used to select desired DRAM from DRAMs connected to select terminals. $\overline{CAS1}$ to $\overline{CAS4}$. Set to "L" when 1-M DRAM is connected.
$\overline{BKLE}$	I	Latch data, input to BANK0, BANK1, when 4-M DRAM is used. "L" indicates a "through" setting. "H" indicates a "latch" setting. Set to "L" when 1-M DRAM is used.

Select Terminal	Bank1	Bank0
$\overline{CAS1}$	L	L
$\overline{CAS2}$	L	H
$\overline{CAS3}$	H	L
$\overline{CAS4}$	H	H

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C Standard is GND=0V	−0.5 to +7	V
Input Voltage	V_I		−0.5 to V_{DD}+0.5	V
Output Voltage	V_O		−0.5 to V_{DD}+0.5	V
Input Current	I_I		−10 to +10	mA
Output Current	I_O		−20 to +20	mA
Storage Temperature	T_{STG}	—	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0V)

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{DD}	4.5 to +5.5	V
Operating Temperature	T_{OP}	−40 to +85	°C
Oscillation Frequency	f_{OSC}	8	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=−40 to +85°C, V_{DD}=5V±10%, GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
H Level Input Voltage	V_{IH}	—	3.5	—	V_{DD}+0.3	V
L Level Input Voltage	V_{IL}	—	−0.3	—	1.5	V
H Level Input Current	I_{IH}	$V_{IH}=V_{DD}$	—	0.01	10	µA
L Level Input Current	I_{IL}	V_{IL}=GND	−10	−0.01	—	µA
Tri-state Output Leak Current (Including open drain output)	I_{OZH}	$V_{OH}=V_{DD}$	—	0.01	10	µA
	I_{OZL}	V_{OL}=GND	−10	−0.01	—	
H Level Output Voltage	V_{OH}	I_{OH}=−5.0mA	2.4	4.20	V_{DD}	V
L Level Output Voltage	V_{OL}	I_{OL}=+5.0mA	GND	0.24	0.5	V
Operating Current Consumption	I_{DD}	Output Open $V_{IH}=V_{DD}$ f_{OSC}=8MHz V_{IL}=GND	—	—	3	mA

*1 Standard when V_{DD}=5.0V, Ta=25°C

APPLICATION CIRCUITS

Figure 2 indicates an example of the circuits used when the MSM6388 (M6588) is used with four 1-Mbit DRAMs.

Figure 3 indicates an example of the circuits used when MSM6388 (M6588) is used with four 4-Mbit DRAMs.

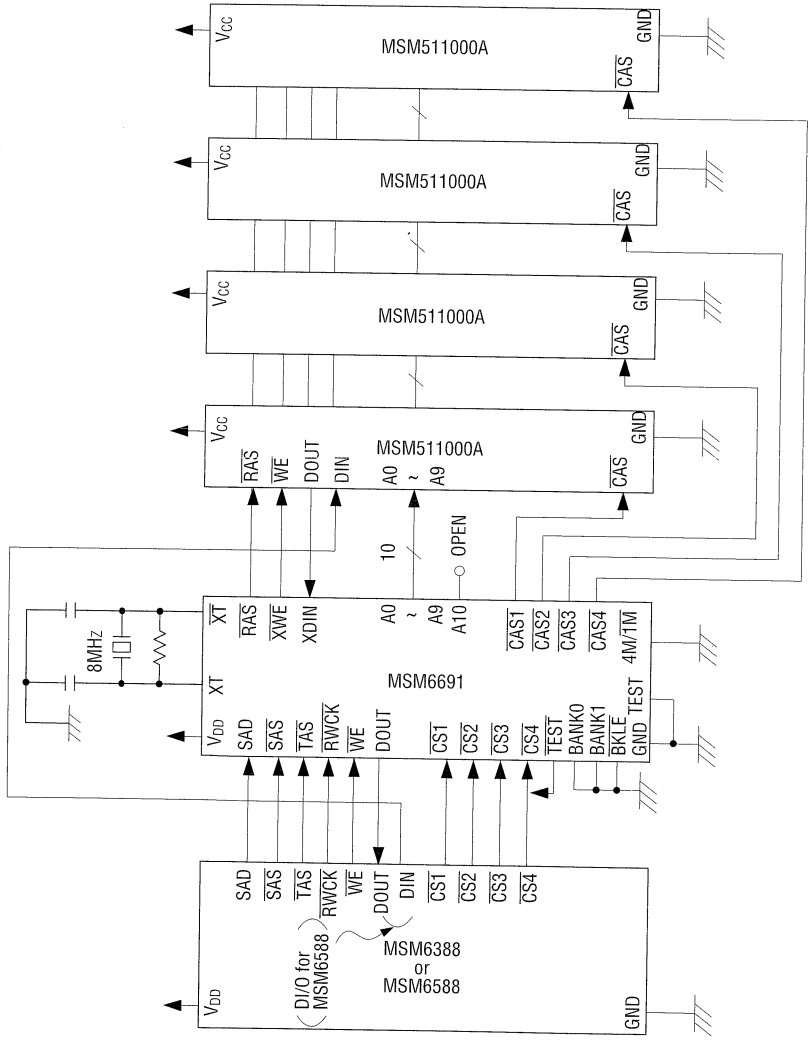


Figure 2. Example of Interfacing with Four 1-Mbit DRAMs

One of four DRAMs can be selected by BANK0 and BANK1.

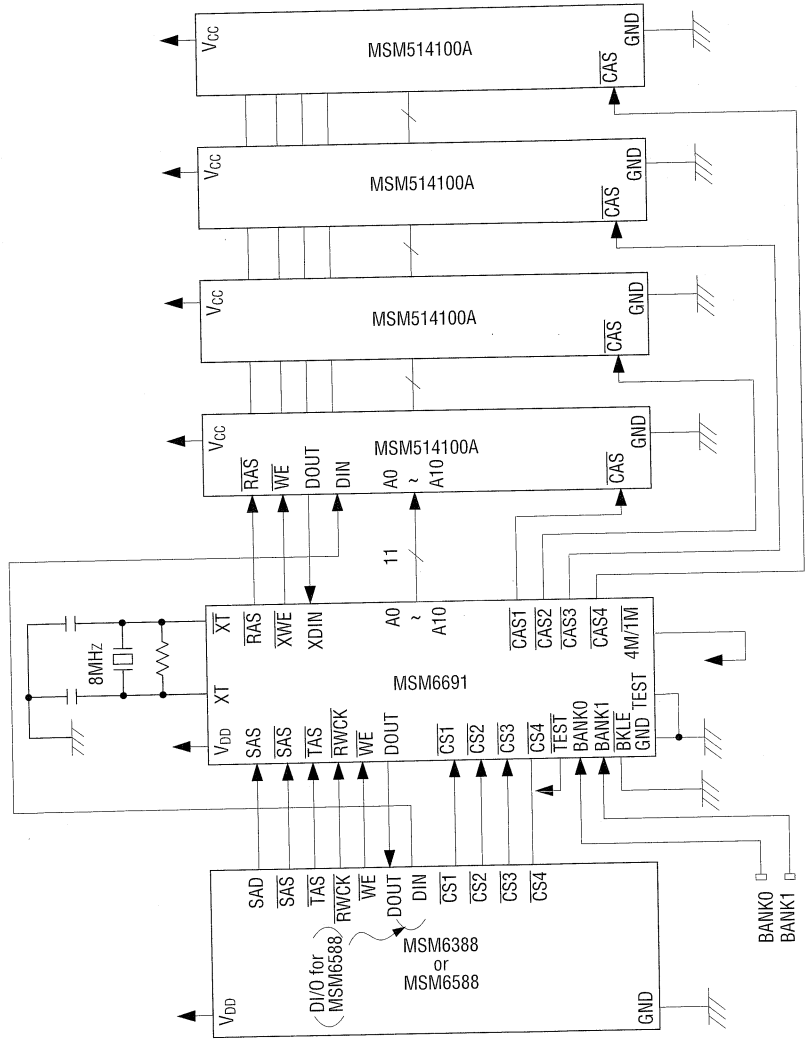


Figure 3. Example of Interfacing with Four 4-Mbit DRAMs

OKI Semiconductor

MSM6791

DRAM Interface iC

GENERAL DESCRIPTION

The MSM6791 can be used as a memory for voice data by connecting OKI solid-state recording and playback ICs (MSM6688 and MSM6788).

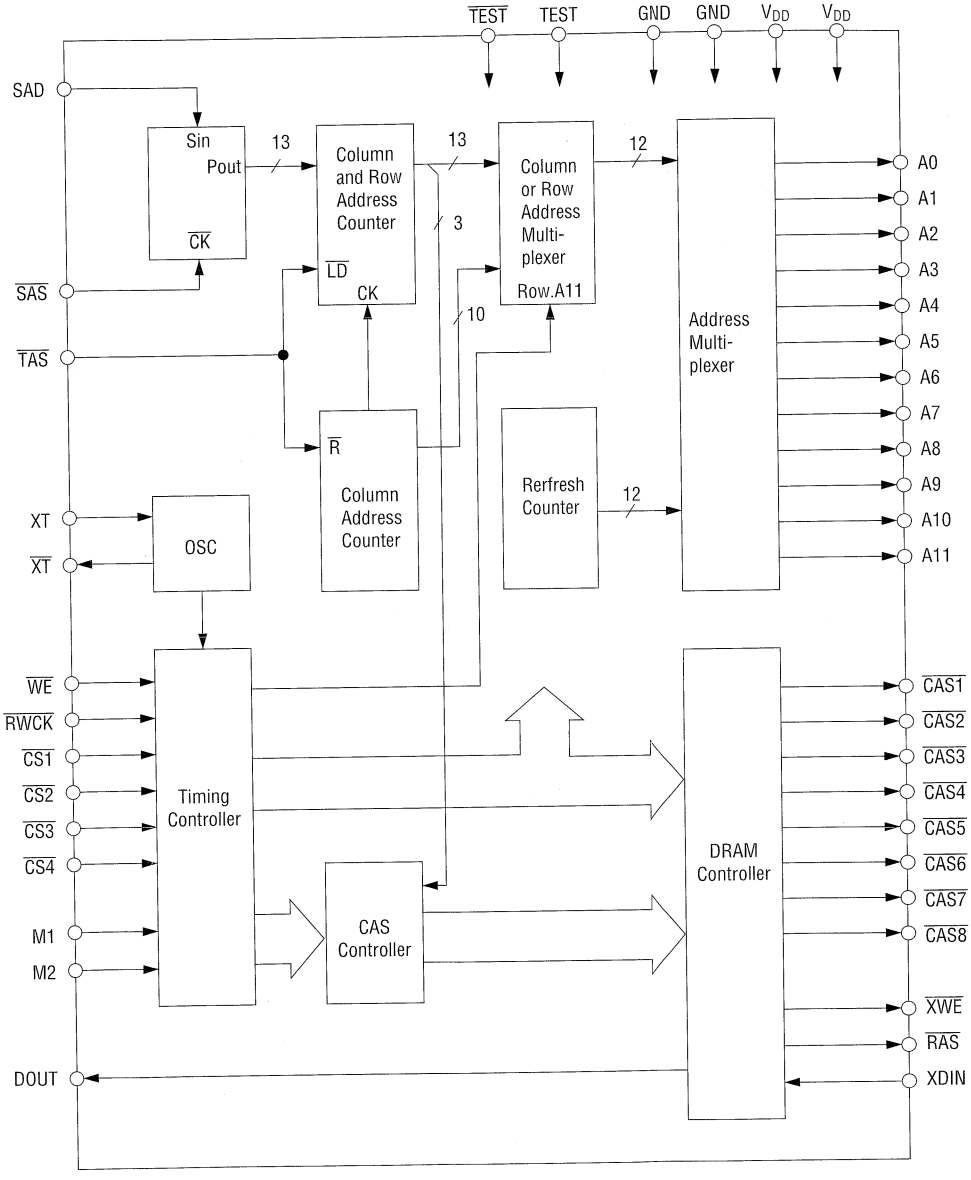
FEATURES

- DRAM (× 1-bit configuration)
  1M-bit DRAM (MSM511000A, MSM511001A) : 8 pcs. can be connected.
  4M-bit DRAM (MSM514100A, MSM514101A) : 8 pcs. can be connected.
  16M-bit DRAM (MSM5116100A) : 2 pcs. can be connected.

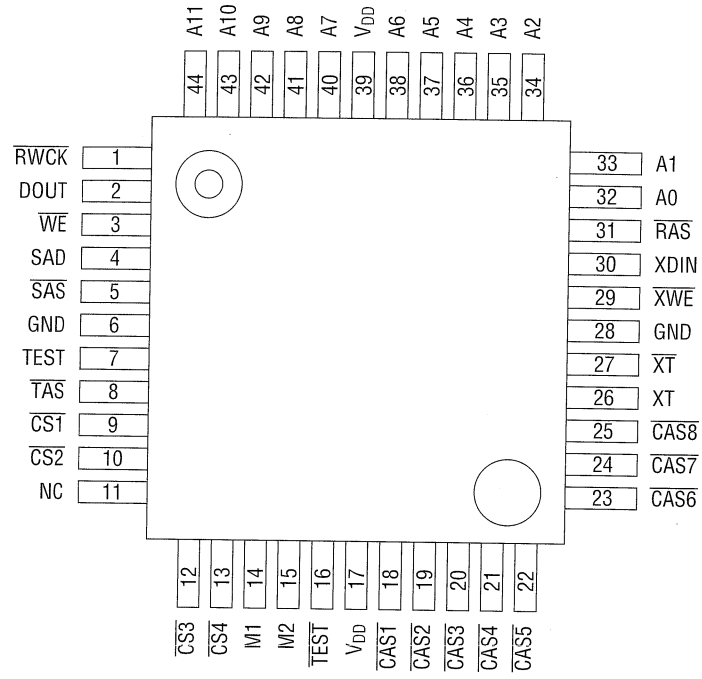
Note: MSM511002A/MSM514102A that corresponds to a static column mode cannot be used.

- Power supply voltage : 5V single rail
- Built-in refresh circuit (RAS only refresh)
- Original oscillation frequency: 8MHz
- Bit rates: 10kbps, 12.5kbps, 16kbps in MSM6788 connection (8kHz sampling fixation)
  7.5kbps, 9.4kbps, 12kbps in MSM6788 connection (6kHz sampling fixation)
  16kbps~32kbps in MSM6688 connection (4kHz~8kHz sampling)
- Package:
  44-pin plastic QFP (QFP44-P-910-2K) (Product name : MSM6791GS-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTION

Symbol	Type	Description
V_{DD}	–	Power supply
GND	–	Ground
XT	I	Oscillator
$\overline{XT}$	O	Oscillator
TEST	I	IC test. Use this pin by setting to 'L' level.
$\overline{TEST}$	I	IC test. Use this pin by setting to 'H' level.
SAD	I	Read/write head address
$\overline{SAS}$	I	Clock to take the serial address data in the internal register
$\overline{TAS}$	I	Serial address data taken in the address register to the internal address counter
$\overline{RWCK}$	I	Clock to read and write the information of the data register. The internal operation starts by the fall edge of $\overline{RWCK}$. In a read mode, the data taken in XDIN is latched and it is output to the DOUT pin. In a write mode, the DI/O output data of MSM6688/6788/6789 is taken in the DIN pin of the DRAM. In addition, the internal address counter automatically increments by the fall edge of $\overline{RWCK}$ and the address data output from A0 to A11.
$\overline{WE}$	I	Select a read mode and write mode.
$\overline{XWE}$	O	DRAM control
A0~A11	O	DRAM address
$\overline{RAS}$	O	DRAM control
$\overline{CAS1}$ ~ $\overline{CAS8}$	O	DRAM control
XDIN	I	Data input
DOUT	O	Data output
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	I	Chip select data in connecting DRAM By inputting a "L" level signal to each pin, up to 32M-bit of memory (8M-bit of memory for each pin) can be controlled for four Pins. These pins become the input pins to select the highest address in 16M-bit DRAM connection.
M1 M2	I	Set the connecting pattern of DRAM.

Connecting Mode	M2	M1	DRAM Connecting Pattern
Mode 0	L	L	1M-bit DRAM × 1~8pcs. connectable
Mode 1	L	H	4M-bit DRAM × 1~8pcs. connectable
Mode 2	H	L	(4M-bit DRAM × 1pcs.) + (1M-bit DRAM × 0~3pcs.) connectable
Mode 3	H	H	16M-bit DRAM × 1~2pcs. connectable

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C GND = 0V	−0.5 to +7	V
Input Voltage	V_I		−0.5 to V_{DD}+0.5	V
Output Voltage	V_O		−0.5 to V_{DD}+0.5	V
Input Current	I_I		−10 to +10	mA
Output Current	I_O		−20 to +20	mA
Storage Temperature	T_{STG}	—	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

GND = 0V

Parameter	Symbol	Range	Unit
Supply Voltage	V_{DD}	4.5 to 5.5	V
Operating Temperature	T_{OP}	−40 to +85	°C
Oscillation Frequency	f_{OSC}	8	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = −40 to +85°C, V_{DD} = 5V±10% GND = 0V)

Parameter	Symbol	Condition	Min.	Typ.*1	Max.	Unit
"H" Level Input Voltage	V_{IH}	—	3.5	—	V_{DD}+0.3	V
"L" Level Input Voltage	V_{IL}	—	−0.3	—	1.5	V
"H" Level Input Current	I_{IH}	V_{IH} = V_{DD}	—	0.01	10	µA
"L" Level Input Current	I_{IL}	V_{IL} = GND	−10	−0.01	—	µA
3-state Output Leak Current	I_{OZH}	V_{OH} = V_{DD}	—	0.01	10	µA
(includes open-drain output)	I_{OZL}	V_{OL} = GND	−10	−0.01	—	µA
H" Level Output Voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	4.20	V_{DD}	V
"L" Level Output Voltage	V_{OL}	I_{OL} = 5.0 mA	V_{SS}	0.24	0.5	V
Operational Current Consumption	I_{DD}	Output open f_{OSC} = 8MHz V_{IH} = V_{DD} V_{IL} = GND	—	—	3	mA

*1 TYP means V_{DD}=5.0V, Ta=25°C

APPLICATION CIRCUITS

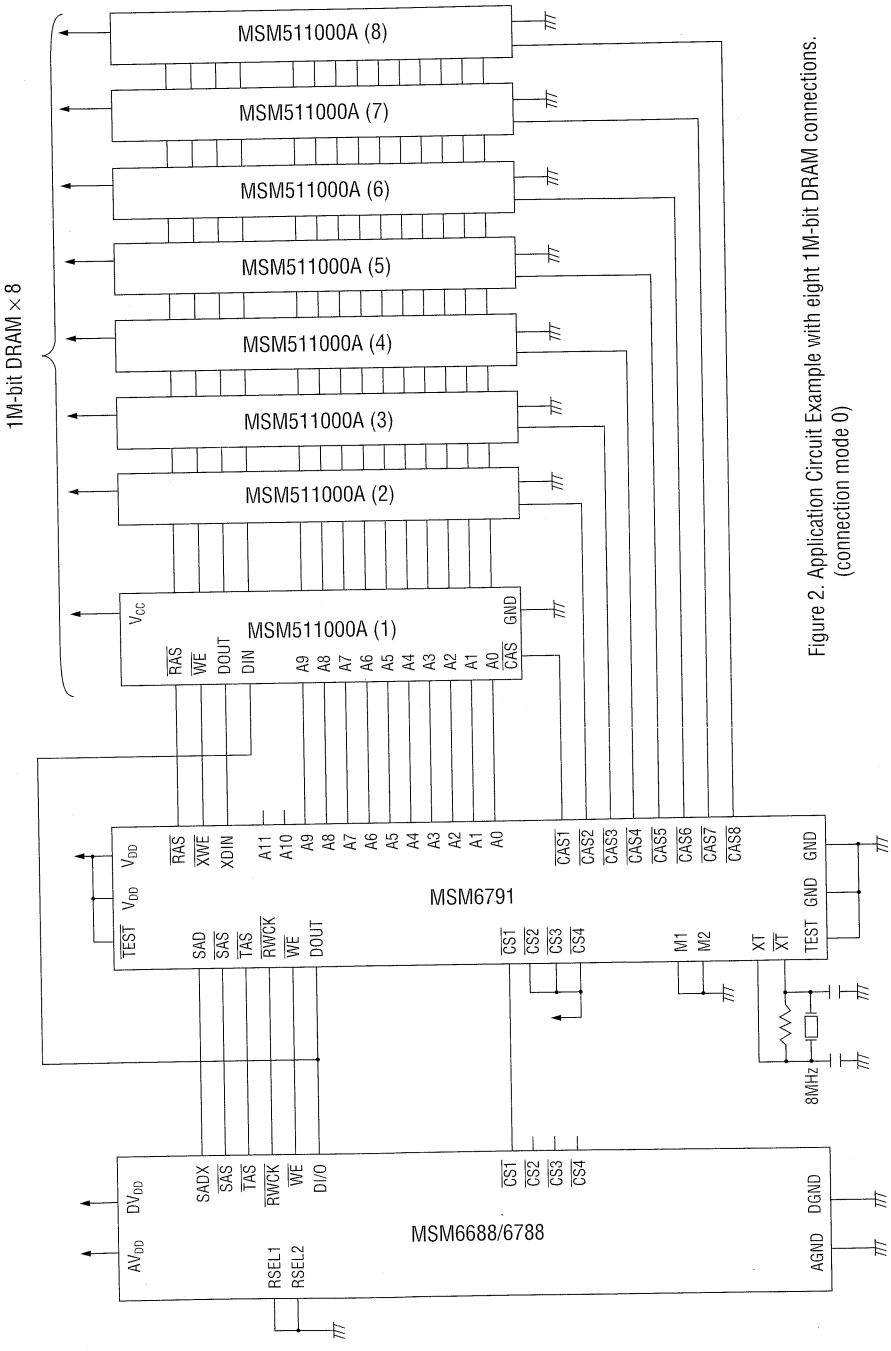


Figure 2. Application Circuit Example with eight 1M-bit DRAM connections. (connection mode 0)

APPLICATION CIRCUITS (Continued)

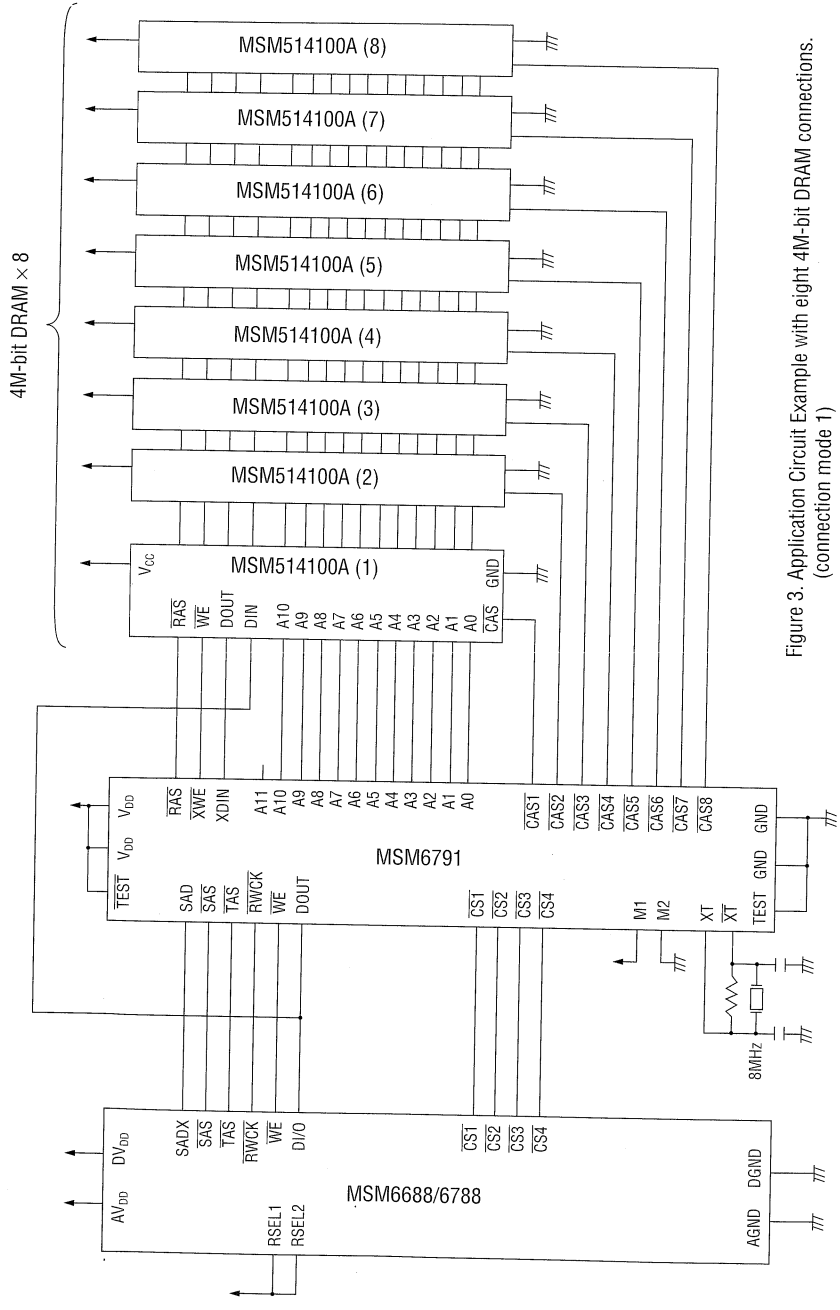


Figure 3. Application Circuit Example with eight 4M-bit DRAM connections. (connection mode 1)

APPLICATION CIRCUITS (Continued)

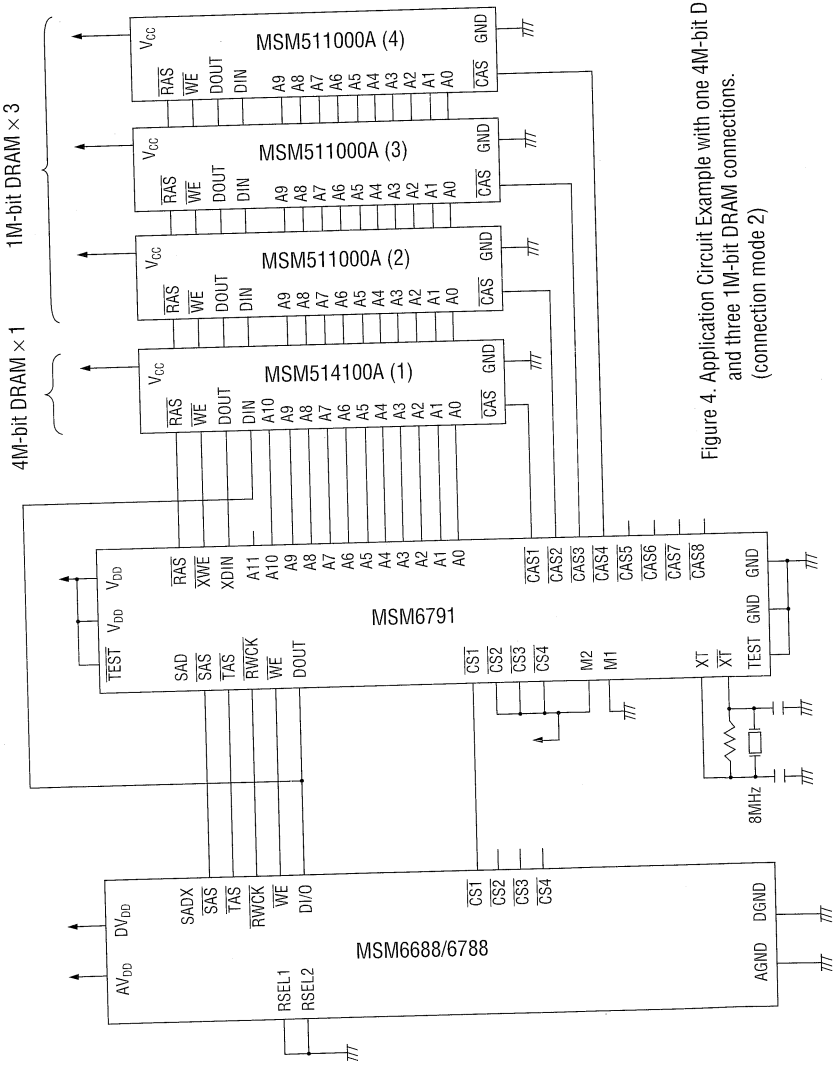


Figure 4. Application Circuit Example with one 4M-bit DRAM and three 1M-bit DRAM connections. (connection mode 2)

APPLICATION CIRCUITS (Continued)

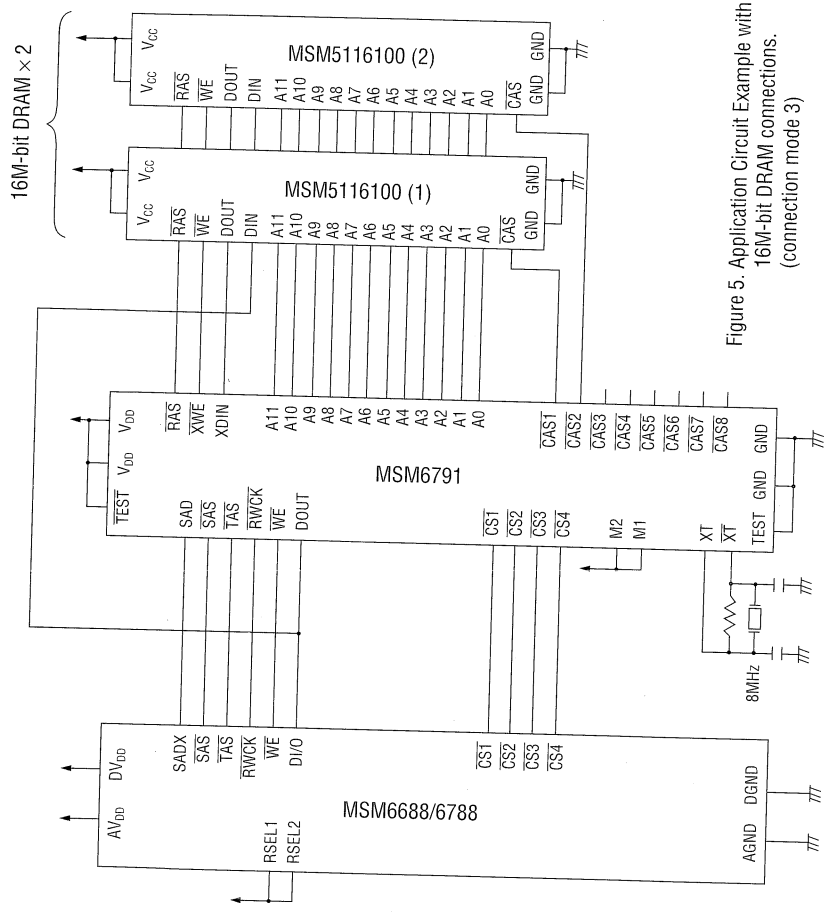


Figure 5. Application Circuit Example with two 16M-bit DRAM connections. (connection mode 3)

APPLICATION CIRCUITS (Continued)

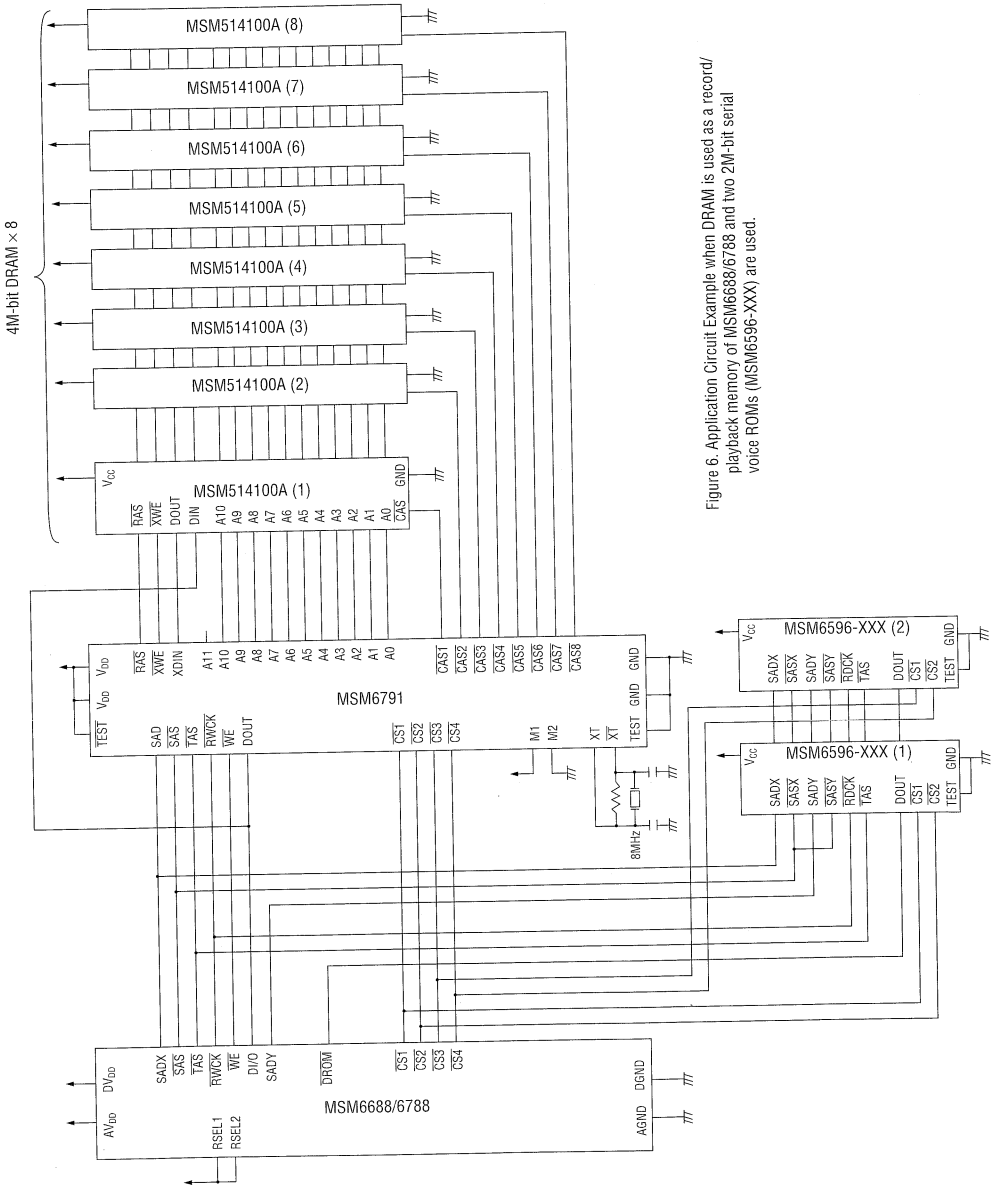


Figure 6. Application Circuit Example when DRAM is used as a record/ playback memory of MSM6688/6788 and two 2M-bit serial voice ROMs (MSM6596-XXX) are used.

OKI Semiconductor

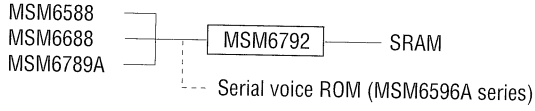
MSM6792

SRAM Interface IC

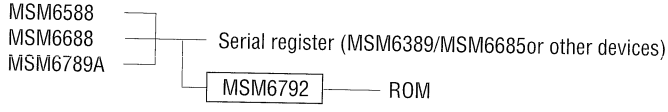
GENERAL DESCRIPTION

When connected to OKI's recording and playback IC, the MSM6792 allows the use of SRAM (Static-RAM), EPROM or mask ROM as a voice data storage memory.
This device has a built-in internal address generation circuit. External single clock input enables serial continuous read/write operation.
The internal address is incremented automatically by read/write operation.
A combination of the device with OKI's recording and playback IC allows the easy organization of a voice recording and playback system with fixed messages.

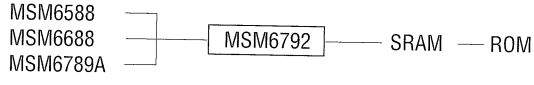
<Connection of SRAM>



<Connection of ROM>



<Connection of SRAM and ROM>

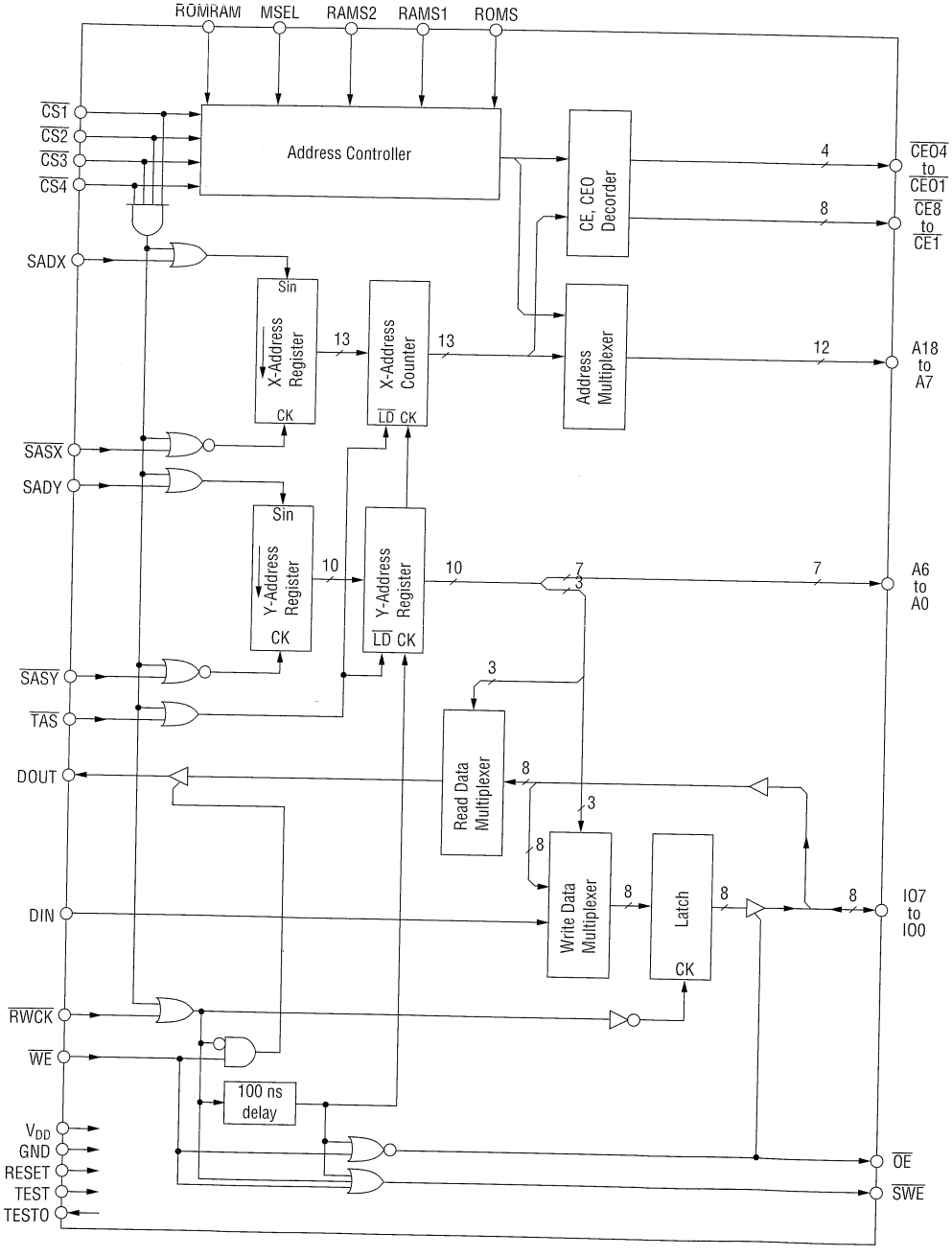


Recording and playback IC	Interface IC	SRAM capacity × number of devices	ROM capacity × number of devices
MSM6588	MSM6792	256 Kbit × 4	1 Mbit × 4 4 Mbit × 1
		1 Mbit × 4	
		4 Mbit × 1	
MSM6688 MSM6789A		1 Mbit × 8	
		1 Mbit × 4 + 4 Mbit × 1	
		4 Mbit × 8	

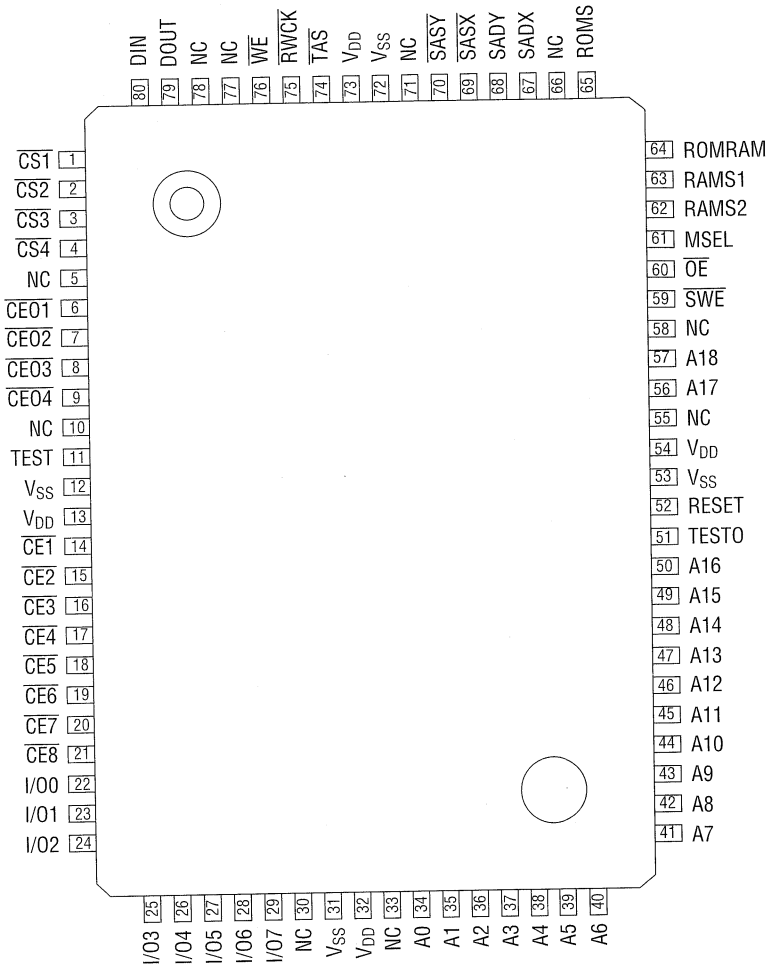
FEATURES

- Applicable SRAM (× 8 bit configuration)
  MSM51257 (32768 × 8 bit)
  MSM521008 (131072 × 8 bit)
- Applicable EPROM and mask ROM (× 8 bit configuration)
  MSM531000 (32768 × 8 bit)
  MSM531001 (131072 × 8 bit)
- Supply voltage : Single 5 V
- Package:
  80-pin plastic QFP (QFP80-P-1420-BK) (Product name: MSM6792GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

80-Pin Plastic QFP

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply. Insert a 0.1 µF or more bypass capacitor between this pin and GND pin.</td></tr>
<tr><td>GND</td><td>—</td><td>GND pin.</td></tr>
<tr><td>ROMRAM</td><td>I</td><td>Memory select pin.
"L" : SRAM
"H" : EPROM/mask ROM</td></tr>
<tr><td>MSEL</td><td>I</td><td>Pin to select recording/playback LSI.
"L" : MSM6588
"H" : MSM6688/MSM6789A</td></tr>
<tr><td>RAMS2
RAMS1</td><td>I</td><td>Pin to select configuration of external SRAM.
<table>
<tr><th>MSEL</th><th>RAMS2</th><th>RAMS1</th><th>SRAM configuration</th><th>Total capacity</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>256KSRAM×4</td><td>1Mbit</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1MSRAM×4</td><td>4Mbit</td></tr>
<tr><td>0</td><td>1</td><td>—</td><td>4MSRAM×1</td><td>4Mbit</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1MSRAM×8</td><td>8Mbit</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4MSRAM×1+1MSRAM×4</td><td>8Mbit</td></tr>
<tr><td>1</td><td>1</td><td>—</td><td>4MSRAM×8</td><td>32Mbit</td></tr>
</table></td></tr>
<tr><td>ROMS</td><td>I</td><td>Pin to select configuration of external EPROM/mask ROM.
<table>
<tr><th>ROMS</th><th>ROM configuration</th><th>Total capacity</th></tr>
<tr><td>0</td><td>1MROM×4</td><td>4Mbit</td></tr>
<tr><td>1</td><td>1MROM×1</td><td>4Mbit</td></tr>
</table></td></tr>
<tr><td>$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$
$\overline{CS4}$</td><td>I</td><td>Input pins for chip select. Connect these pins to $\overline{CS1}$ to $\overline{CS4}$ of recording/playback LSI. Inputting "L" level enables access to memory. The memory capacity per pin is as follows.
<table>
<tr><th>ROMRAM</th><th>MSEL</th><th>Memory capacity per pin</th></tr>
<tr><td>0</td><td>0</td><td>1 Mbit</td></tr>
<tr><td>0</td><td>1</td><td>8 Mbit</td></tr>
<tr><td>1</td><td>—</td><td>1 Mbit</td></tr>
</table></td></tr>
<tr><td>SADX</td><td>I</td><td>Pin to input first X address to read/write in serial. The number of bits of X address is as follows.
<table>
<tr><th>ROMRAM</th><th>MSEL</th><th>Number of bits of X address</th></tr>
<tr><td>0</td><td>0</td><td>10 bits</td></tr>
<tr><td>0</td><td>1</td><td>13 bits</td></tr>
<tr><td>1</td><td>—</td><td>10 bits</td></tr>
</table></td></tr>
<tr><td>SADY</td><td>I</td><td>Pin to input first Y address to be read/written in serial. The number of bits of Y address is 10 bits.</td></tr>
<tr><td>$\overline{SASX}$</td><td>I</td><td>Clock input pin to fetch a serial address data of X address and load in an internal register.</td></tr>
<tr><td>$\overline{SASY}$</td><td>I</td><td>Clock input pin to fetch a serial address data of Y address and load in an internal register.</td></tr>
</table>

Symbol	Type	Description
$\overline{TAS}$	I	Control input pin to set X and Y addresses loaded in the internal registers to the internal address counters.
$\overline{RWCK}$	I	Clock input pin to read/write data from/to external memory. Internal operation starts at the fall of $\overline{RWCK}$. In read mode, read data from external memory is output to the DOUT pin. In write mode, data of the DIN pin os written to external memory via IO0-7 pins. Internal address counter is automatically incremented by the rise of $\overline{RWCK}$, and output address data from A0-A18 pins.
$\overline{WE}$	I	Input pin to select read mode and write mode. "L" : Write mode "H" : Read mode
DIN	I	Pin to input write data in write mode.
DOUT	O	Pin to output read data in read mode.
$\overline{CE1}$ to $\overline{CE8}$	O	Chip enable pins for external SRAM.
$\overline{CEO1}$ to $\overline{CEO4}$	O	Chip enable pins for external EPROM/mask ROM.
A0 to A18	O	Address output pins for external memory.
IO0 to IO7	I/O	Data input/output pins to/from external memory.
$\overline{SWE}$	O	Read mode/write mode control pin for external memory.
$\overline{OE}$	O	Data output control pin for external memory.
RESET	I	Pin to test LSI. Set this pin to "L" level for testing.
TEST	I	Pin to test LSI. Set this pin to "L" level for testing.
TESTO	O	Pin to test LSI. Leave this pin open.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C with respect to GND=0 V	−0.5 to +6.5	V
Input Voltage	V_I		−0.5 to V_{DD}+0.5	V
Output Voltage	V_O		−0.5 to V_{DD}+0.5	mA
Input Current	I_I		−10 to +10	mA
Output Current	I_O		−13 to +13	mA
Storage Temperature	T_{STG}	—	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{DD}	+4.5 to +5.5	V
Operating Temperature	T_{op}	−40 to +85	°C

ELECTRICAL CHARACTERISTICS

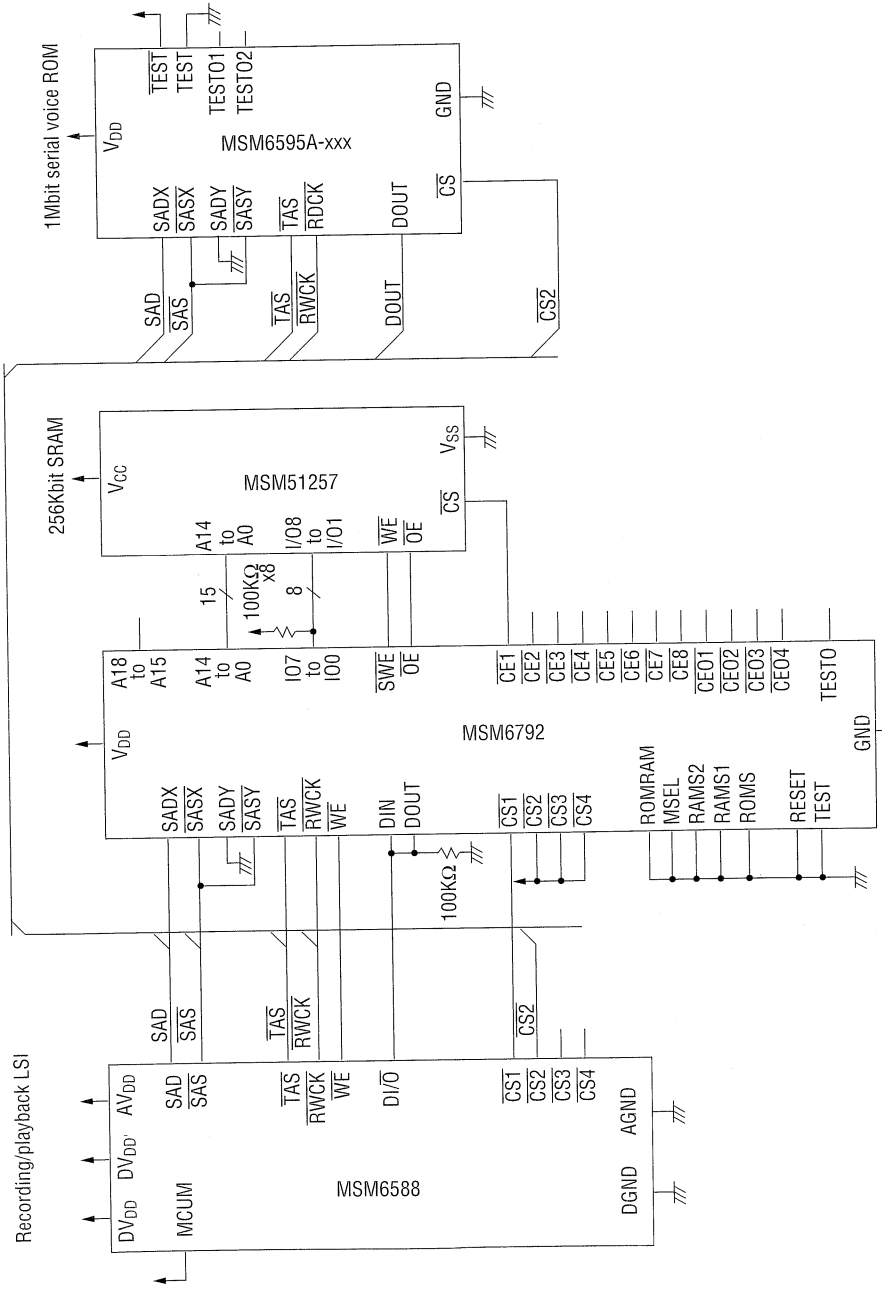
DC Characteristics

(Ta=−40 to +85°C, V_{DD}=5 V±10%, GND=0 V)

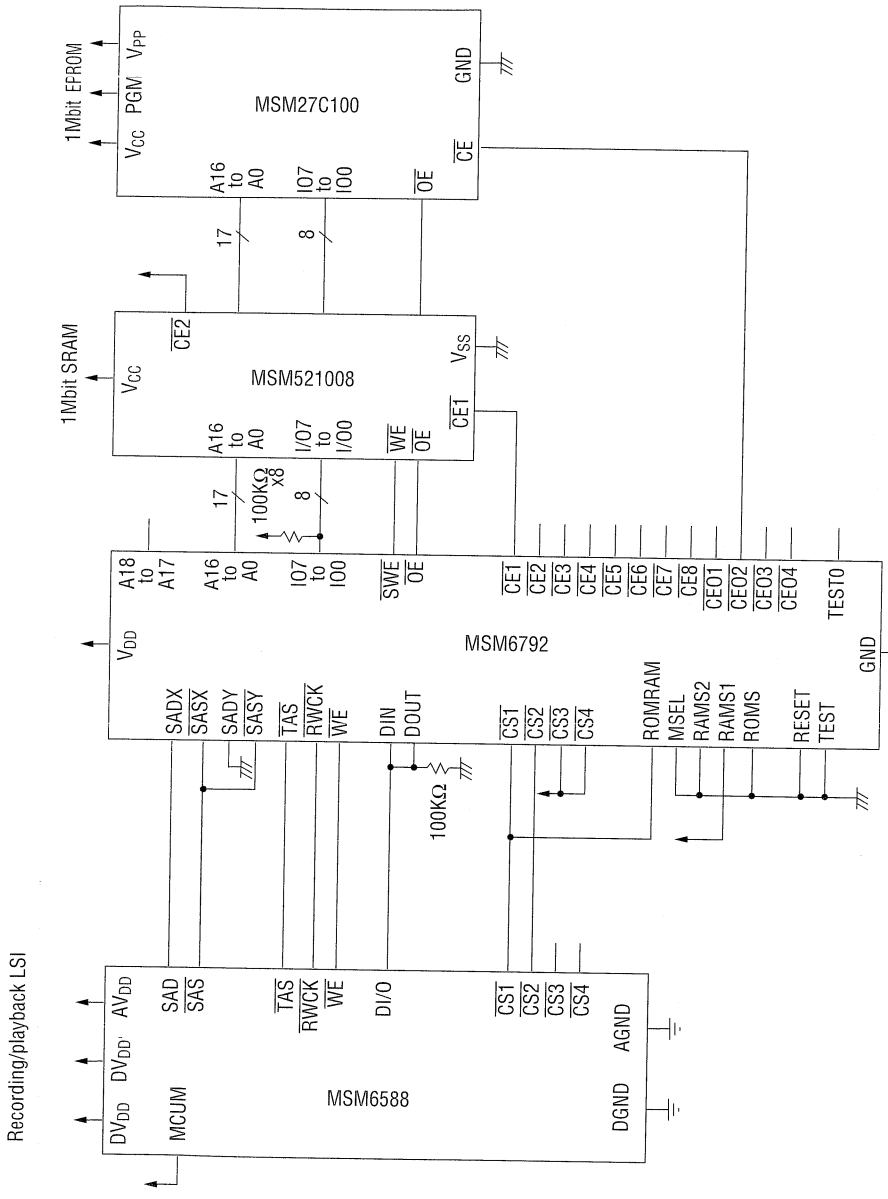
Parameter	Symbol	Condition		Min.	Typ.*1	Max.	Unit
High Level Input Voltage	V_{IH}	—		0.7×V_{DD}	—	V_{DD}+0.5	V
Low Level Input Voltage	V_{IL}	—		−0.5	—	0.3×V_{DD}	V
High Level Input Current	I_{IH}	V_{IH}=V_{DD}		—	0.01	10	µA
Low Level Input Current	I_{IL}	V_{IL}=GND		−10	−0.01	—	µA
Three State Output Leakage Current (including open drain output)	I_{OZH}	V_{OH}=V_{DD}		—	0.01	10	µA
	I_{OZL}	V_{OL}=GND		−10	−0.01	—	µA
High Level Output Voltage	V_{OH}	I_{OH}=−4.0 mA		3.7	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL}=4.0 mA		—	—	0.4	V
Operating Current	I_{DD}	Output open, f_{OSC}=8 MHz V_{IH}=V_{DD} V_{IL}=GND		—	—	5	mA
Standby Current	I_{DDS}	Output open V_{IH}=V_{DD} V_{IL}=GND	Ta=−40 to +70°C	—	—	10	µA
			Ta=+70 to +85°C	—	—	100	µA

*1 Typical value denotes V_{DD}=5.0V at Ta=25°C.

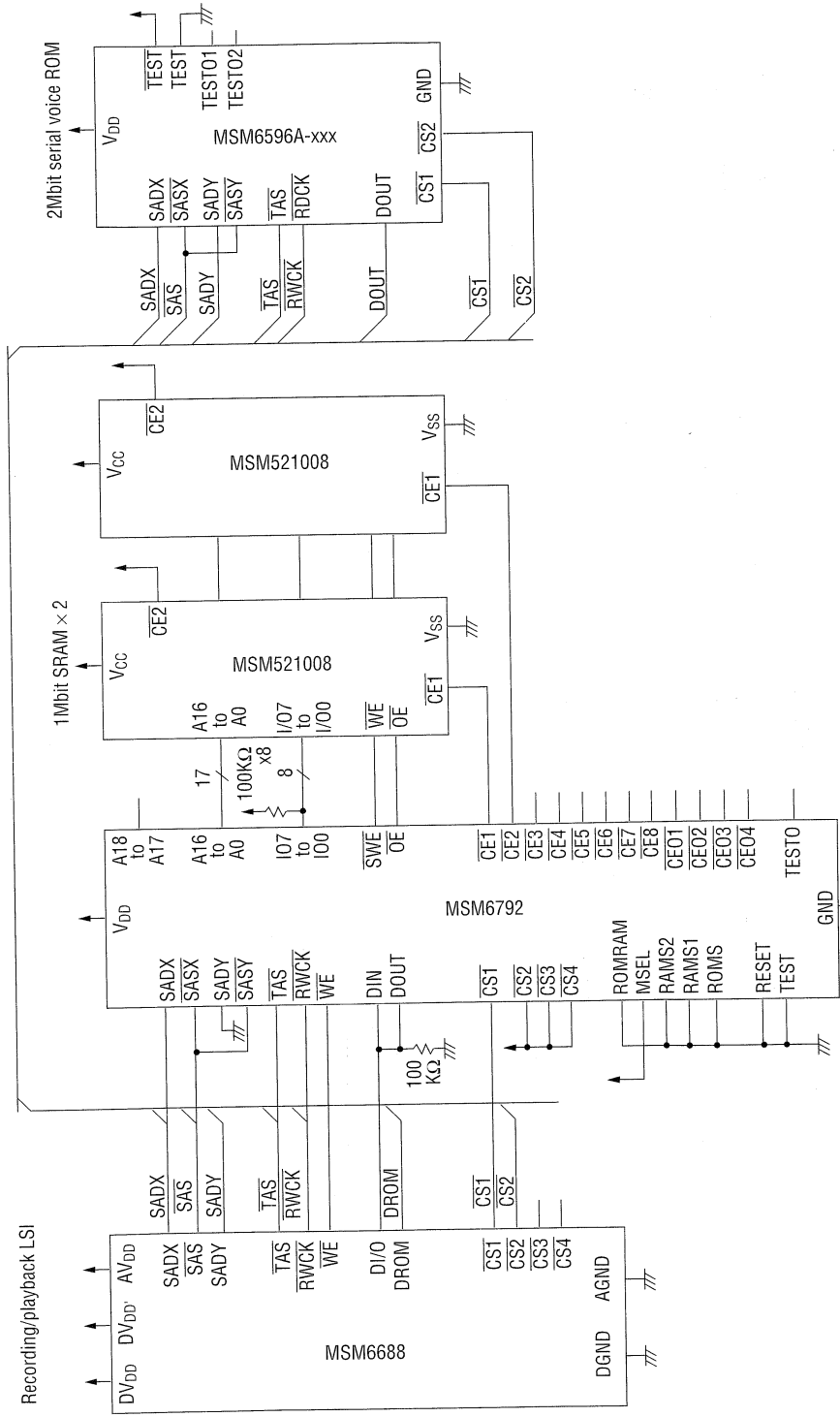
APPLICATION CIRCUITS



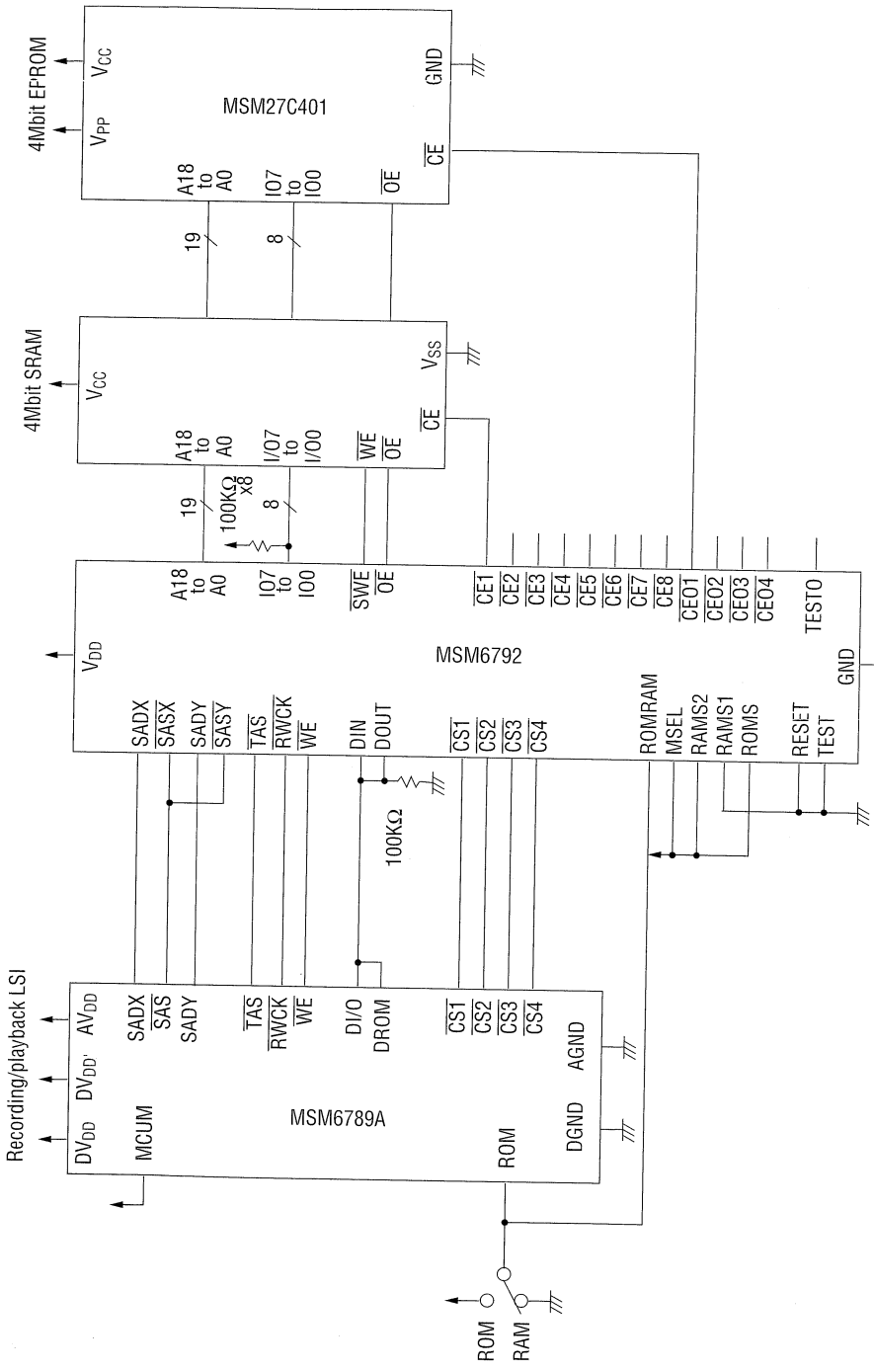
This is an applicaiton circuit example when MSM6588, one 256 Kbit SRAM and 1 Mbit serial voice ROM are connected.



This is an application circuit example when MSM6588, one 1Mbit SRAM, and 1Mbit EPROM are connected.



This is an application circuit example when MSM6688, two 1Mbit SRAM and one 2Mbit serial voice ROM are connected.



This is an application circuit example when MSM6789A, one 4Mbit SRAM, and one 4Mbit EPROM are connected.

DATA SHEET 5 VOICE PITCH CONTROLLERS

OKI Semiconductor

MSM6722

Pitch Control IC for The Speech Signal

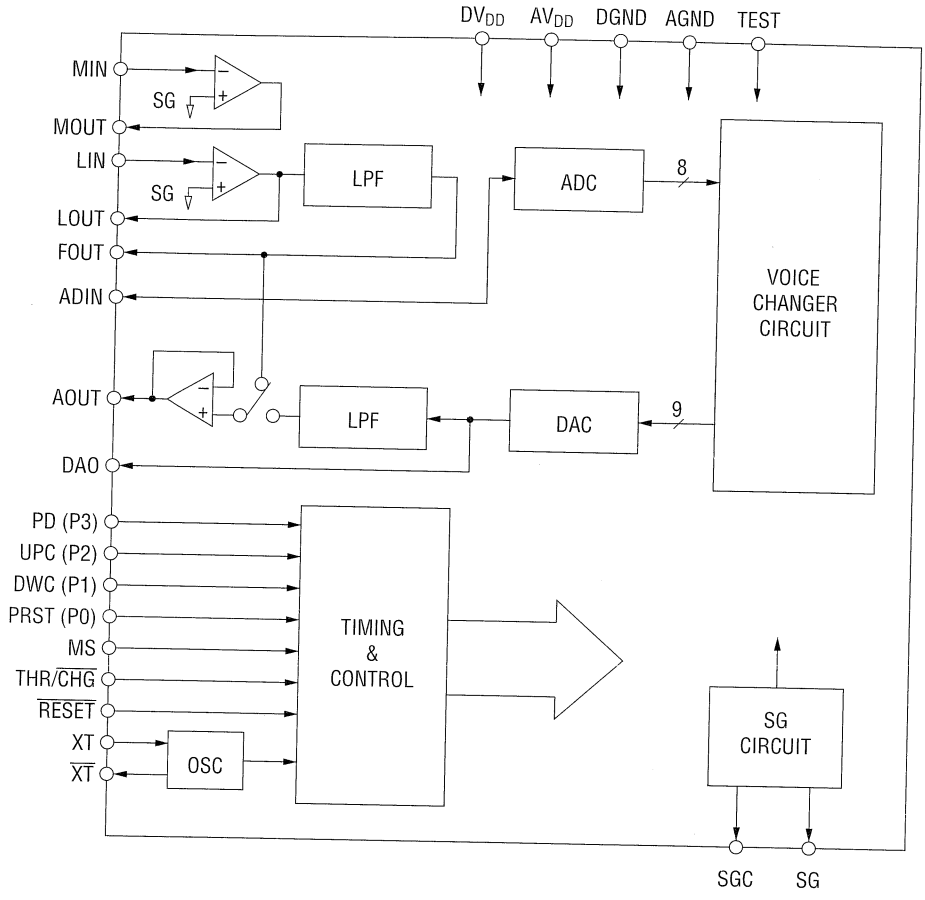
GENERAL DESCRIPTION

The MSM6722 converts in real-time the pitch of the speech signal in a range of one octave upward or downward.
Two pitch control methods can be selected. One is to change the pitch in 17 steps by two switch inputs, and the other is to select one of 16 steps by four binary input lines.
Since a microphone preamplifier and a low-pass filter are built in, the pitch conversion set can easily be configured by connecting a microphone, amplifier, and speaker in the peripheral circuit.

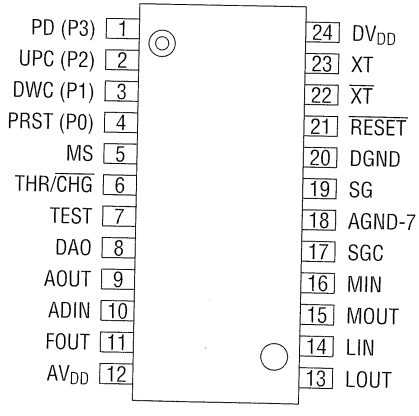
FEATURES

- Built-in microphone preamplifier
- Built-in low-pass filters
- Built-in 8-bit AD converter
- Built-in 9-bit DA converter
- Speech pitch alterable in 17 steps (including the no pitch change step)
- Master clock frequency at 4 MHz
- 5 V single power supply
- Package : 24-pin plastic SOP (SOP24-P-430-K) (Product name : MSM6722GS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



24-Pin Plastic SOP

PIN DESCRIPTIONS

Common to UP/DOWN Mode and BINARY Mode

Pin	Symbol	Type	Description
24	DV_{DD}	—	Digital power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and DGND.
20	DGND	—	Digital ground pin.
12	AV_{DD}	—	Analog power supply pin. Insert a bypass capacitor of 0.1μF or more between this pin and AGND.
18	AGND	—	Analog ground pin.
16	MIN	I	Inverting input pins for the built-in OP amplifier. The non-inverting input pin is connected internally to SG.
14	LIN		
15	MOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN respectively.
13	LOUT		
10	ADIN	I	Input pin for the built-in 8-bit AD converter.
11	FOUT	O	Output pin from the built-in LPF. Connect to ADIN Pin.
9	AOUT	O	Output pin from built-in LPF. This pin is used to output speech signals and to connect the amplifier for driving speaker.
8	DAO	O	Output pin from built-in 9-bit DA converter.
21	$\overline{RESET}$	I	The IC enters the initial state when this pin is at the "L" level. At this time, the oscillation stops and the DA converter output (DAO) and audio output (AOUT) fall to the GND level. Then the IC returns to the initial state. The IC has a built-in power-on-reset circuit. For normal power-on reset operation, supply the power within 1 msec. If power cannot be supplied within 1 msec, apply a $\overline{RESET}$ pulse after the power is switched on.
6	THR/$\overline{CHG}$	I	Select pin for the pitch control or non-pitch control. With a "H" level input, the IC outputs a normal speech signal from the AOUT pin through the built-in OP amplifier. With a "L" level input, the IC outputs a pitch controlled speech signal from the AOUT pin.
7	TEST	I	Test pin to be fixed to "L" level.
23	XT	I	Crystal oscillator connecting pin. When using the external clock, use this pin as the input.
22	$\overline{XT}$	O	Crystal oscillator connecting pin. When using the external clock, this pin must be left OPEN.
19	SG	O	These pins output the reference voltage (signal ground (SG)) of the analog circuit. The output is approximately 1/2 the AV_{DD} level.
17	SGC		

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UP/DOWN Mode Only

Pin	Symbol	Type	Description
5	MS	I	Mode select pin. This pin must always be tied low.
2	UPC	I	Pins for raising or lowering the pitch by one step at a time. The pitch changes by one step upward (or downward) each time a "H" level pulse is input to the UPC (or DWC) pin. The circuit enters the "no pitch change" state when an "H" level pulse is input to these pins simultaneously.
3	DWC		
1	PD	I	Power-down pin. All clocks, including the internal oscillator circuit, are stopped when the PD pin is set to the "H" level.
4	PRST	I	Pitch reset pin. The circuit enters the "no pitch change" state when this pin is set to the "H" level.

Binary Mode Only

Pin	Symbol	Type	Description
5	MS	I	Mode select pin. This pin must always be tied high.
1	P3	I	The pitch step is directly set by 4 pins (bits) of P3 (MSB) to P0 (LSB). One of the 16 steps from step 0 (P3=P2=P1=P0="L") to step 15(P3=P2=P1=P0="H") can be set.
2	P2		
3	P1		
4	P0		

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power-supply voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power-supply voltage	V_{DD}	DGND = AGND = 0 V	+4.5 to +5.5	V
Operating temperature	T_{op}	—	−10 to +70	°C
Master clock frequency	f_{OSC}	—	4 to 4.5	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = −10 to 70°C, DV_{DD} = AV_{DD} = 4.5 V to 5.5 V, DGND = AGND = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
"H" input voltage	V_{IH}	—	0.8 x V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.2 x V_{DD}	V
"H" input current *1	I_{IH1}	V_{IH} = V_{DD}	—	—	10	µA
"H" input current *2	I_{IH2}	V_{IH} = V_{DD}	—	—	20	µA
"L" input current *4	I_{IH3}	V_{IH} = V_{DD}	20	—	650	µA
"L" input current *3	I_{IL1}	V_{IL} = GND	−10	—	—	µA
"L" input current *2	I_{IL2}	V_{IL} = GND	−20	—	—	µA
Operating current consumption (1)	I_{DD}	f_{OSC} = 4 MHz, no load	—	6	12	mA
Operating current consumption (2)	I_{PD}	At power down, no load	—	—	10	µA

*1 Applies to all input pins excluding the XT pin.
*2 Applies to the XT pin.
*3 Applies to all the input pins without pull-down resistors, excluding the XT pin (i.e., pins 1, 5-7, 10, 14, 16, 21; however pin 1 is applied only during UP/DOWN mode).
*4 Applies to the input pins with pull-down resistors, excluding the XT pin (i.e., pins 1, 2, 3, 4; however, pin 1 is applied only during BINARY mode).

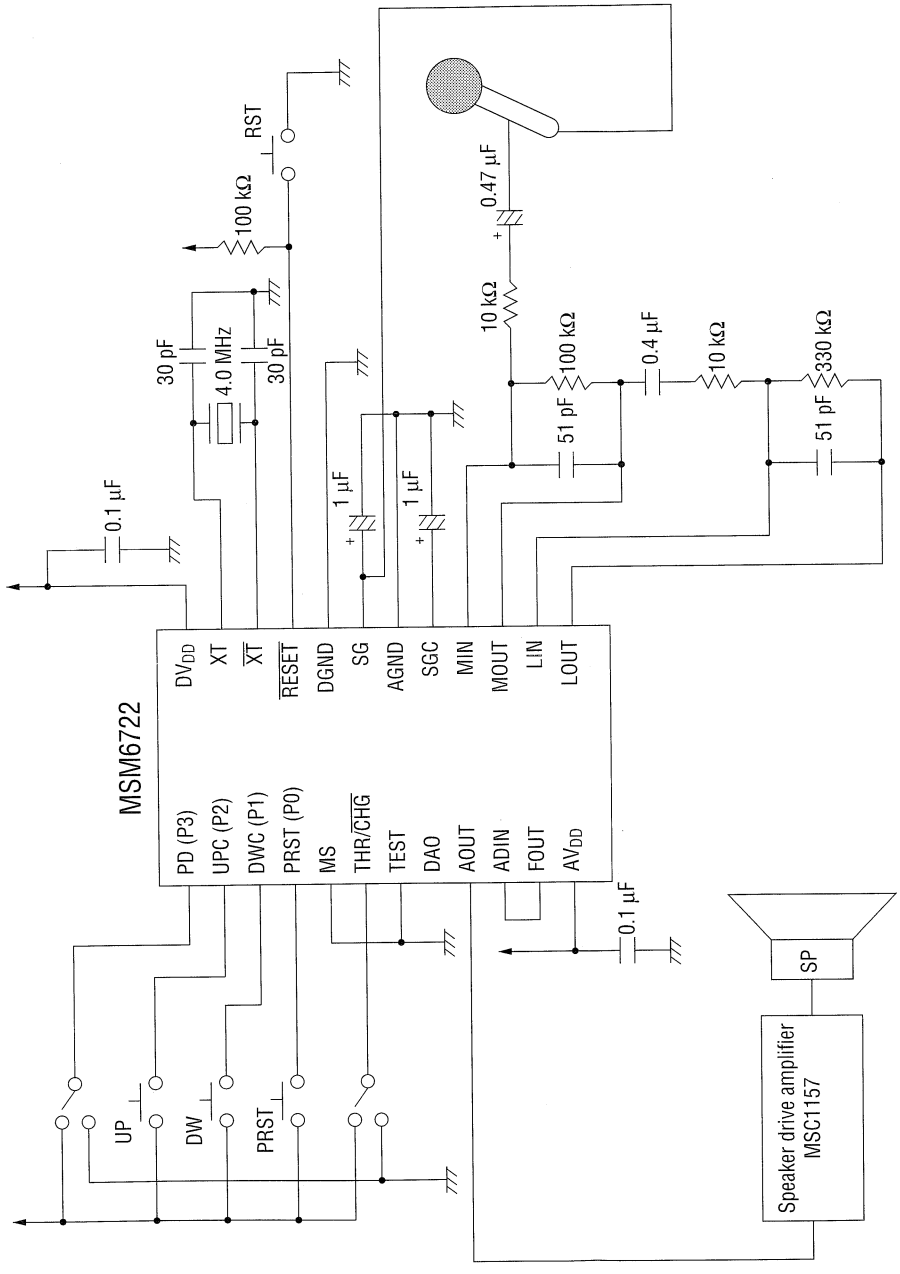
Analog Characteristics

(Ta = −10 to +70°C, DV_{DD} = AV_{DD} = 4.5 V to 5.5 V, DGND = AGND = 0 V)

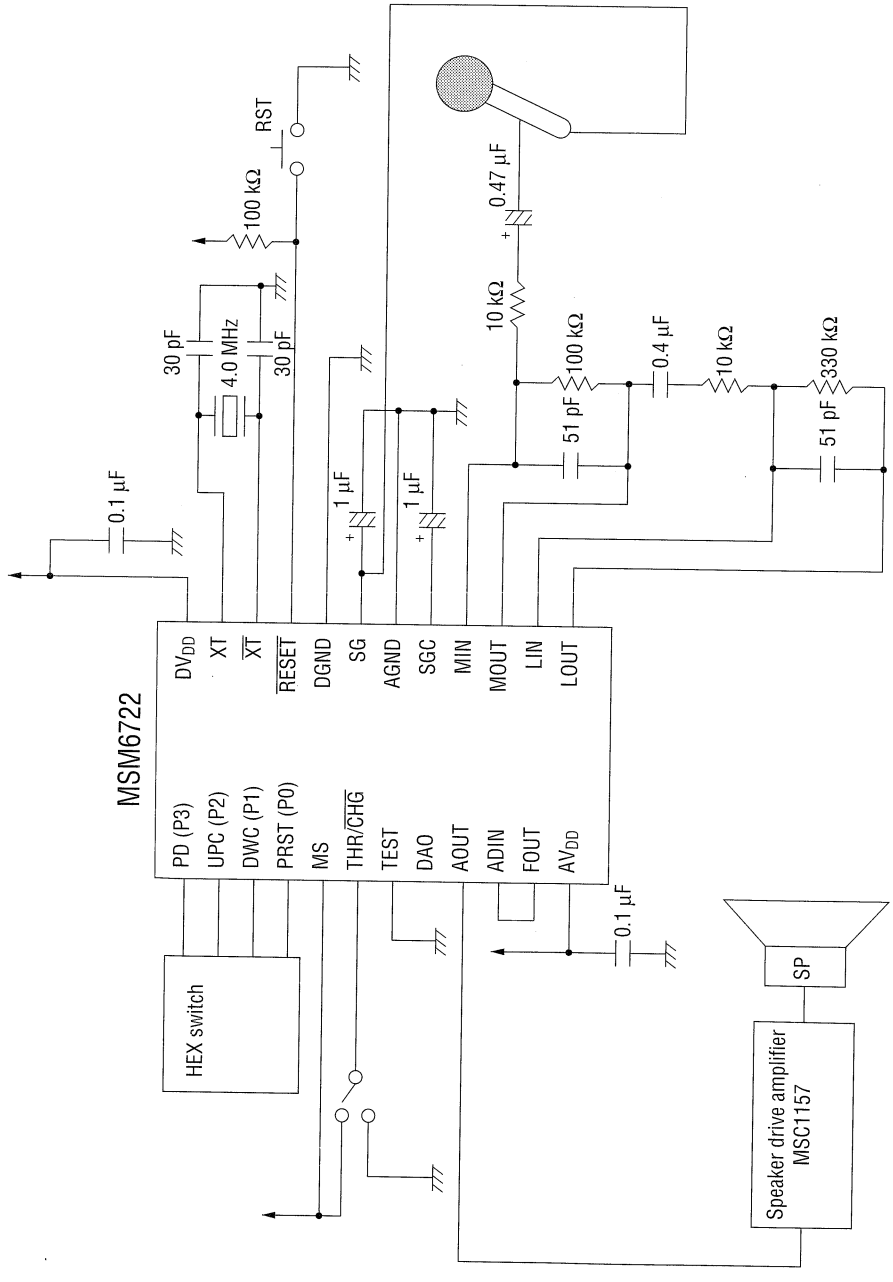
Parameter	Symbol	Condition	Min	Typ	Max	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
AD output relative error	$\lvert V_{ADE} \rvert$	No load	—	—	40	mV
SCF allowable input voltage range	V_{FIN}	—	1	—	V_{DD}−1	V
SCF input impedance	R_{FIN}	—	1	—	—	MΩ
OP amplifier open loop gain	G_{OP}	f_{IN} = 0 to 4 kHz	40	—	—	dB
OP amplifier input impedance	R_{INA}	—	1	—	—	MΩ
OP amplifier load resistance	R_{OUTA}	—	200	—	—	kΩ

APPLICATION CIRCUITS

UP/DOWN Mode



BINARY Mode


MSM6722
DVDD
XT
XT
RESET
DGND
SG
AGND
SGC
MIN
MOUT
LIN
LOUT
PD (P3)
UPC (P2)
DWC (P1)
PRST (P0)
MS
THR/CHG
TEST
DAO
AOUT
ADIN
FOUT
AVDD
0.1 µF
30 pF
4.0 MHz
30 pF
100 kΩ
RST
1 µF
1 µF
0.47 µF
10 kΩ
100 kΩ
51 pF
0.4 µF
10 kΩ
330 kΩ
51 pF
0.1 µF
HEX switch
SP
Speaker drive amplifier
MSC1157

DATA SHEET 6 SPEAKER AMPLIFIERS

OKI Semiconductor

MSC1157

Speaker Drive Amplifier

GENERAL DESCRIPTION

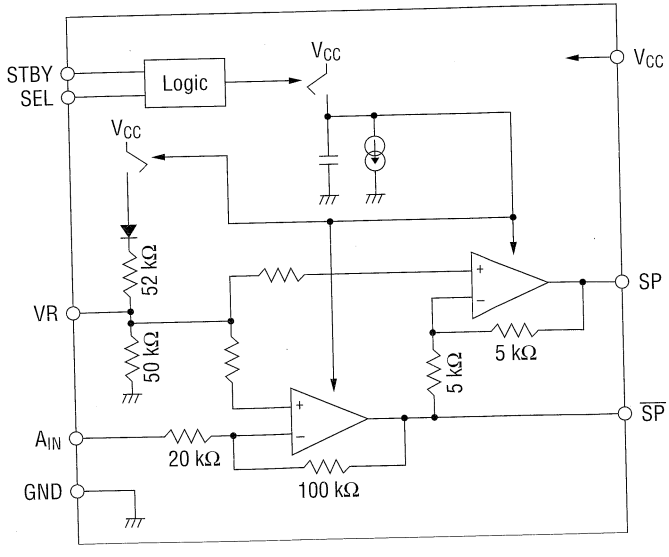
The MSC1157, designed specifically to operate at a low voltage with low current consumption, is a power amplifier developed for driving a speaker for a voice IC.
The voltage gains can be adjusted over a range of up to ten. The differential output can directly drive a speaker without any output coupling capacitors. The MSC 1157, because of its ability to stand by, is ideally suitable for portable equipment applications powered by a battery.

FEATURES

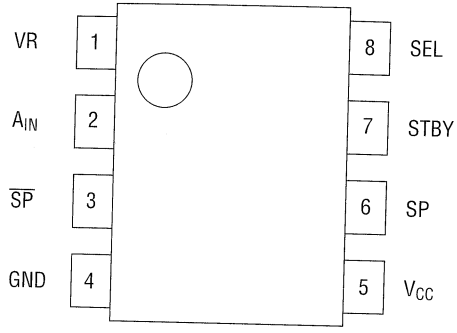
- Low voltage operation : 2.0 to 6.0 V (Single power supply)
- Low current dissipation
  Operating current : 1.6mA without load (typ.)
  : Current dissipation less than 1 µA in standby
- Standby function : 350mA peak
- High output current : A speaker can be directly connected between differential outputs.
- Differential outputs : Gain can be adjusted by use of an external resistor.
- Adjustable gain
- Package options:
  8-pin plastic DIP (DIP8-P-300) (Product name : MSC1157RS)
  8-pin plastic SOP (SOP8-P-250-K) (Product name : MSC1157MS-K)
  Chip

7

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



8-Pin Plastic DIP
or
8-Pin Plastic SOP

PIN DESCRIPTIONS

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>5</td><td>V_{CC}</td><td>—</td><td>Power supply pin.</td></tr>
<tr><td>4</td><td>GND</td><td>—</td><td>Ground pin.</td></tr>
<tr><td>2</td><td>A_{IN}</td><td>I</td><td>Signal input pin for analog signal inputs, etc.</td></tr>
<tr><td>7, 8</td><td>STBY, SEL</td><td>I</td><td>Digital input pins. Setting these pins configures the standby status. See the table below for how to set the pins.
<table><tr><th>SEL</th><th>STBY</th><th>Status</th></tr><tr><td rowspan="3">0</td><td>0</td><td>Operation</td></tr><tr><td>1</td><td>Standby</td></tr><tr><td>Clock</td><td>Operation</td></tr><tr><td rowspan="3">1</td><td>0</td><td>Standby</td></tr><tr><td>1</td><td>Operation</td></tr><tr><td>Clock</td><td>Operation</td></tr><tr><td rowspan="3">Clock</td><td>0</td><td>Operation</td></tr><tr><td>1</td><td>Operation</td></tr><tr><td>Clock</td><td>Unstable Operation</td></tr></table>
Applying a clock between 32kHz and 4MHz to either the STBY or the SEL pin leads the IC to operation status regardless of the status set at the other pin. Applying clocks to both of the pins at the same time may cause malfunction.</td></tr>
<tr><td>1</td><td>VR</td><td>O</td><td>Bias output pin for internal circuits. This pin is at GND potential during standby. Connecting a capacitor between VR and the GND pin reduces the pop-up noise at power on and improves the ripple elimination ratio.</td></tr>
<tr><td>3</td><td>$\overline{SP}$</td><td>O</td><td>Speaker output pin. This pin outputs a negative phase with respect to the input signal.</td></tr>
<tr><td>6</td><td>SP</td><td>O</td><td>Speaker output pin. This pin outputs a positive phase with respect to the input signal.</td></tr>
</table>

7

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Remark
Power Supply Voltage	V_{CC}	Ta=25°C	−0.3 to +6.5	V	V_{CC}
Input Voltage	V_{IN}	Ta=25°C	−0.3 to V_{CC}+0.3	V	STBY A_{IN}, SEL
Maximum Output Current	I_{OMAX}	Ta=25°C	(Note) ±400	mA	SP, $\overline{SP}$
Power Dissipation	P_D	Ta=25°C	470	mW	DIP type
			400	mW	SOP type
Junction Temperature	T_{jMAX}	—	125	°C	Chip
Storage Temperature	T_{STG}	—	−55 to +150	°C	

Note: Avoid shorting the output pins (SP and $\overline{SP}$) to V_{CC} or GND because the IC may be damaged.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	—	2.0	6.0	V
Load Impedance	RL	—	8.0	—	Ω
Peak Load Current	I_{O-P}	—	—	±350	mA
"H" Input Voltage	V_{IH}	For STBY and SEL pins	0.7 V_{CC}	—	V
"L" Input Voltage	V_{IL}		—	0.3 V_{CC}	V
STBY Operating Frequency	f_{STBY}	At clock input	32 k	4 M	Hz
Operating Temperature	Top	—	−20	+70	°C

7

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, Ta=25°C, V_{CC}=2 to 6 V

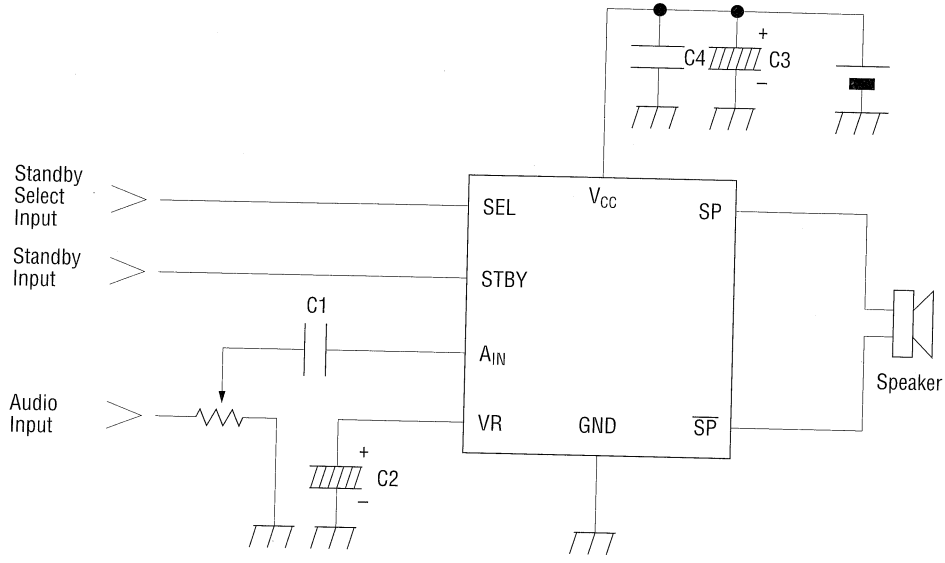
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
A_{IN} Input Resistance	R_{IN}	—	14	20	26	kΩ
Voltage Gain	A_{V1}	A_{IN}→$\overline{SP}$	13.44	14	14.49	dB
	A_{V2}	$\overline{SP}$→SP	−1.94	0	1.58	
	A_{V3}	A_{IN}→(Between $\overline{SP}$-SP)	19.46	20	20.51	
Output Power	P_{OUT1}	V_{CC}=3 V, f=1 kHz RL=8 Ω, THD≥10%	100	178	—	mW
	P_{OUT2}	V_{CC}=6 V, f=1 kHz RL=32 Ω, THD≥10%	300	440	—	mW
Total Harmonic Distortion	THD1	V_{CC}=3 V, RL=8 Ω f=1 kHz, P_{OUT}=45 mW	—	1.2	—	%
	THD2	V_{CC}=6 V, RL=32 Ω f=1 kHz, P_{OUT}=125 mW	—	0.37	—	%
Ripple Elimination Ratio	RR	f=1 kHz, C2=4.7 µF	30	43	—	dB
Output DC Voltage (Note)	V_O	In no signal state, V_{CC}=2 V	0.53	0.65	0.77	V
		In no signal state, V_{CC}=6 V	2.49	2.61	2.73	
Output Offset Voltage	ΔV_O	Between SP-$\overline{SP}$	—	—	±30	mV
Output "H" Voltage	V_{OH}	A_{IN}=V_{CC} or GND I_{OUT}=−100 mA	V_{CC}−1.15	V_{CC}−1.04	—	V
Output "L" Voltage	V_{OL}	A_{IN}=V_{CC} or GND I_{OUT}=100 mA	—	0.17	0.3	V
STBY, SEL Input Current	I_{IH}	V_I=V_{CC}	—	—	±0.1	µA
	I_{IL}	V_I=GND	—	—	±0.1	µA
VR Equivalent Resistance	R_{VR}	—	18	25	32	kΩ
Circuit Current During Operation	I_{CC}	V_{CC}=6 V, RL=∞	1.1	1.6	2.4	mA
Circuit Current During Standby	I_{CCS}	—	—	—	1.0	µA

Note: The typical value of the output voltage in no signal state is determined from the following equation.

$$V_O = (V_{CC} - 0.67) \frac{50\ k\Omega}{50\ k\Omega + 52\ k\Omega}$$

7

APPLICATION CIRCUIT



- If parasitic capacitance of 60pF or more exists between GND and the speaker output pin $\overline{SP}$ or $\overline{SP}$, oscillation may occur. Implement the circuit mount design so as to be less than 60pF.

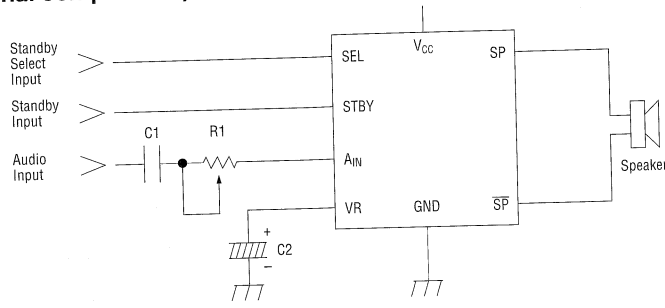
- C1 is the AC coupling capacitor. Cutoff frequency fc on the low frequency side is determined by the following equation. Choose a value of C1 according to the bandwidth.

$$fc = \frac{1}{2 \times \pi \times C1 \times 20k} \text{ (Hz)}$$

- Choose a value of C2 that is 80 to 100 times as large as that of C1.
- When the standby function is not used, connect the pins STBY and SEL to V_{CC} or GND.
- It is recommended that the capacitor C4 (approximately 0.1μF) having better high frequency characteristics and the capacitor C3 (approximately 10μF) be placed between the pins V_{CC} and GND.

GAIN ADJUSTMENT

1. Gain Adjustment Using Input Resistance (This approach allows gain adjustment with fewer external components)



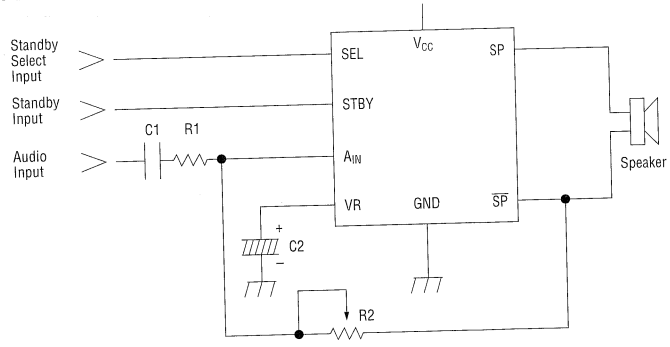
- Cutoff frequency fc on the low frequency side is determined from the equation:

$$fc \fallingdotseq \frac{1}{2 \times \pi \times C1 \times (R1 + 20k)} \text{ (Hz)}$$

- Voltage gain A_{V1} is determined from the equation:

$$A_{V1} \fallingdotseq \frac{100k}{R1 + 20k} \text{ (V/V)}$$

2. Gain Adjustment Using Feedback Resistance (This approach has the advantage over the above approach (less noise approach), but the number of components is increased)



- Cutoff frequency fc on the low frequency side is determined from the equation:

$$fc \fallingdotseq \frac{1}{2 \times \pi \times C1 \times Zin} \text{ (Hz)} \qquad Zin \fallingdotseq R1 + \frac{R2 \times 20k}{R2 + 120k} \text{ (}\Omega\text{)}$$

- Voltage gain A_{V1} is determined from the equation:

$$A_{V1} \fallingdotseq \frac{5}{1 + \dfrac{R1}{20k} + \dfrac{6 \times R1}{R2}} \text{ (V/V)}$$

OKI Semiconductor

MSA180

Piezo Speaker Amplifier

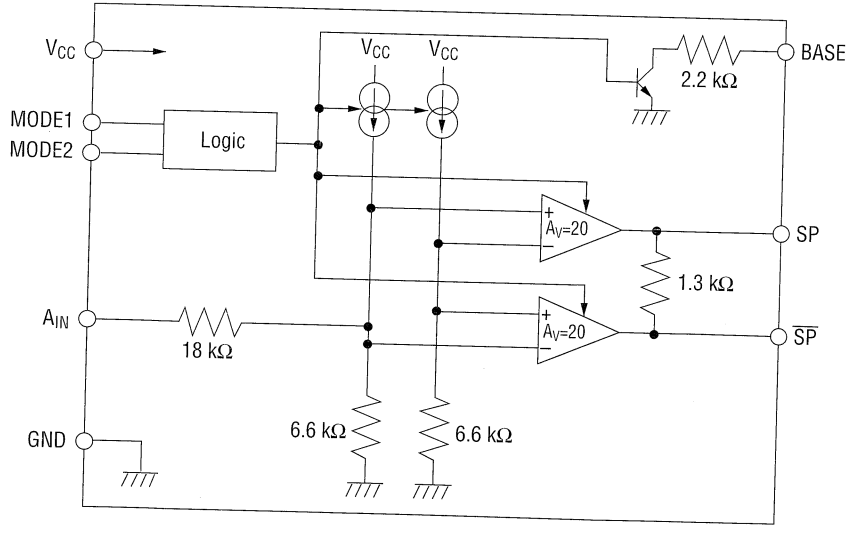
GENERAL DESCRIPTION

The MSA180 is a piezo speaker driver for OKI's speech synthesizers. Its voltage gain can be adjusted by a factor of up to 10. The differential output provides an amplitude of twice the voltage supply. A separate output connects to the base of an external transistor for controlling system voltage. A standby function eliminates power loss when no input signal is present.

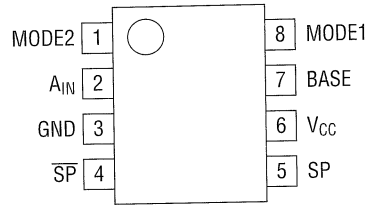
FEATURES

- Power supply voltage : +2.0 V to +6.0 V
- Low current consumption : 4.2 mA typ (V_{CC}=3 V)
- Standby current : <1 µA
- Differential output : Amplitude twice the supply voltage
- Package options :
  - 8-pin plastic DIP (DIP8-P-300) (Product name: MSA180RS)
  - 8-pin plastic SOP (SOP8-P-250-K) (Product name: MSA180MS-K)
  - Chip (Product name: MSA180)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



8-Pin Plastic DIP or 8-Pin Plastic SOP

PIN DESCRIPTIONS

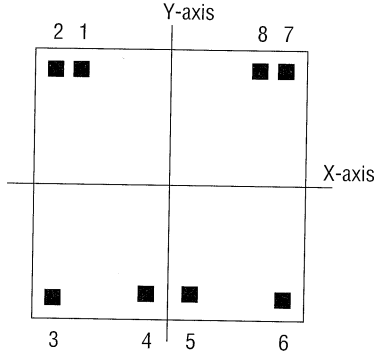
Pin	Symbol	Type	Description
6	V_{CC}	—	Power supply pin.
3	GND	—	Ground pin.
2	A_{IN}	I	Voice signal input pin.
8	MODE1	I	This pin switches the device between operation and standby modes. The IC is in operation mode if $V_{IH} > 1.0$ V on the MODE1 pin and is in standby mode if $V_{IL} < 0.3$ V on the MODE1 pin. When MODE1 is used, MODE2 must be connected to V_{CC}.
1	MODE2	I	This pin switches the device between operation and standby modes. The IC is in operation mode if $V_{IL} < V_{CC}-1.0$ V on MODE1 pin and is in standby mode if $V_{IH} > V_{CC}-0.3$ V on MODE1 pin. When MODE2 is used MODE1 must be connected to GND.
7	BASE	O	This pin is connected to the base of an external transistor. If an external transistor is not used to control system voltage, this pin must be left open.
4	$\overline{SP}$	O	This is a speaker output pin that provides signals with the same phase as the input.
5	SP	O	This is a speaker output pin that provides signals with an inverted phase to the input.

7

PAD CONFIGURATION

- Chip Layout

Chip size	:	2.00 mm × 2.00 mm
Chip thickness	:	350 µm ± 30 µm
Pad size	:	110 µm × 110 µm
Board potential	:	GND potential



Pad Coordinates (Chip center: X=0, Y=0)

Pad	Pad name	X-coordinate [µm]	Y-coordinate [µm]
1	MODE2	−655	835
2	A_{IN}	−835	835
3	GND	−835	−835
4	$\overline{SP}$	−185	−789
5	SP	121	−789
6	V_{CC}	815	−835
7	BASE	793	835
8	MODE1	613	835

ABSOLUTE MAXIMUM RATINGS

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Rating	Unit	Remarks
Power Supply Voltage	V_{CC}	—	−0.3 to +6.5	V	—
Input Voltage	V_{IN}	—	−0.3 to V_{CC}+0.3	V	A_{IN} MODE1 MODE2 BASE
Maximum Output Current	I_{oMAX}	V_{CC}=3 V	±80	mA	SP, $\overline{SP}$
Power Dissipation	P_D	Ta=25°C	400	mW	DIP type
			340	mW	SOP type
Junction Temperature	T_{jMAX}	—	110	°C	Chip
Storage Temperature	T_{STG}	—	−55 to +150	°C	—

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	—	2.0	6.0	V
Load Impedance	Z_L	—	200	—	Ω
Peak Load Current	I_{O-P}	—	—	±30	mA
"H" Input Voltage	V_{IH1}	Applied to MODE1 pin	1.0	—	V
	V_{IH2}	Applied to MODE2 pin	V_{CC}−0.3	—	V
"L" Input Voltage	V_{IL1}	Applied to MODE1 pin	—	0.3	V
	V_{IL2}	Applied to MODE2 pin	—	V_{CC}−1.0	V
Operating Temperature	T_{op}	—	−40	85	°C

ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{CC}=2 V to 6 V unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Voltage Gain	A_{V1}	A_{IN}→SP		4.25	5	5.75	V/V
	A_{V2}	A_{IN}→$\overline{SP}$		4.25	5	5.75	V/V
	A_{V3}	A_{IN}→(SP, $\overline{SP}$)		8.5	10	11.5	V/V
A_{IN} Input Resistance	R_{IN}	—		17.2	24.6	32.0	kΩ
Output DC Voltage *1	V_O	A_{IN}=OPEN	V_{CC}=2 V	0.7	1.0	1.3	V
		Z_L=∞	V_{CC}=6 V	2.5	3.5	4.6	V
Output DC Offset Voltage *2	ΔV_O	A_{IN}=OPEN	V_{CC}=2 V	—	—	0.2	V
		Z_L=∞	V_{CC}=6 V	—	—	0.6	V
SP, $\overline{SP}$ Output "H" Voltage	V_{OH}	I_{OUT}=−10 mA		V_{CC}−0.25	—	—	V
SP, $\overline{SP}$ Output "L" Voltage	V_{OL}	I_{OUT}=10 mA		—	—	0.25	V
Operating Current	I_{CC}	V_{CC}=3 V A_{IN}=Open Z_L=∞ BASE=Open MODE1=MODE2=GND or MODE1=MODE2=V_{CC}		—	4.2	6.2	mA
Circuit Current in Standby Mode	I_{CCS}	A_{IN}=Open MODE1=GND MODE2=V_{CC}		—	—	1	μA
A_{IN} Input DC Bias Voltage *3	V_{AIN}	V_{CC}=2 V		0.18	0.26	0.34	V
		V_{CC}=6 V		0.52	0.74	0.96	V
MODE1 "H" Input Current	I_{IH1}	MODE1=V_{CC}		—	—	160	μA
MODE2 "H" Input Current	I_{IH2}	MODE2=V_{CC}		—	—	1	μA
MODE1 "L" Input Current	I_{IL1}	MODE1=GND		−1	—	—	μA
MODE2 "L" Input Current	I_{IL2}	MODE2=GND		−160	—	—	μA
Base Output Current	I_{BO1}	V_{CC}=2 V BASE=V_{CC}		0.4	—	—	mA
	I_{BO2}	V_{CC}=6 V BASE=V_{CC}		1.6	—	—	mA

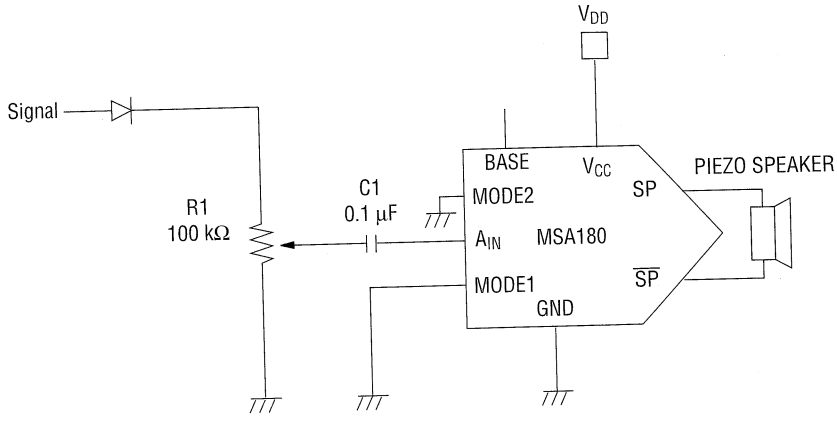
*1 Typical value is $V_O = V_{CC} \times 0.625 - 0.25$.
*2 Maximum value is $\Delta V_O = V_{CC} \times 0.1$.
*3 Typical value is $V_{AIN} = V_{CC} \times 0.12 + 0.02$.

7

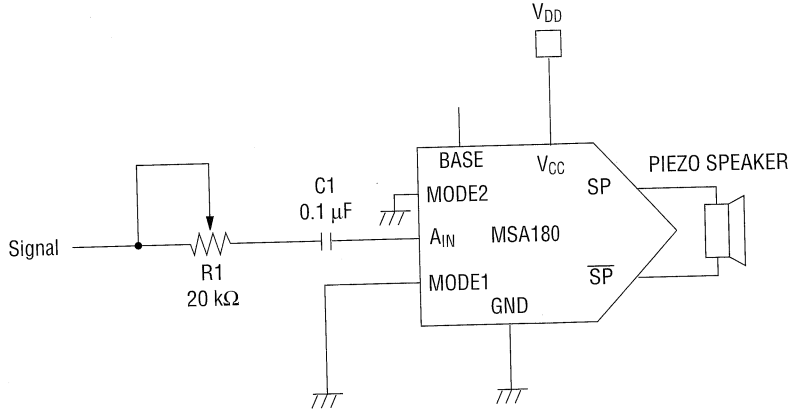
APPLICATION CIRCUITS

How to Adjust Gain

Gain control adjustment of the input signal level is shown below. When using OKI's speech synthesizer devices, insert a diode in series with the variable resistor to reduce pop noise.

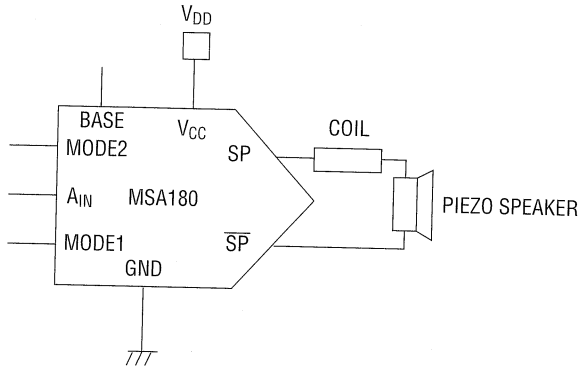


The circuit below also implements gain adjustment for a higher impedance signal source.



How to Connect the Piezo Speaker

To achieve the full gain level of 10 V, even at a low supply voltage (V_{CC}=3 V), connect a coil in series with the piezo speaker.



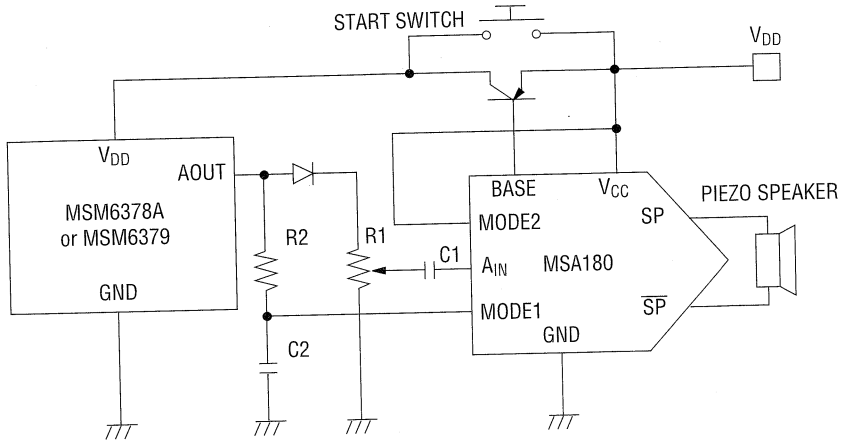
The resonance frequency that occurs in the circuit containing the coil and the piezo speaker is :

$$f_Q = \frac{1}{2\pi\sqrt{C_L \times L_L}} \text{ [Hz]}$$

Where C_L is the piezo capacitance and L_L the coil inductance.
For instance, if the piezo capacitance is 0.1 µF and f_Q is in a range of 2 to 3 kHz, then the coil inductance should be 30 mH.

Application Example for Circuits Containing the MSM6378A/MSM6379 Speech Synthesizers

This example shows how to connect the MSA180 with an MSM6378A or MSM6379 speech synthesizer using an external transistor and the MODE1 pin. The analog output of both synthesizers lowers to 0 V in their standby mode. For this reason, the voice signal can be used to control operation and standby modes of the MSA180. The circuit also controls the voltage via an external transistor. If this function is not used, leave the BASE pin open.

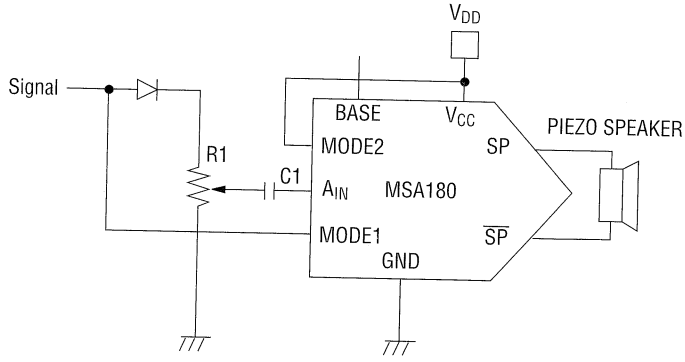


Operation Flow

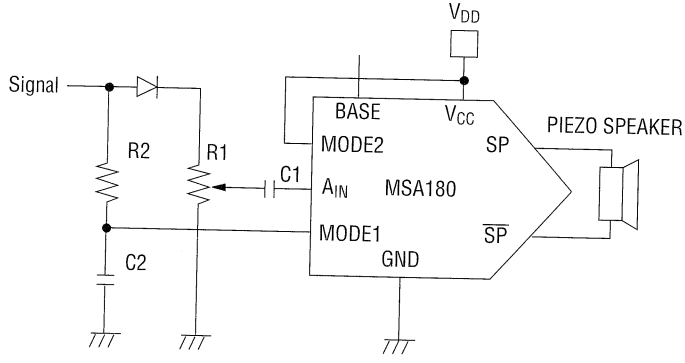
1. When the start switch is pressed, power is supplied to the V_{DD} pins on the MSM6378A or MSM6379, and operation mode is invoked. Voice output level then rises.
2. When operation mode is involved, the voice signal rises above the GND level, and MODE1 on MSA180 goes high (H).
3. The BASE pin on MSA180 goes low (L) to drive the external transistor for power-supply control.
4. The audio IC continues to operate using the external transistor as a power supply. The device continues to operate and voice sounds, even if the start switch is released at this time.
5. When the sound ends, MODE1 on MSA180 falls low (L), the voice signal falls to GND level, and standby mode ensues.
6. The external transistor for power-supply control is switched off, switching the voice synthesizer off because the power supply is switched off.

Supplemental Information When Using a Voice Signal on the MODE1 Pin

When using the voice signal on MODE1, as in the circuit below, care must be taken regarding the voice input level. Application of the voice signal below V_{IH1} level to the MODE1 pin causes the MSA180 to switch into standby mode, interrupting the voice reproduction flow, and causing undesired noises.



When using a voice signal lower than V_{IH}, refer to the circuit below. With a low-pass filter consisting of R2 and C2, voice levels lower than V_{IH1} are passed through. However, select values for R2 and C2 such that the input voltage on MODE1 is greater than V_{IH2}.



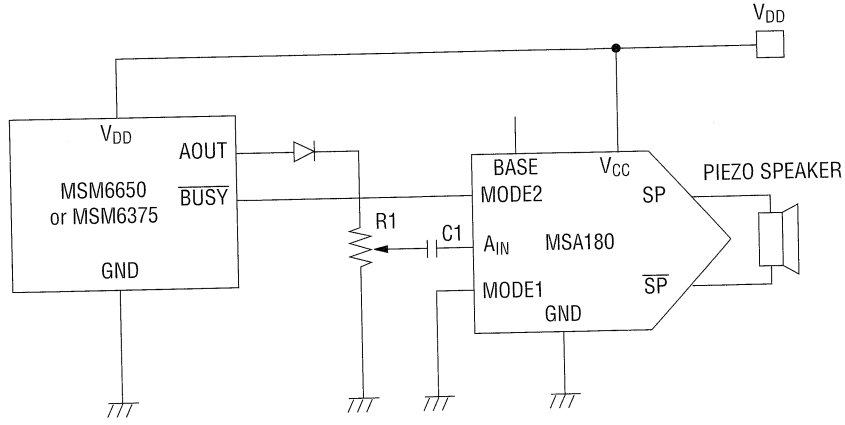
The cutoff frequency of the low-pass filter is calculated as follows:

$$f_C = \frac{1}{2\pi \times R2 \times C2} \text{ [Hz]}$$

For instance, if the cutoff frequency is 50 Hz, C2 is 0.1 µF and R2 is 30 kΩ. For a lower cutoff frequency, use a larger value for C2 or R2.

Application Example for Circuits Containing MSM6375/MSM6650 Family Speech Synthesizers

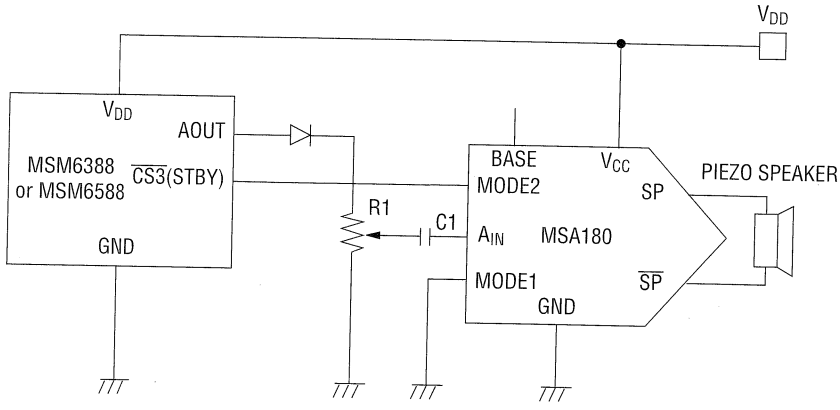
The example below shows how to connect the MSA180 with the MSM6375 or MSM6650 family speech synthesizers using the synthesizer's $\overline{BUSY}$ output to control operation and standby mode of the MSA180. As voice output stops, $\overline{BUSY}$ rises to the "H" level. For this reason, MODE2 is used to control operation and standby modes of the MSA180.



Notes:
1. The diode on A_{OUT} reduces pop noise.
2. This circuit makes use of the $\overline{BUSY}$ output of the speech synthesizer.
3. As the voice reproduction stops, $\overline{BUSY}$ outputs a "H" level to MODE2, setting the standby function.
4. If MODE2 is used, MODE1 must be connected to GND.
5. Leave the BASE pin open if it is not used.

Application Example for Circuits Containing the MSM6388/MSM6588 Speech Recorders

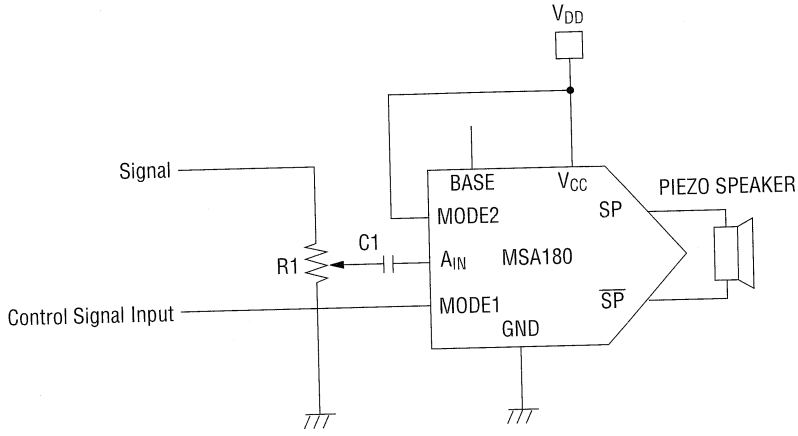
The example below shows how to connect the MSA180 with the MSM6388 or MSM6588 family speech recording ICs using the recorders' STBY output to control operation and standby mode of the MSA180. As voice output stops, STBY rises to the "H" level. For this reason, MODE2 is used to control operation and standby modes of the MSA180.



Notes:
1. The diode on A_{OUT} reduces pop noise.
2. This circuit makes use of the STBY output of the speech synthesizer.
3. As the voice reproduction stops, STBY outputs a "H" level to MODE2, setting the standby function.
4. If MODE2 is used, MODE1 must be connected to GND.
5. Leave the BASE pin open if it is not used.

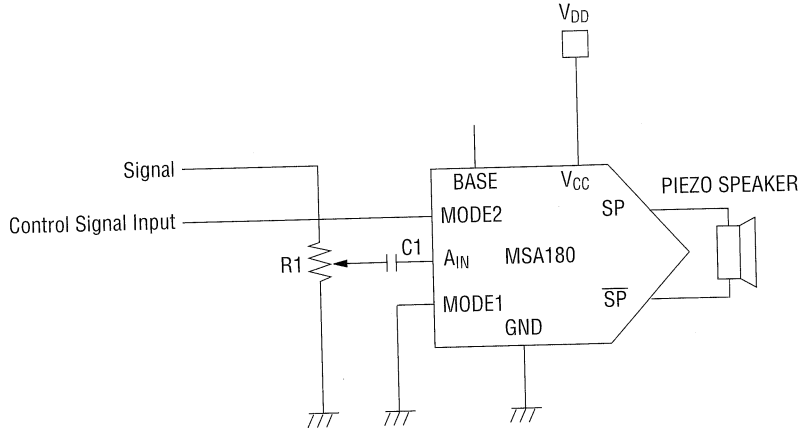
Application Examples for Circuits Containing a Microcontroller or Other Peripheral Devices

The circuit below uses a voice signal which rises high in operation mode. The MODE1 pin is used. Be sure to connect the MODE2 pin to V_{CC} pin.



Note: If the BASE pin is not used, leave it open.

In the circuit below, the signal falls low in operation mode. The MODE2 pin is used. Be sure to connect the MODE1 pin to the GND pin.



Note: If the BASE pin is not used, leave it open.

8 GENERAL-PURPOSE ROM CODE LIBRARY

Built-in mask ROM voice synthesis ICs and serial voice ROMs are manufactured according to customer orders. The following standard products are also available for general use and for sound quality evaluation and demonstration.

For details, feel free to contact our business department.

MSM6375 family general-purpose ROM codes

Model	Contents	Application	f_{SAM}	Option
MSM6372-100	Japanese female voice	Demonstration	6.4/8.0 kHz	B
MSM6372-119	Japanese female voice	Switching between FAX and telephone set	6.4 kHz	L
MSM6373-308	Japanese female voice	Answering machine and clock time reporting	4.0 kHz	A
MSM6373-329	English male voice	Answering machine and clock time reporting	4.0 kHz	G
MSM6374-006	Japanese female voice	Answering machine and clock time reporting	6.4 kHz	E
MSM6374-007	English female voice	Answering machine and clock time reporting	6.4 kHz	G
MSM6374-519	Japanese female voice	Answering machine and clock time reporting	5.3 kHz	A
MSM6374-544	English female voice	Answering machine and clock time reporting	6.4 kHz	G
MSM6374-545	Chinese female voice	Answering machine and clock time reporting	6.4 kHz	G
MSM6374-553	Japanese female voice	Answering machine and clock time reporting	6.4 kHz	G

MSM6650 family general-purpose ROM codes

Model	Contents	Applicaiton	f_{SAM}	Option
MSM6653-301	Demonstration	Demonstration message (in eight languages)	10.6/8.0/5.3 kHz	C
MSM6654-405	Demonstration	Demonstraiton message	Various frequencies	C
MSM6654-410	Demonstration	Demonstration (Japanese, English, sound effects)	Various frequencies	A
MSM6656-601	Demonstration	Demonstration message (Japanese)	Various frequencies	C
MSM6656-603	Demonstration	Demonstration message (English)	Various frequencies	C
MSM6658A-800	Demonstration	Demonstraiton message	Various frequencies	A

MSM6596A series general-purpose ROM codes

Model	Contents	Application	f_{SAM}	Option
MSM6596A-900	Voice in eight languages	Time stamp for answering machine demonstration	6.4/8.0 kHz	—
MSM6597A-750	Japanese and English female voice	Time stamp for answering machine demonstration	6.4/8.0 kHz	—

MSM9800 series general-purpose ROM codes

Model	Contents	Application	f_{SAM}	Option
MSM9802-200	Bell and birdcall	Demonstration (sound effects)	8.0 kHz	—

Details are shown in the following tables.

MSM6375 FAMILY GENERAL-PURPOSE ROM CODES

MSM6372-100 Voice Word Address Corresponding List
(for demonstration)

Specification: F_{OSC} = 64kHz, Option B

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	Stop Code	—	20		
01	いらっしゃいませ	8.0	21		
02	いらっしゃいませ	6.4	22		
03	ありがとうございました	8.0	23		
04	ありがとうございました	6.4	24		
05			25		
06			26		
07			27		
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10			30		
11			31		
12			32		
13			33		
14			34		
15			35		
16			36		
17			37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40			60		
41			61		
42			62		
43			63		
44			64		
45			65		
46			66		
47			67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51			71	↓	
52			72	↓	
53			73	↓	
54			74	↓	
55			75	↓	
56			76	↓	
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6372-119 Voice Word Address Corresponding List
(for telephone and facsimile switchable guidance in Japanese)
Specification: F_{OSC} = 64kHz, Option L

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20		
01	電話を呼び出しております	6.4	21		
02	ファクシミリにつながります	6.4	22		
03	送信ボタンを押して下さい	6.4	23		
04			24		
05			25		
06			26		
07			27		
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10			30		
11			31		
12			32		
13			33		
14			34		
15			35		
16			36		
17			37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40			60		
41			61		
42			62		
43			63		
44			64		
45			65		
46			66		
47			67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51			71	↓	
52			72		
53			73		
54			74		
55			75		
56			76		
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E	↓	
5F			7F		

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MSM6373-308 Voice Word Address Corresponding List (for Japanese Time Signal)

Specification: F_{OSC} = 64kHz, Option A

Address	Voice Word	fs(kHz)
00	Stop Code	—
01	いち (時)	4.0
02	に (時・分)	4.0
03	さん (時)	4.0
04	よ (時)	4.0
05	ご (時・分)	4.0
06	ろく (時)	4.0
07	なな (時・分)	4.0
08		
09		
0A		
0B		
0C		
0D		
0E		
0F		
10	はち (時・分)	4.0
11	く (時)	4.0
12	じゅう (時)	4.0
13	じゅういち (時)	4.0
14	じゅうに (時)	4.0
15		
16	ぜろ (件)	4.0
17	時	4.0
18		
19		
1A		
1B		
1C		
1D		
1E		
1F		

Address	Voice Word	fs(kHz)
20	いっ (分)	4.0
21	さん (分)	4.0
22	よん (分)	4.0
23		
24	ろっ (分)	4.0
25		
26		
27	きゅう (分)	4.0
28		
29		
2A		
2B		
2C		
2D		
2E		
2F		
30	無音 200 (ms)	4.0
31	じゅっ (分)	4.0
32	にじゅっ (分)	4.0
33	さんじゅっ (分)	4.0
34	よんじゅっ (分)	4.0
35	ごじゅっ (分)	4.0
36		
37		
38		
39		
3A		
3B		
3C		
3D		
3E		
3F		

Address	Voice Word	fs(kHz)
40	無音 30 (ms)	4.0
41	じゅう	4.0
42	にじゅう	4.0
43	さんじゅう	4.0
44	よんじゅう	4.0
45	ごじゅう	4.0
46	伝言	4.0
47	件	4.0
48		
49		
4A		
4B		
4C		
4D		
4E		
4F		
50	無音 50 (ms)	4.0
51	午前	4.0
52	午後	4.0
53	ぶん	4.0
54	ふん	4.0
55	です	4.0
56		
57		
58		
59		
5A		
5B		
5C		
5D		
5E		
5F		

Address	Voice Word	fs(kHz)
60	シャープ	4.0
61	スター	4.0
62	ポーズ	4.0
63		
64	日 (にち)	6.4
65		
66		
67		
68		
69		
6A		
6B		
6C		
6D		
6E		
6F		
70	BEEP Sound Code	
71	———	
72		
73		
74		
75		
76		
77	▼	
78	Test Code	
79		
7A	———	
7B		
7C		
7D		
7E	▼	
7F		

MSM6373-329 Voice Word Address Corresponding List (for English Time Signal)
Specification: F_{OSC} = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	SIX-	4.0
01	ONE	4.0	21	SEVEN-	4.0
02	TWO	4.0	22	EIGHT-	4.0
03	THREE	4.0	23	NINE-	4.0
04	FOUR	4.0	24	TWENTY	4.0
05	FIVE	4.0	25	THIRTY	4.0
06	SIX	4.0	26	FORTY	4.0
07	SEVEN	4.0	27	FIFTY	4.0
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	EIGHT	4.0	30	OH	4.0
11	NINE	4.0	31	AM	4.0
12	TEN	4.0	32	PM	4.0
13	ELEVEN	4.0	33	SUN-	4.0
14	TWELVE	4.0	34	MON-	4.0
15	THIR-	4.0	35	TUES-	4.0
16	FOUR-	4.0	36	WEDNES-	4.0
17	FIF-	4.0	37	THURS-	4.0
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	FRI-	4.0	60		
41	SATUR-	4.0	61		
42	-DAY	4.0	62		
43	-TEEN	4.0	63		
44	Set the DAY and TIME	4.0	64		
45	No Voice 30 m sec	4.0	65		
46			66		
47			67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51			71		
52			72		
53			73		
54			74		
55			75		
56			76		
57			77		
58			78	Test Code	
59			79		
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E		
5F			7F		

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MSM6374-006 Voice Word Address Corresponding List (for Japanese Time Signal)

Specification: F_{OSC} = 64kHz, Option E

Address	Voice Word	fs(kHz)
00	STOP Code	—
01	いち (時)	6.4
02	に (時、分)	6.4
03	さん (時)	6.4
04	よ (時)	6.4
05	ご (時)	6.4
06	ろく (時)	6.4
07	なな (時)	6.4
08		
09		
0A		
0B		
0C		
0D		
0E		
0F		
10	はち (時)	6.4
11	く (時)	6.4
12	じゅう (時)	6.4
13	じゅういち (時)	6.4
14	じゅうに (時)	6.4
15	れい (時)	6.4
16		
17	時	6.4
18		
19		
1A		
1B		
1C		
1D		
1E		
1F		

Address	Voice Word	fs(kHz)
20	いっ (分)	6.4
21	さん (分)	6.4
22	よん (分)	6.4
23	ご (分)	6.4
24	ろっ (分)	6.4
25	なな (分)	6.4
26	はっ (分)	6.4
27	きゅう (分)	6.4
28		
29		
2A		
2B		
2C		
2D		
2E		
2F		
30		
31	じゅっ (分)	6.4
32	にじゅっ (分)	6.4
33	さんじゅっ (分)	6.4
34	よんじゅっ (分)	6.4
35	ごじゅっ (分)	6.4
36		
37		
38		
39		
3A		
3B		
3C		
3D		
3E		
3F		

Address	Voice Word	fs(kHz)
40		
41	じゅう	6.4
42	にじゅう	6.4
43	さんじゅう	6.4
44	よんじゅう	6.4
45	ごじゅう	6.4
46		
47	件	6.4
48		
49		
4A		
4B		
4C		
4D		
4E		
4F		
50		
51	午前	6.4
52	午後	6.4
53	ぶん	6.4
54	ふん	6.4
55	です	6.4
56		
57	メモ	6.4
58		
59		
5A		
5B		
5C		
5D		
5E		
5F		

Address	Voice Word	fs(kHz)
60		
61		
62		
63		
64		
65		
66		
67		
68		
69		
6A		
6B		
6C		
6D		
6E		
6F		
70	BEEP Sound Code	
71		
72		
73		
74		
75		
76		
77		
78	Test Code	
79		
7A		
7B		
7C		
7D		
7E		
7F		

MSM6374-007 Voice Word Address Corresponding List (for English Time Signal)
Specification: F_{OSC} = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	TY-FOUR	6.4
01	ALARM	6.4	21	TY-FIVE	6.4
02	SETTING	6.4	22	TY-SIX	6.4
03	ON	6.4	23	TY-SEVEN	6.4
04	OFF	6.4	24	TY-EIGHT	6.4
05	HOUR	6.4	25	TY-NINE	6.4
06	MINUTE	6.4	26	-TY	6.4
07	SECOND	6.4	27	-TEEN	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	NINE	6.4	30	ONE	6.4
11	TEN	6.4	31	TWO	6.4
12	ELEVEN	6.4	32	THREE	6.4
13	TWELVE	6.4	33	FOUR	6.4
14	ZERO-	6.4	34	FIVE	6.4
15	TWEN-	6.4	35	SIX	6.4
16	THIR-	6.4	36	SEVEN	6.4
17	FIF-	6.4	37	EIGHT	6.4
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	O'CLOCK	6.4	60		
41	SIX-	6.4	61		
42	SEVEN-	6.4	62		
43	EIGHT-	6.4	63		
44	NINE-	6.4	64		
45	TY-ONE	6.4	65		
46	TY-TWO	6.4	66		
47	TY-THREE	6.4	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	OH	6.4	70	BEEP Sound Code	
51	FOR-	6.4	71	⟶	
52	TO GO	6.4	72		
53	IT'S	6.4	73		
54	No Voice 50 ms	6.4	74		
55	No Voice 200 ms	6.4	75		
56	AM	6.4	76	⟶	
57	PM	6.4	77		
58			78	Test Code	
59			79	⟶	
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E	⟶	
5F			7F		

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MSM6374-519 Voice Word Address Corresponding List (for Japanese Time Signal)

Specification: F_{OSC} = 53kHz, Option A

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	無音 100 (ms)	3.3
01	いち (月, 日, 時, 秒)	5.3	21	じゅっ (10分, 件)	5.3
02	に (時, 2分, 件)	5.3	22	に (20分/秒)	5.3
03	さん (時)	5.3	23		
04	よ (時)	5.3	24		
05	ご (月, 日, 時, 分, 秒, 件)	5.3	25	ご (50分/秒)	5.3
06	ろく (月, 日, 時, 秒)	5.3	26	じゅっ (20, 30, 40分)	5.3
07	なな (月, 日, 時, 分, 秒, 件)	5.3	27	じゅう (20, 30, 40秒)	5.3
08	はち (月, 日, 時, 分, 秒, 件)	5.3	28	午前	5.3
09	く (月, 日, 時)	5.3	29	午後	5.3
0A	じゅう (月, 日, 10時, 10秒)	5.3	2A	時	5.3
0B	じゅういち (月, 日, 時, 秒)	5.3	2B	ぶん	5.3
0C	じゅうに (月, 日, 時, 分, 秒, 件)	5.3	2C	ふん	5.3
0D			2D	秒	5.3
0E			2E	です	5.3
0F			2F		
10	れい (時, 分, 秒)	5.3	30	無音 30 (ms)	3.3
11	いっ (分, 件)	5.3	31	じゅう～ (11-19分/件)	5.3
12			32	に (月, 日, 21-29分/秒, 2秒)	5.3
13	さん(月, 日, 3, 13, 23, 30-39分/秒, 件)	5.3	33		
14	よん (日, 4, 14, 24, 40-49分/秒, 件)	5.3	34		
15			35	ごじゅう～ (51-59分/秒)	5.3
16	ろっ (分, 件)	5.3	36	じゅう～ (21-29, 31-39, 41-49分/秒)	5.3
17			37		
18			38		
19	きゅう (分, 秒, 件)	5.3	39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	日	5.3	60	BEEP音 (64 ms, 883 Hz)	5.3
41	月	5.3	61	BEEP音 (128 ms, 883 Hz)	5.3
42	火	5.3	62		
43	水	5.3	63		
44	木	5.3	64		
45	金	5.3	65		
46	土	5.3	66		
47	曜日	5.3	67		
48	シャープ	5.3	68		
49	アスター	5.3	69		
4A	ポーズ	5.3	6A		
4B	PB	5.3	6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	無音 50 (ms)	3.3	70	BEEP Sound Code	
51	ぜろ (件)	5.3	71		
52	伝言	5.3	72		
53	件	5.3	73		
54	し (月)	5.3	74		
55	月 (がつ)	5.3	75		
56	日 (にち)	5.3	76		
57	しち (月)	5.3	77		
58			78	Test Code	
59			79		
5A	只今留守にしております	5.3	7A		
5B	後ほどおかけ直し下さい	5.3	7B		
5C	ピーという音の後にお話し下さい	5.3	7C		
5D			7D		
5E			7E		
5F			7F		

8

0時 0分です (10) (2A) (10) (2C) (2E)
1時 1分です (01) (〃) (11) (2B) (〃) 1秒 (01) (2D)
2時 2分です (02) (〃) (02) (2C) (〃) 2秒 (32) (2D)
3時 3分です (03) (〃) (13) (2B) (〃)
4時 4分です (04) (〃) (14) (2B) (〃)
5時 5分です (05) (〃) (05) (2C) (〃)
6時 6分です (06) (〃) (16) (2B) (〃) 6秒 (06) (2D)
7時 7分です (07) (〃) (07) (2C) (〃)
8時 8分です (08) (〃) (08) (2C) (〃)
9時 9分です (09) (〃) (19) (2C) (〃)

10時 10分です (0A) (2A) (21) (2B) (2E) 10秒 (0A) (2D)
11時 11分です (0B) (〃) (31) (11) (2B) (〃) 11秒 (0B) (2D)
12時 12分です (0C) (〃) (0C) (2C) (〃)
3時 13分です (03) (〃) (31) (13) (2B) (〃)
4時 14分です (04) (〃) (〃) (14) (2B) (〃)
5時 15分です (05) (〃) (〃) (05) (2C) (〃)
6時 16分です (06) (〃) (〃) (16) (2B) (〃) 16秒 (31) (06) (2D)
7時 17分です (07) (〃) (〃) (07) (2C) (〃)
8時 18分です (08) (〃) (〃) (08) (2C) (〃)
9時 19分です (09) (〃) (〃) (19) (2C) (〃)

0時 20分です (10) (2A) (22) (26) (2B) (2E) 20秒 (22) (27) (2D)
1時 21分です (01) (〃) (32) (36) (11) (2B) (〃) 21秒 (32) (36) (01) (2D)
2時 22分です (02) (〃) (〃) (〃) (02) (2C) (〃) 22秒 (32) (36) (32) (2D)
3時 23分です (03) (〃) (〃) (〃) (13) (2B) (〃)
4時 24分です (04) (〃) (〃) (〃) (14) (2B) (〃)
5時 25分です (05) (〃) (〃) (〃) (05) (2C) (〃)
6時 26分です (06) (〃) (〃) (〃) (16) (2B) (〃) 26秒 (32) (36) (06) (2D)
7時 27分です (07) (〃) (〃) (〃) (07) (2C) (〃)
8時 28分です (08) (〃) (〃) (〃) (08) (2C) (〃)
9時 29分です (09) (〃) (〃) (〃) (19) (2C) (〃)

0時 30分です (10) (2A) (13) (26) (2B) (2E) 30秒 (13) (27) (2D)
1時 31分です (01) (〃) (〃) (36) (11) (2B) (〃) 31秒 (13) (36) (01) (2D)
2時 32分です (02) (〃) (〃) (〃) (02) (2C) (〃) 32秒 (13) (36) (32) (2D)
3時 33分です (03) (〃) (〃) (〃) (13) (2B) (〃)
4時 34分です (04) (〃) (〃) (〃) (14) (2B) (〃)
5時 35分です (05) (〃) (〃) (〃) (05) (2C) (〃)
6時 36分です (06) (〃) (〃) (〃) (16) (2B) (〃) 36秒 (13) (36) (06) (2D)
7時 37分です (07) (〃) (〃) (〃) (07) (2C) (〃)
8時 38分です (08) (〃) (〃) (〃) (08) (2C) (〃)
9時 39分です (09) (〃) (〃) (〃) (19) (2C) (〃)

0時 40分です (10) (2A) (14) (26) (2B) (2E) 40秒 (14) (27) (2D)
1時 41分です (01) (〃) (〃) (36) (11) (2B) (〃) 41秒 (14) (36) (01) (25)
2時 42分です (02) (〃) (〃) (〃) (02) (2C) (〃) 42秒 (14) (36) (32) (2D)
3時 43分です (03) (〃) (〃) (〃) (13) (2B) (〃)
4時 44分です (04) (〃) (〃) (〃) (14) (2B) (〃)
5時 45分です (05) (〃) (〃) (〃) (05) (2C) (〃)
6時 46分です (06) (〃) (〃) (〃) (16) (2B) (〃) 46秒 (14) (36) (06) (2D)
7時 47分です (07) (〃) (〃) (〃) (07) (2C) (〃)
8時 48分です (08) (〃) (〃) (〃) (08) (2C) (〃)
9時 49分です (09) (〃) (〃) (〃) (19) (2C) (〃)

0時 50分です (10) (2A) (25) (26) (2B) (2E) 50秒 (25) (27) (2D)
1時 51分です (01) (〃) (35) (11) (2B) (〃) 51秒 (35) (01) (2D)
2時 52分です (02) (〃) (〃) (02) (2C) (〃) 52秒 (35) (32) (2D)
3時 53分です (03) (〃) (〃) (13) (2B) (〃)
4時 54分です (04) (〃) (〃) (14) (2B) (〃)
5時 55分です (05) (〃) (〃) (05) (2C) (〃)
6時 56分です (06) (〃) (〃) (16) (2B) (〃) 56秒 (35) (06) (2D)
7時 57分です (07) (〃) (〃) (07) (2C) (〃)
8時 58分です (08) (〃) (〃) (08) (2C) (〃)
9時 59分です (09) (〃) (〃) (19) (2C) (〃)

8

1月 1日 (01) (55) (01) (56)
2月 2日 (32) (55) (32) (56)
3月 3日 (13) (55) (13) (56)
4月 4日 (54) (55) (14) (56)
5月 5日 (05) (55) (05) (56)
6月 6日 (06) (55) (06) (56)
7月 7日 (57) (55) (07) (56)
8月 8日 (08) (55) (08) (56)
9月 9日 (09) (55) (09) (56)
10月 10日 (0A) (55) (0A) (56)
11月 11日 (0B) (55) (0B) (56)
12月 12日 (0C) (55) (0C) (56)

MSM6374-544 Voice Word Address Corresponding List (for English Time Signal)

Specification: F_{OSC} = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	-TY	6.4
01	ONE	6.4	21	TY-ONE	6.4
02	TWO	6.4	22	TY-TWO	6.4
03	THREE	6.4	23	TY-THREE	6.4
04	FOUR	6.4	24	TY-FOUR	6.4
05	FIVE	6.4	25	TY-FIVE	6.4
06	SIX	6.4	26	TY-SIX	6.4
07	SEVEN	6.4	27	TY-SEVEN	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	EIGHT	6.4	30	TY-EIGHT	6.4
11	NINE	6.4	31	TY-NINE	6.4
12	TEN	6.4	32	OH	6.4
13	ELEVEN	6.4	33	TEEN	6.4
14	TWELVE	6.4	34	TEEN	6.4
15	ZERO	6.4	35	No Voice 200 ms	6.4
16	No Voice 50 ms	6.4	36	No Voice 200 ms	6.4
17	No Voice 50 ms	6.4	37	No Voice 200 ms	6.4
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	EIGHT-	6.4	60	SUN-	6.4
41	NINE-	6.4	61	MON-	6.4
42	TWEN-	6.4	62	TUES-	6.4
43	THIR-	6.4	63	WEDNES-	6.4
44	FOR-	6.4	64	THURS-	6.4
45	FIF-	6.4	65	FRI-	6.4
46	SIX-	6.4	66	SATUR-	6.4
47	SEVEN-	6.4	67	-DAY	6.4
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	IT'S	6.4	70	BEEP Sound Code	
51	O'CLOCK	6.4	71	←	
52	AM	6.4	72		
53	PM	6.4	73		
54	SET	6.4	74		
55	DATA	6.4	75		
56	TIME	6.4	76		
57			77	→	
58			78	Test Code	
59			79	←	
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E		
5F			7F	→	

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MSM6374-545 Voice Word Address Corresponding List (for Chinese Time Signal)

Specification: F_{OSC} = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	1 (分)	6.4
01	1 (時)	6.4	21	2 (分)	6.4
02	2 (時)	6.4	22	3 (分)	6.4
03	3 (時)	6.4	23	4 (分)	6.4
04	4 (時)	6.4	24	5 (分)	6.4
05	5 (時)	6.4	25	6 (分)	6.4
06	6 (時)	6.4	26	7 (分)	6.4
07	7 (時)	6.4	27	8 (分)	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	8 (時)	6.4	30	9 (分)	6.4
11	9 (時)	6.4	31		
12	10 (時)	6.4	32	0 (分)	6.4
13	11 (時)	6.4	33	10 (分, 例如1×分)	6.4
14	12 (時)	6.4	34	2 (分, 例如2×分)	6.4
15			35	3 (分, 例如3×分)	6.4
16			36	4 (分, 例如4×分)	6.4
17	點 (時)	6.4	37	5 (分, 例如5×分)	6.4
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	無聲音 200ms	4.0	60		
41	無聲音 50ms	4.0	61		
42	無聲音 30ms	4.0	62		
43			63		
44	早上	6.4	64		
45	下午	6.4	65		
46			66		
47	分	6.4	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	鐘聲	6.4	70	BEEP Sound Code	
51			71		
52			72		
53			73		
54			74		
55			75		
56			76		
57			77		
58			78	Test Code	
59			79		
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E		
5F			7F		

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MSM6374-553 Voice Word Address Corresponding List (for Japanese Time Signal)
Specification: F_{OSC} = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	いっ (分)	6.4
01	いち (時)	6.4	21	さん (分)	6.4
02	に (時、分)	6.4	22	よん (分)	6.4
03	さん (時)	6.4	23	ご (分)	6.4
04	よ (時)	6.4	24	ろっ (分)	6.4
05	ご (時)	6.4	25	なな (分)	6.4
06	ろく (時)	6.4	26	はっ (分)	6.4
07	なな (時)	6.4	27	きゅう (分)	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	はち (時)	6.4	30		
11	く (時)	6.4	31	じゅっ (分)	6.4
12	じゅう (時)	6.4	32	にじゅっ (分)	6.4
13	じゅういち (時)	6.4	33	さんじゅっ (分)	6.4
14	じゅうに (時)	6.4	34	よんじゅっ (分)	6.4
15	れい (時)	6.4	35	ごじゅっ (分)	6.4
16			36		
17	時	6.4	37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40			60		
41	じゅう	6.4	61		
42	にじゅう	6.4	62		
43	さんじゅう	6.4	63		
44	よんじゅう	6.4	64		
45	ごじゅう	6.4	65		
46			66		
47	件	6.4	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51	午前	6.4	71	———	
52	午後	6.4	72	———	
53	ぶん	6.4	73		
54	ふん	6.4	74		
55	です	6.4	75		
56			76	▼	
57	メモ	6.4	77	▼	
58			78	Test Code	
59			79	———	
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E	▼	
5F			7F	▼	

MSM6650 Family general-purpose ROM Codes

MSM6653-301 Edit ROM Address Corresponding List (for Demonstration)
Specification: Option C

X address	Voice word
00	—
01	Pekingese (0.8 kHz) 0.5 sec English (0.8 kHz) 0.5 sec German (0.8 kHz) 0.5 sec French (0.8 kHz) 0.5 sec
02	Spanish (0.8 kHz) 0.5 sec Korean (0.8 kHz) 0.5 sec Japanese (0.8 kHz) 0.5 sec Italian (0.8 kHz) 0.5 sec
03	Pekingese (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
04	English (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
05	German (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
06	French (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
07	Spanish (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
08	Korean (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
09	Japanese (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
0A	Italian (10.6 kHz) 0.5 sec (8.0 kHz) 0.5 sec (5.3 kHz)
0B	Pekingese (8.0 kHz) (Fade-out, 4 times)
0C	English (8.0 kHz) (Fade-out, 4 times)
0D	German (8.0 kHz) (Fade-out, 4 times)
0E	French (8.0 kHz) (Fade-out, 4 times)
0F	Spanish (8.0 kHz) (Fade-out, 4 times)
10	Korean (8.0 kHz) (Fade-out, 4 times)
11	Japanese (8.0 kHz) (Fade-out, 4 times)
12	Italian (8.0 kHz) (Fade-out, 4 times)
13	Pekingese (8.0 kHz) (Echo)
14	English (8.0 kHz) (Echo)
15	German (8.0 kHz) (Echo)
16	French (8.0 kHz) (Echo)
17	Spanish (8.0 kHz) (Echo)
18	Korean (8.0 kHz) (Echo)
19	Japanese (8.0 kHz) (Echo)
1A	Italian (8.0 kHz) (Echo)
1B	Pekingese (10.6 kHz)
1C	Pekingese (8.0 kHz)
1D	Pekingese (5.3 kHz)
1E	English (10.6 kHz)
1F	English (8.0 kHz)

MSM6653-301 Edit ROM Address Corresponding List (for Demonstration)
Specification: Option C

(Continued)

X address	Voice word
20	English (5.3 kHz)
21	German (10.6 kHz)
22	German (8.0 kHz)
23	German (5.3 kHz)
24	French (10.6 kHz)
25	French (8.0 kHz)
26	French (5.3 kHz)
27	Spanish (10.6 kHz)
28	Spanish (8.0 kHz)
29	Spanish (5.3 kHz)
2A	Korean (10.6 kHz)
2B	Korean (8.0 kHz)
2C	Korean (5.3 kHz)
2D	Japanese (10.6 kHz)
2E	Japanese (8.0 kHz)
2F	Japanese (5.3 kHz)
30	Italian (10.6 kHz)
31	Italian (8.0 kHz)
32	Italian (5.3 kHz)

MSM6653-301 Voice Word Address Corresponding List (for Demonstration)

Y address	Voice word		Playback method	Frequency [kHz]
00	—		—	—
01	Pekingese 2-A	(Female)	ADPCM	10.6
02	Pekingese 2-A	(Female)	ADPCM	8.0
03	Pekingese 2-A	(Female)	ADPCM	5.3
04	English 2-B	(Female)	ADPCM	10.6
05	English 2-B	(Female)	ADPCM	8.0
06	English 2-B	(Female)	ADPCM	5.3
07	German 2-A	(Male)	ADPCM	10.6
08	German 2-A	(Male)	ADPCM	8.0
09	German 2-A	(Male)	ADPCM	5.3
0A	French 2-A	(Female)	ADPCM	10.6
0B	French 2-A	(Female)	ADPCM	8.0
0C	French 2-A	(Female)	ADPCM	5.3
0D	Spanish 2-A	(Male)	ADPCM	10.6
0E	Spanish 2-A	(Male)	ADPCM	8.0
0F	Spanish 2-A	(Male)	ADPCM	5.3
10	Korean 2-A	(Female)	ADPCM	10.6
11	Korean 2-A	(Female)	ADPCM	8.0
12	Korean 2-A	(Female)	ADPCM	5.3
13	Japanese 2-A	(Female)	ADPCM	10.6
14	Japanese 2-A	(Female)	ADPCM	8.0
15	Japanese 2-A	(Female)	ADPCM	5.3
16	Italian 2-C	(Female)	ADPCM	10.6
17	Italian 2-C	(Female)	ADPCM	8.0
18	Italian 2-C	(Female)	ADPCM	5.3

MSM6654-405 Editing ROM Address Corresponding List (for Demonstration)
Specification: Option C

Address	Voice word	Remarks
X00	—	No voice phrase
X01	Y01+Y02+Y03+Y04+Y05+Y06	
X02	(F4) Y07	(F4) Fade-out + four repetitions
X03	(E) Y08	(E) Echo (No. 1)
X04	(E) Y08	(E) Echo (No. 2)
X05	(E) Y08	(E) Echo (No. 3)
X06	(2) Y09+<Beep tone (4 times)>	(2) Two repetitions
X07	(F4) (4) (E) Y08 (BGM) Y0D+Y0A	Phrase playback, with a melody to be repeated four times as BGM, then an echo playback
X08	(F4) Y07	
X09	(F4) (F4) (F4) Y0E+Y0F+Y10	
X0A	(F4) (F4) Y07+Y07	
X0B	Y0B+Y0C	
X0C	Y0A+Y0D	(4) Four repetitions
X0D	Y06	
X0E	(F2) Y09+<Beep tone (4 times)>	(F2) Fade-out + two repetitions
X0F	—	
X10	—	No voice phrase
X11	Y01	
X12	Y0A	
X13	Y02	
X14	Y01	
X15	Y03	
X16	Y04	
X17	Y05	

MSM6654-405 Edit ROM Address Corresponding List (for Demonstration)
Specification: Option C

(Continued)

Address	Voice word	Remarks
X18	Y0C	
X19	Y06	
X1A	Y0A	
X1B	Y07	
X1C	Y0B	
X1D	Y0E	
X1E	Y0C	
X1F	Y0F	
X20	—	No voice phrase
X21	Y08	
X22	Y09	
X23	Y0B	
X24	Y0A	
X25	Y0E	
X26	Y0F	
X27	Y10	
X28	Y02	
X29	Y03	
X2A	Y04	
X2B	Y05	
X2C	Y06	
X2D	Y07	
X2E	Y08	
X2F	Y09	

MSM6654-405 Voice Word Address Corresponding List (for Demonstration)

Address	Voice phrase contents
Y00	—
Y01	5種類のサンプリング周波数による音の違いをお聞き下さい。(Voice)
Y02	4 kHz (Voice) + <music>
Y03	5.3 kHz (Voice) + <music>
Y04	6.4 kHz (Voice) + <music>
Y05	8 kHz (Voice) + <music>
Y06	16 kHz (Voice) + <music>
Y07	フェードアウト機能 (Voice)
Y08	2チャンネルミキシング機能 (Voice)
Y09	ビープ音 (Voice)
Y0A	メロディ機能 (Voice)
Y0B	PCM (Voice)
Y0C	<1kHz sinusoidal wave (0.5 second) >
Y0D	<Melody sound (cuckoo) >
Y0E	<500 Hz sinusoidal wave (0.3 second) >
Y0F	<500 Hz sinusoidal wave (0.3 second) >
Y10	<500 Hz sinusoidal wave (0.1 second) >

MSM6654-410 Edit ROM Address Corresponding List (for Demonstration)
Specification: Option A

X address	Voice word
00	—
01	" ありがとう　ありがとう　ありがとう" (0.5 second between phrases)
02	"Thanks a lot Thanks a lot Thanks a lot" (0.5 second between phrases)
03	" ありがとう" (Echo)
04	"Thanks a lot" (Echo)
05	" ありがとう" (Fade-out, 4 times)
06	"Thanks a lot" (Fade-out, 4 times)
07	"Beep Beep Beep Explosion sound" (Silence for 1 second between phrases)
08	"rring, rring, · · · " (Fade-in, 3 times) " 申し訳ございません。ただ今席をはずしております。"
09	(Doorbell sound) (Echo) " 上へまいります。"
0A	(Doorbell sound) (Echo) " 下へまいります。"
0B	" ありがとう" (f_S=10.6kHz)
0C	" ありがとう" (f_S=8.0kHz)
0D	" ありがとう" (f_S=5.3kHz)
0E	"Thanks a lot" (f_S=10.6 kHz)
0F	"Thanks a lot" (f_S=8.0 kHz)
10	"Thanks a lot" (f_S=5.3 kHz)
11	"Beep" (Sound effects)
12	(Explosion sound)
13	"rring, rring, · · · " (Telephone bell sound)
14	" 申し訳ございません。"
15	" ただ今席をはずしております。"
16	(Doorbell sound)
17	" 上へまいります。"
18	" 下へまいります。"

MSM6654-410 Voice Word Address Corresponding List (for Demonstration)

Y address	Voice word	Playback method	Frequency [kHz]
00	—	—	—
01	"ありがとう"	ADPCM	10.6
02	"ありがとう"	ADPCM	8.0
03	"ありがとう"	ADPCM	5.3
04	"Thanks a lot"	ADPCM	10.6
05	"Thanks a lot"	ADPCM	8.0
06	"Thanks a lot"	ADPCM	5.3
07	"Beep" (Sound effects)	ADPCM	10.6
08	(Explosion sound)	ADPCM	10.6
09	"rring, rring, · · · " (Telephone bell sound)	ADPCM	10.6
0A	"申し訳ございません。"	ADPCM	10.6
0B	"ただ今席を外しております。"	ADPCM	10.6
0C	(Doorbell sound)	ADPCM	10.6
0D	"上へまいります。"	ADPCM	10.6
0E	"下へまいります。"	ADPCM	10.6

MSM6656-601 Edit ROM Address Corresponding List (for Demonstration)
Specification: Option C

X address	Voice word
01	"4種類のサンプリング周波数による、音の違いをお聞き下さい。 16 kHz <Music> 8 kHz <Music> 6.4 kHz <Music> 5.3 kHz <Music>"
02	"ADPCM ' キャー ' <A female's scream> PCM ' キャー ' <A female's scream> (Playback method: PCM)"
03	" フェードアウト機能 " <Cuckoo sound> (4 times)"
04	" 2チャンネルミキシング機能 ' エコーですね。' (echo) ' このようにBGMをかけることも出来ます。' (with BGM)"
05	" ビープ音 'Beep Beep Beep Beep' (Edit ROM)"
06	<Melody>
07	"16 kHz <Music>"
08	"8 kHz <Music>"
09	"6.4 kHz <Music>"
0A	"5.3 kHz <Music>"

MSM6656-603 Edit ROM Address Corresponding List (for Demonstration)
Specification: Option C

X address	Voice word
01	"One can hear four different sounds by using four kinds of sampling frequency. 16 kHz <MUSIC> 8 kHz <MUSIC> 6.4 kHz <MUSIC> 5.3 kHz <MUSIC>"
02	"ADPCM <A female's scream> PCM <A female's scream>"
03	"Fade-out function <a cuckoo sound> (4 times)"
04	"2-channel mixing 'Echo sounds' (with echo) 'Background music is also produced by mixing various kinds of sounds' (with BGM)"
05	"Beep tone <Beep Beep Beep Beep>"
06	"Melody 'Happy Birthday' "
07	"16 kHz <MUSIC>"
08	"8 kHz <MUSIC>"
09	"6.4 kHz <MUSIC>"
0A	"5.3 kHz <MUSIC>"

MSM6658A-800 Edit ROM Address Corresponding List (for Demonstration)
Specification: Option A

X address	Voice word	
00	—	—
01	"32 kHz <Music>"	Japanese
02	"16 kHz <Music>"	Japanese
03	"12.8 kHz <Music>"	Japanese
04	"10.6 kHz <Music>"	Japanese
05	"8 kHz <Music>"	Japanese
06	"6.4 kHz <Music>"	Japanese
07	"5.3 kHz <Music>"	Japanese
08	"ADPCM <A female's scream> (Playback method: ADPCM) PCM <A female's scream> (Playback method: PCM)"	Japanese
09	" フェードアウト機能 <Cuckoo sound> (Four repetitions. Fade-out)"	Japanese
0A	" 2チャンネルミキシング機能 ' エコーですね。' (echo) ' このようにBGMをかけることも出来ます ' (with BGM)"	Japanese
0B	" ビープ音 <Beep tone>"	Japanese
0C	" メロディ <Melody>"	Japanese
0D		
0E		
0F		
10		
11	"32 kHz <Music>"	English
12	"16 kHz <Music>"	English
13	"12.8 kHz <Music>"	English
14	"10.6 kHz <Music>"	English
15	"8 kHz <Music>"	English
16	"6.4 kHz <Music>"	English
17	"5.3 kHz <Music>"	English
18	"ADPCM <A feamale's scream> (Playback method: ADPCM) PCM <A feamale's scream> (Playback method: PCM)"	English
19	"Fade-out function. <Cuckoo sound> (Four repetitions. Fade-out)"	English
1A	"2-Channel Mixing 'Echo sounds' (Echo) 'Back ground music is also produced by mixing various kinds of sounds' (with BGM)"	English
1B	"Beep tone <Beep tone>"	English
1C	"Melody <Melody>"	English

MSM6658A-800 Voice Word Address Corresponding List (for Demonstration)

Y address	Voice word		Playback method	Frequency [kHz]
00	—		—	—
01	32 kHz	Japanese	ADPCM	32.0
02	16 kHz	Japanese	ADPCM	16.0
03	12.8 kHz	Japanese	ADPCM	12.8
04	10.6 kHz	Japanese	ADPCM	10.6
05	8 kHz	Japanese	ADPCM	8.0
06	6.4 kHz	Japanese	ADPCM	6.4
07	5.3 kHz	Japanese	ADPCM	5.3
08	ADPCM	Japanese	ADPCM	6.4
09	PCM	Japanese	ADPCM	6.4
0A	フェードアウト機能	Japanese	ADPCM	6.4
0B	2チャンネルミキシング	Japanese	ADPCM	6.4
0C	エコーですね	Japanese	ADPCM	6.4
0D	このようにBGMをかけることも出来ます	Japanese	ADPCM	6.4
0E	ビープ音	Japanese	ADPCM	6.4
0F	メロディ	Japanese	ADPCM	6.4
10	32 kHz	English	ADPCM	32.0
11	16 kHz	English	ADPCM	16.0
12	12.8 kHz	English	ADPCM	12.8
13	10.6 kHz	English	ADPCM	10.6
14	8 kHz	English	ADPCM	8.0
15	6.4 kHz	English	ADPCM	6.4
16	5.3 kHz	English	ADPCM	5.3
17	ADPCM	English	ADPCM	6.4
18	PCM	English	ADPCM	6.4
19	Fede-out function	English	ADPCM	6.4
1A	2-channel Mixing	English	ADPCM	6.4
1B	Echo Sound	English	ADPCM	6.4
1C	Background music is also produced by mixing various kinds of sounds	English	ADPCM	6.4
1D	Beep Tone	English	ADPCM	6.4
1E	Melody	English	ADPCM	6.4
1F	<Music (32.0 kHz)>		ADPCM	32.0

MSM6658A-800 Voice Word Address Corresponding List (for Demonstration)

(Continued)

Y address	Voice word	Playback method	Frequency [kHz]
20	<Music> (16.0 kHz)	ADPCM	16.0
21	<Music> (12.8 kHz)	ADPCM	12.8
22	<Music> (10.8 kHz)	ADPCM	10.6
23	<Music> (8.0 kHz)	ADPCM	8.0
24	<Music> (6.4 kHz)	ADPCM	6.4
25	<Music> (5.3 kHz)	ADPCM	5.3
26	<A female's scream> (playback method: ADPCM)	ADPCM	10.6
27	<A female's scream> (playback method: PCM)	PCM	10.6
28	<Cuckoo sound>	ADPCM	8.0
29	<BGM>	ADPCM	6.4
2A	<Melody>	ADPCM	8.0

MSM6596A GENERAL PURPOSE ROM CODES

Contents of MSM6596A-900 addresses

Address	Contents
01 to 2F	MSM6374–007 (Time stamp)
30 to 57	MSM6596–600 (Only time stamp)
58 to 5F	Japanese week day
60 to 6F	Greetings in eight languages
70 to 73	ADPCM long-change phrases (Japanese/English)
74 to 76	Effect sound
77 to 79	Animal voice

Greetings in eight languages at addresses 60 to 6F

Address	Contents
Chinese (60)	你好
Chinese (61)	再見
English (62)	Hello
English (63)	Good-by
German (64)	Guten tag
German (65)	Aufwiedersehen
French (66)	Bonjour Monsieur
French (67)	Au revoir Monsieur
Spanish (68)	Buenos dias
Spanish (69)	Adios
Korean (6A)	안녕하십니까?
Korean (6B)	안녕하 가십시요.
Japanese (6C)	こんにちわ
Japanese (6D)	さようなら
Italian (6E)	Buongiorno Signore
Italian (6F)	Arrivederla Sibnore

MSM6596A-900 address list (time stamp and demonstration) 1/4

	Address for evaluation	Voice word	M6388 and M6588 start address	M6388 stop address and M6588 upper stop address	M6588 lower stop address	ADPCM length (Bit)	fs (kHz)	Playback time (Seconds)
No. 1	01	ALARM	0	B	71	4	6.4	0.48
No. 2	02	SETTING	C	16	4B	4	6.4	0.42
No. 3	03	ON	17	1E	55	4	6.4	0.31
No. 4	04	OFF	1F	25	67	4	6.4	0.27
No. 5	05	HOUR	26	2E	67	4	6.4	0.35
No. 6	06	MINUTE	2F	37	35	4	6.4	0.34
No. 7	07	SECOND	38	41	0B	4	6.4	0.36
No. 8	08	NINE	42	4D	0D	4	6.4	0.44
No. 9	09	TEN	4E	56	31	4	6.4	0.34
No.10	0A	ELEVEN	57	65	37	4	6.4	0.58
No.11	0B	TWELVE	66	70	47	4	6.4	0.42
No.12	0C	ZERO	71	7F	09	4	6.4	0.56
No.13	0D	TWEN-	80	85	33	4	6.4	0.22
No.14	0E	THIR-	86	8A	57	4	6.4	0.19
No.15	0F	FIF-	8B	90	47	4	6.4	0.22
No.16	10	TY-FOUR	91	A2	0D	4	6.4	0.68
No.17	11	TY-FIVE	A3	B6	47	4	6.4	0.78
No.18	12	TY-SIX	B7	C6	5B	4	6.4	0.63
No.19	13	TY-SEVEN	C7	D6	01	4	6.4	0.60
No.20	14	TY-EIGHT	D7	E6	4B	4	6.4	0.62
No.21	15	TY-NINE	E7	F6	6B	4	6.4	0.63
No.22	16	-TY	F7	FD	2B	4	6.4	0.25
No.23	17	-TEEN	FE	106	3D	4	6.4	0.34
No.24	18	ONE	107	110	39	4	6.4	0.38
No.25	19	TWO	111	118	1B	4	6.4	0.29
No.26	1A	THREE	119	121	01	4	6.4	0.32
No.27	1B	FOUR	122	12B	0D	4	6.4	0.36
No.28	1C	FIVE	12C	135	4B	4	6.4	0.38
No.29	1D	SIX	136	140	2D	4	6.4	0.41
No.30	1E	SEVEN	141	14A	51	4	6.4	0.39
No.31	1F	EIGHT	14B	152	2B	4	6.4	0.29
No.32	20	O'CLOCK	153	163	35	4	6.4	0.66
No.33	21	SIX-	164	16B	73	4	6.4	0.32
No.34	22	SEVEN-	16C	176	05	4	6.4	0.40
No.35	23	EIGHT-	177	17D	2B	4	6.4	0.25
No.36	24	NINE-	17E	186	11	4	6.4	0.33

MSM6596A-900 address list (time stamp and demonstration) 2/4

	Address for evaluation	Voice word	M6388 and M6588 start address	M6388 stop address and M6588 upper stop address	M6588 lower stop address	ADPCM length (Bit)	fs (kHz)	Playback time (Seconds)
No.37	24	TY-ONE	187	196	0F	4	6.4	0.58
No.38	25	TY-TWO	197	1A6	45	4	6.4	0.58
No.39	26	TY-THREE	1A7	1B7	3B	4	6.4	0.58
No.40	27	OH	1B8	1BF	65	4	6.4	0.58
No.41	28	FOR-	1C0	1C6	31	4	6.4	0.58
No.42	2A	TO GO	1C7	1D4	29	4	6.4	0.58
No.43	2B	IT'S	1D5	1DC	11	4	6.4	0.58
No.44	2C	Silence 50 ms	1DD	1DE	1D	4	6.4	0.58
No.45	2D	Silence 200 ms	1DF	1E3	7D	4	6.4	0.58
No.46	2E	AM	1E4	1F2	55	4	6.4	0.58
No.47	2F	PM	1F3	201	73	4	6.4	0.58
No.48	30	午前	202	212	5D	4	6.4	0.58
No.49	31	午後	213	221	31	4	6.4	0.58
No.50	32	メモ	222	22D	27	4	6.4	0.45
No.51	33	れい (Hours)	22E	239	27	4	6.4	0.45
No.52	34	いち (Hours)	23A	244	74	4	6.4	0.44
No.53	35	に (Hours and minutes)	245	24C	33	4	6.4	0.30
No.54	36	さん (Hours)	24D	257	0F	4	6.4	0.40
No.55	37	よ (Hours)	258	25F	01	4	6.4	0.28
No.56	38	ご (Hours)	260	266	4F	4	6.4	0.26
No.57	39	ろく (Hours)	267	271	43	4	6.4	0.42
No.58	3A	なな (Hours)	272	27C	39	4	6.4	0.42
No.59	3B	はち (Hours)	27D	288	27	4	6.4	0.45
No.60	3C	く (Hours)	289	28F	1D	4	6.4	0.25
No.61	3D	じゅう (Hours)	290	29A	57	4	6.4	0.43
No.62	3E	じゅういち (Hours)	29B	2AF	25	4	6.4	0.81
No.63	3F	じゅうに (Hours)	2B0	2BF	15	4	6.4	0.61
No.64	40	時	2C0	2C4	5F	4	6.4	0.19
No.65	41	じゅう	2C5	2D0	21	4	6.4	0.45
No.66	42	にじゅう	2D1	2DF	0D	4	6.4	0.56
No.67	43	さんじゅう	2E0	2F0	27	4	6.4	0.65
No.68	44	よんじゅう	2F1	301	7B	4	6.4	0.68
No.69	45	ごじゅう	302	30F	1F	4	6.4	0.53
No.70	46	いっ (Minutes)	310	319	5F	4	6.4	0.39
No.71	47	さん (Minutes)	31A	323	69	4	6.4	0.39
No.72	48	よん (Minutes)	324	32D	23	4	6.4	0.37
No.73	49	ご (Minutes)	32E	335	79	4	6.4	0.32
No.74	4A	ろっ (Minutes)	336	33F	13	4	6.4	0.37

MSM6596A-900 address list (time stamp and demonstration) 3/4

	Address for evaluation	Voice word	M6388 and M6588 start address	M6388 stop address and M6588 upper stop address	M6588 lower stop address	ADPCM length (Bit)	fs (kHz)	Playback time (Seconds)
No.75	4B	なな (Minutes)	340	34A	3B	4	6.4	0.42
No.76	4C	はっ (Minutes)	34B	354	2D	4	6.4	0.37
No.77	4D	きゅう (Minutes)	355	35D	07	4	6.4	0.32
No.78	4E	じゅっ (Minutes)	35E	368	6F	4	6.4	0.44
No.79	4F	にじゅっ (Minutes)	369	377	19	4	6.4	0.57
No.80	50	さんじゅっ (Minutes)	378	388	77	4	6.4	0.68
No.81	51	よんじゅっ (Minutes)	389	39A	37	4	6.4	0.70
No.82	52	ごじゅっ (Minutes)	39B	3A8	53	4	6.4	0.55
No.83	53	ぜろ	3A9	3B3	11	4	6.4	0.41
No.84	54	ふん	3B4	3BC	33	4	6.4	0.34
No.85	55	ぷん	3BD	3C5	4D	4	6.4	0.34
No.86	56	件	3C6	3CF	31	4	6.4	0.38
No.87	57	です	3D0	3D4	37	4	6.4	0.18
No.88	58	月	3D5	3DF	35	4	6.4	0.42
No.89	59	火	3E0	3E5	3D	4	6.4	0.22
No.90	5A	水	3E6	3EE	25	4	6.4	0.33
No.91	5B	木	3EF	3F8	7D	4	6.4	0.40
No.92	5C	金	3F9	402	1B	4	6.4	0.37
No.93	5D	土	403	409	17	4	6.4	0.25
No.94	5E	日	40A	414	73	4	6.4	0.44
No.95	5F	曜日	415	421	4D	4	6.4	0.50
No.96	60	Greetings (Chinese)	422	434	71	4	8.0	0.60
No.97	61	〃	435	448	41	4	8.0	0.62
No.98	62	Greetings (English)	449	45A	59	4	8.0	0.57
No.99	63	〃	45B	46E	05	4	8.0	0.61
No.100	64	Greetings (German)	46F	487	05	4	8.0	0.77
No.101	65	〃	488	4A1	59	4	8.0	0.82
No.102	66	Greetings (French)	4A2	4BC	73	4	8.0	0.86
No.103	67	〃	4BD	4D5	3F	4	8.0	0.78
No.104	68	Greetings (Spanish)	4D6	4ED	5D	4	8.0	0.76
No.105	69	〃	4EE	5FB	77	4	8.0	0.45
No.106	6A	Greetings (Korean)	4FC	522	58	4	8.0	1.24
No.107	6B	〃	523	549	17	4	8.0	1.22
No.108	6C	Greetings (Japanese)	54A	55E	4F	4	8.0	0.66
No.109	6D	〃	55F	576	3F	4	8.0	0.75
No.110	6E	Greetings (Italian)	577	5A1	27	4	8.0	1.35
No.111	6F	〃	5A2	5D8	4B	4	8.0	1.75

MSM6596A-900 address list (time stamp and demonstration) 4/4

	Address for evaluation	Voice word	M6388 and M6588 start address	M6388 stop address and M6588 upper stop address	M6588 lower stop address	ADPCM length (Bit)	fs (kHz)	Playback time (Seconds)
No.112	70	Japanese greetings (3 bits)	5D9	5EF	49	4	8.0	0.95
No.113	71	Japanese greetings (4 bits)	5F0	60D	65	4	8.0	0.95
No.114	72	English greetings (3 bits)	60E	61F	15	4	8.0	0.73
No.115	73	English greetings (4 bits)	620	636	5F	4	8.0	0.73
No.116	74	Effect sound - 1	637	660	29	4	8.0	1.32
No.117	75	Effect sound - 2	661	68A	7F	4	8.0	1.34
No.118	76	Effect sound - 3	68B	6EB	29	4	8.0	3.08
No.119	77	Barking of dog	6EC	709	7D	4	8.0	0.96
No.120	78	Roar of lion	70A	789	27	4	8.0	4.07
No.121	79	Lowing of cattle	78A	7E1	43	4	8.0	2.80

MSM6597A-750 address list (For general-purpose application) 1/5

(1) M6388, M6588 start address
(2) M6388 stop address
M6588 upper stop address
(3) M6588 lower stop address

Address	Voice word		(1)	(2)	(3)	Playback [s]	Frequency [kHz]	ADPCM bit length
00	—		—	—	—	—	—	—
01	午前		0	10	5D	0.67	6.4	4
02	午後		11	1F	31	0.58	6.4	4
03	メモ		20	2B	27	0.45	6.4	4
04	れい	(Hours)	2C	37	27	0.45	6.4	4
05	いち	(Hours)	38	42	74	0.44	6.4	4
06	に	(Hours and minues)	43	4A	33	0.30	6.4	4
07	さん	(Hours)	4B	55	0F	0.40	6.4	4
08	よ	(Hours)	56	5D	01	0.28	6.4	4
09	ご	(Hours)	5E	64	4F	0.26	6.4	4
0A	ろく	(Hours)	65	6F	43	0.42	6.4	4
0B	なな	(Hours)	70	7A	39	0.42	6.4	4
0C	はち	(Hours)	7B	86	27	0.45	6.4	4
0D	く	(Hours)	87	8D	1D	0.25	6.4	4
0E	じゅう	(Hours)	8E	98	57	0.43	6.4	4
0F	じゅういち	(Hours)	99	AD	25	0.81	6.4	4
10	じゅうに	(Hours)	AE	BD	15	0.61	6.4	4
11	時		BE	C2	5F	0.19	6.4	4
12	じゅう		C3	CE	21	0.45	6.4	4
13	にじゅう		CF	DD	0D	0.56	6.4	4
14	さんじゅう		DE	EE	27	0.65	6.4	4
15	よんじゅう		EF	FF	7B	0.68	6.4	4
16	ごじゅう		100	10D	1F	0.53	6.4	4
17	いっ	(Minutes)	10E	117	5F	0.39	6.4	4
18	さん	(Minutes)	118	121	69	0.39	6.4	4
19	よん	(Minutes)	122	12B	23	0.37	6.4	4
1A	ご	(Minutes)	12C	133	79	0.32	6.4	4
1B	ろっ	(Minutes)	134	13D	13	0.37	6.4	4
1C	なな	(Minutes)	13E	148	3B	0.42	6.4	4
1D	はっ	(Minutes)	149	152	2D	0.37	6.4	4
1E	きゅう	(Minutes)	153	15B	07	0.32	6.4	4
1F	じゅっ	(Minutes)	15C	166	6F	0.44	6.4	4

MSM6597A-750 address list (For general-purpose application) 2/5

(1) M6388, M6588 start address
(2) M6388 stop address
M6588 upper stop address
(3) M6588 lower stop address

Address	Voice word	(1)	(2)	(3)	Playback [s]	Frequency [kHz]	ADPCM bit length
20	にじゅっ (Minues)	167	175	19	0.57	6.4	4
21	さんじゅっ (Minues)	176	186	77	0.68	6.4	4
22	よんじゅっ (Minues)	187	198	37	0.70	6.4	4
23	ごじゅっ (Minues)	199	1A6	53	0.55	6.4	4
24	ぜろ	1A7	1B1	11	0.41	6.4	4
25	ふん	1B2	1BA	33	0.34	6.4	4
26	ぷん	1BB	1C3	4D	0.34	6.4	4
27	件	1C4	1CD	31	0.38	6.4	4
28	です	1CE	1D2	37	0.18	6.4	4
29	Message + music (Japanese)	1D3	216	5F	4.34	4.0	4
2A	Message + music (Japanese)	217	277	35	4.66	5.3	4
2B	Message + music (Japanese)	278	2EE	47	4.74	6.4	4
2C	Message + music (Japanese)	2EF	377	47	4.37	8.0	4
2D	Message + cattle voice (Japanese)	378	3B0	13	3.59	4.0	4
2E	Message + cattle voice (Japanese)	3B1	405	19	4.07	5.3	4
2F	Message + cattle voice (Japanese)	406	464	6D	3.79	6.4	4
30	Message + cattle voice (Japanese)	465	4D0	6F	3.45	8.0	4
31	Message + music (English)	4D1	510	49	4.07	4.0	4
32	Message + music (English)	511	571	5D	4.67	5.3	4
33	Message + music (English)	572	5E8	15	4.73	6.4	4
34	Message + music (English)	5E9	663	5B	3.93	8.0	4
35	Message + cattle voice (English)	664	6A5	11	4.17	4.0	4
36	Message + cattle voice (English)	6A6	707	7D	4.73	5.3	4
37	Message + cattle voice (English)	708	77A	45	4.58	6.4	4
38	Message + cattle voice (English)	77B	7F3	25	3.85	8.0	4
39	ALARM	7F4	7FF	71	0.48	6.4	4
3A	SETTING	800	80A	4B	0.42	6.4	4
3B	ONE	80B	814	39	0.38	6.4	4
3C	TWO	815	81C	1B	0.29	6.4	4
3D	THREE	81D	825	01	0.32	6.4	4
3E	FOUR	826	82F	0D	0.36	6.4	4
3F	FIVE	830	839	4B	0.38	6.4	4

MSM6597A-750 address list (For general-purpose application) 3/5

(1) M6388, M6588 start address
(2) M6388 stop address
M6588 upper stop address
(3) M6588 lower stop address

Address	Voice word	(1)	(2)	(3)	Playback [s]	Frequency [kHz]	ADPCM bit length
40	SIX	83A	844	2D	0.41	6.4	4
41	SEVEN	845	84E	51	0.39	6.4	4
42	EIGHT	84F	856	2B	0.29	6.4	4
43	NINE	857	862	0D	0.44	6.4	4
44	TEN	863	86B	31	0.34	6.4	4
45	ELEVEN	86C	87A	37	0.58	6.4	4
46	TWELVE	87B	885	47	0.42	6.4	4
47	ZERO	886	894	09	0.56	6.4	4
48	TWEN-	895	89A	33	0.22	6.4	4
49	THIR-	89B	89F	57	0.19	6.4	4
4A	FOR-	8A0	8A6	31	0.26	6.4	4
4B	FIF-	8A7	8AC	47	0.22	6.4	4
4C	TY-ONE	8AD	8BC	0F	0.60	6.4	4
4D	TY-TWO	8BD	8CC	45	0.62	6.4	4
4E	TY-THREE	8CD	8DD	3B	0.66	6.4	4
4F	TY-FOUR	8DE	8EF	0D	0.68	6.4	4
50	TY-FIVE	8F0	903	47	0.78	6.4	4
51	TY-SIX	904	913	5B	0.63	6.4	4
52	TY-SEVEN	914	923	01	0.60	6.4	4
53	TY-EIGHT	924	933	4B	0.62	6.4	4
54	TY-NINE	934	943	6B	0.63	6.4	4
55	-TEEN	944	94C	3D	0.34	6.4	4
56	-TY	94D	953	2B	0.25	6.4	4
57	SIX-	954	95B	73	0.32	6.4	4
58	SEVEN-	95C	966	05	0.40	6.4	4
59	EIGHT-	967	96D	2B	0.25	6.4	4
5A	NINE-	96E	976	11	0.33	6.4	4
5B	OH	977	97E	65	0.31	6.4	4
5C	IT'S	97F	986	11	0.29	6.4	4
5D	Silence (50 ms)	987	988	1D	0.05	6.4	4
5E	Silence (200 ms)	989	98D	7D	0.20	6.4	4
5F	AM	98E	99C	55	0.59	6.4	4

MSM6597A-750 address list (For general-purpose application) 4/5

(1) M6388, M6588 start address
(2) M6388 stop address
M6588 upper stop address
(3) M6588 lower stop address

Address	Voice word	(1)	(2)	(3)	Playback [s]	Frequency [kHz]	ADPCM bit length
60	PM	99D	9AB	73	0.60	6.4	4
61	ALARM	9AC	9B4	A1	0.48	6.4	3
62	SETTING	9B5	9BC	A5	0.42	6.4	3
63	ONE	9BD	9C4	13	0.38	6.4	3
64	TWO	9C5	9CA	49	0.29	6.4	3
65	THREE	9CB	9D1	05	0.32	6.4	3
66	FOUR	9D2	9D8	91	0.36	6.4	3
67	FIVE	9D9	9E0	25	0.38	6.4	3
68	SIX	9E1	9E8	87	0.41	6.4	3
69	SEVEN	9E9	9F0	2B	0.39	6.4	3
6A	EIGHT	9F1	9F6	59	0.29	6.4	3
6B	NINE	9F7	9FF	3D	0.44	6.4	3
6C	TEN	A00	A06	35	0.34	6.4	3
6D	ELEVEN	A07	A11	93	0.58	6.4	3
6E	TWELVE	A12	A19	A1	0.42	6.4	3
6F	ZERO	A1A	A24	65	0.56	6.4	3
70	TWIN-	A25	A29	0B	0.22	6.4	3
71	THIR-	A2A	A2D	59	0.19	6.4	3
72	FOR-	A2E	A32	89	0.26	6.4	3
73	FIF-	A33	A37	1F	0.22	6.4	3
74	TY-ONE	A38	A43	41	0.60	6.4	3
75	TY-TWO	A44	A4F	77	0.62	6.4	3
76	TY-THREE	A50	A5C	43	0.66	6.4	3
77	TY-FOUR	A5D	A69	95	0.68	6.4	3
78	TY-FIVE	A6A	A78	7B	0.78	6.4	3
79	TY-SIX	A79	A84	8D	0.63	6.4	3
7A	TY-SEVEN	A85	A90	33	0.60	6.4	3
7B	TY-EIGHT	A91	A9C	7D	0.62	6.4	3
7C	TY-NINE	A9D	AA8	9D	0.63	6.4	3
7D	-TEEN	AA9	AAF	41	0.34	6.4	3
7E	-TY	AB0	AB4	83	0.25	6.4	3
7F	SIX-	AB5	ABA	A1	0.32	6.4	3

MSM6597A-750 address list (For general-purpose application) 5/5

(1) M6388, M6588 start address
(2) M6388 stop address
M6588 upper stop address
(3) M6588 lower stop address

Address	Voice word	(1)	(2)	(3)	Playback [s]	Frequency [kHz]	ADPCM bit length
80	SEVEN-	ABB	AC2	5F	0.40	6.4	3
81	EIGHT-	AC3	AC7	83	0.25	6.4	3
82	NINE-	AC8	ACE	15	0.33	6.4	3
83	OH	ACF	AD4	93	0.31	6.4	3
84	IT'S	AD5	ADA	3F	0.29	6.4	3
85	Silence (50 ms)	ADB	ADB	9D	0.05	6.4	3
86	Silence (200 ms)	ADC	ADF	7F	0.20	6.4	3
87	AM	AE0	AEB	07	0.59	6.4	3
88	PM	AEC	AF7	25	0.60	6.4	3

MSM9800 Series General-Purpose ROM Codes

MSM9802-200 Edit ROM Address Corresponding List (for Demonstration)

Address	Voice Word
00	—
01	<Sound of a bell> (straight PCM, 8 kHz)
02	<Sound of a bell> (nonlinear PCM, 8 kHz)
03	<Birdcall> (straight PCM, 8 kHz)
04	<Birdcall> (nonlinear PCM, 8 kHz)
05	<Sound of a bell> (straight PCM, 8 kHz), <Sound of a bell> (nonlinear PCM, 8 kHz)
06	<Birdcall> (straight PCM, 8 kHz), <Birdcall> (nonlinear PCM, 8 kHz)
07	<Sound of a bell> (straight PCM, 8 kHz), <Sound of a bell> (nonlinear PCM, 8 kHz), <Birdcall> (straight PCM,8 kHz), <Birdcall> (nonlinear PCM, 8 kHz)

MSM9802-201 Voice Word Address Corresponding List (for Demonstration)

Y Address	Voice Word	Playback Method	Frequency[kHz]
00	—	—	—
01	Sound of a high-hat close	Nonlinear	16.0
02	Sound of a high-hat close	Nonlinear	12.8
03	Sound of a high-hat close	Nonlinear	10.6
04	Sound of a high-hat close	Nonlinear	8.0
05	Sound of a high-hat close	Nonlinear	6.4
06	Sound of a high-hat close	Nonlinear	5.3
07	Sound of a high-hat close	Nonlinear	4.0
08	Sound of a bass drum	Nonlinear	16.0
09	Sound of a bass drum	Nonlinear	12.8
0A	Sound of a bass drum	Nonlinear	10.6
0B	Sound of a bass drum	Nonlinear	8.0
0C	Sound of a bass drum	Nonlinear	6.4
0D	Sound of a bass drum	Nonlinear	5.3
0E	Sound of a bass drum	Nonlinear	4.0
0F	"Hello" (female voice)	Nonlinear	8.0
10	"Hello" (female voice)	Nonlinear	6.4
11	"Hello" (female voice)	Nonlinear	5.3
12	"Hello" (female voice)	Nonlinear	4.0
13	"今日の天気は晴れです" (female voice)	Nonlinear	8.0
14	"今日の天気は晴れです" (female voice)	Nonlinear	6.4
15	"今日の天気は晴れです" (female voice)	Nonlinear	5.3
16	"今日の天気は晴れです" (female voice)	Nonlinear	4.0

MSM9802-201 Edit ROM Address Corresponding List (for Demonstration)

X Address	Voice Word
00	—
01	"今日の天気は晴れです (4.0kHz)"
02	"今日の天気は晴れです (5.3kHz)"
03	"今日の天気は晴れです (6.4kHz)"
04	"今日の天気は晴れです (8.0kHz)"
05	"今日の天気は晴れです (4.0kHz) silence (512ms) Hello (4.0kHz)"
06	"今日の天気は晴れです (5.3kHz) silence(512ms) Hello (5.3kHz)"
07	"今日の天気は晴れです (4.0kHz) silence (128ms) 今日の天気は晴れです (5.3kHz) silence (128ms) 今日の天気は晴れです (6.4kHz) silence (128ms) 今日の天気は晴れです (8.0kHz) silence (128ms)"
08	"今日の天気は晴れです (4.0kHz) 今日の天気は晴れです (5.3kHz) 今日の天気は晴れです (6.4kHz) 今日の天気は晴れです (8.0kHz) Hello (4.0kHz) Hello (5.3kHz) Hello (6.4kHz) Hello (8.0kHz)"
09	"Hello (4.0kHz)"
0A	"Hello (5.3kHz)"
0B	"Hello (6.4kHz)"
0C	"Hello (8.0kHz)"
0D	"今日の天気は晴れです (6.4kHz) silence (512ms) Hello (6.4kHz)"
0E	"今日の天気は晴れです (8.0kHz) silence (512ms) Hello (8.0kHz)"
0F	"Hello (4.0kHz) silence (128ms) Hello (5.3kHz) silence (128ms) Hello (6.4kHz) silence (128ms) Hello (8.0kHz) silence (128ms)"
10	"Sound of a high-hat close (8.0kHz) silence (128ms)" (4 times)
11	"Sound of a high-hat close (4.0kHz) silence (256ms)"
12	"Sound of a high-hat close (5.3kHz) silence (256ms)"
13	"Sound of a high-hat close (6.4kHz) silence (256ms)"
14	"Sound of a high-hat close (8.0kHz) silence (256ms)"
15	"Sound of a bass drum (4.0kHz) silence (288ms) Sound of a high-hat close (4.0kHz) silence (256ms)"
16	"Sound of a bass drum (5.3kHz) silence (288ms) Sound of a high-hat close (5.3kHz) silence (256ms)"
17	"Sound of a high-hat close (4.0kHz) silence (128ms) Sound of a high-hat close (5.3kHz) silence (128ms) Sound of a high-hat close (6.4kHz) silence (128ms) Sound of a high-hat close (8.0kHz) silence (128ms)"
18	"Sound of a bass drum (8.0kHz) silence128ms" Sound of a high-hat close (8.0kHz) silence128ms)" (2 times)
19	"Sound of a bass drum (4.0kHz) silence (256ms)"
1A	"Sound of a bass drum (5.3kHz) silence (256ms)"
1B	"Sound of a bass drum (6.4kHz) silence (256ms)"
1C	"Sound of a bass drum (8.0kHz) silence (256ms)"
1D	"Sound of a bass drum (6.4kHz) silence (288ms) Sound of a high-hat close (6.4kHz) silence (256ms)"
1E	"Sound of a bass drum (8.0kHz) silence (288ms) Sound of a high-hat close (8.0kHz) silence (256ms)"
1F	"Sound of a bass drum (4.0kHz) silence (128ms) Sound of a bass drum (5.3kHz) silence (128ms) Sound of a bass drum (6.4kHz) silence (128ms) Sound of a bass drum (8.0kHz) silence (128ms)"

MSM9802-201 Edit ROM Address Corresponding List (for Demonstration) (Continued)

X Address	Voice Word
20	"Sound of a high-hat close (16.0kHz) silence (128ms)" (4 times)
21	"Sound of a high-hat close (4.0kHz) silence (256ms)"
22	"Sound of a high-hat close (5.3kHz) silence (256ms)"
23	"Sound of a high-hat close (6.4kHz) silence (256ms)"
24	"Sound of a high-hat close (8.0kHz) silence (256ms)"
25	"Sound of a high-hat close (10.6kHz) silence (256ms)"
26	"Sound of a high-hat close (12.8kHz) silence (256ms)"
27	"Sound of a high-hat close (16.0kHz) silence (256ms)"
28	"Sound of a bass drum (16.0kHz) silence (128ms)" (4 times)
29	"Sound of a bass drum (4.0kHz) silence (128ms)"
2A	"Sound of a bass drum (5.3kHz) silence (128ms)"
2B	"Sound of a bass drum (6.4kHz) silence (128ms)"
2C	"Sound of a bass drum (8.0kHz) silence (128ms)"
2D	"Sound of a bass drum (10.6kHz) silence (128ms)"
2E	"Sound of a bass drum (12.8kHz) silence (128ms)"
2F	"Sound of a bass drum (16.0kHz) silence (128ms)"
30	"Sound of a bass drum (16.0kHz) silence (288ms) Sound of a high-hat close (16.0kHz) silence (256ms) Sound of a high-hat close (16.0kHz) silence (256ms) Sound of a high-hat close (16.0kHz) silence (256ms)"
31	"Sound of a bass drum (4.0kHz) silence (288ms) Sound of a high-hat close (4.0kHz) silence (256ms)" (2 times)
32	"Sound of a bass drum (5.3kHz) silence (288ms) Sound of a high-hat close(5.3kHz) silence (256ms)" (2 times)
33	"Sound of a bass drum (6.4kHz) silence (288ms) Sound of a high-hat close (6.4kHz) silence (256ms)" (2 times)
34	"Sound of a bass drum (8.0kHz) silence (288ms) Sound of a high-hat close (8.0kHz) silence (256ms)" (2 times)
35	"Sound of a bass drum (10.6kHz) silence (288ms) Sound of a high-hat close (10.6kHz) silence (256ms)" (2 times)
36	"Sound of a bass drum (12.8kHz) silence (288ms) Sound of a high-hat close (12.8kHz) silence (256ms)" (2 times)
37	"Sound of a bass drum (16.0kHz) silence (288ms) Sound of a high-hat close (16.0kHz) silence (256ms)" (2 times)
38	"Sound of a bass drum (16.0kHz) silence (288ms) Sound of a bass drum (16.0kHz) silence (288ms) Sound of a bass drum (16.0kHz) silence (288ms) Sound of a high-hat close (16.0kHz) silence (256ms)"
39	"Sound of a bass drum (4.0kHz) silence (160ms) Sound of a bass drum (4.0kHz) silence (160ms) Sound of a high-hat close (4.0kHz) silence (384ms)"
3A	"Sound of a bass drum (5.3kHz) silence (160ms) Sound of a bass drum (5.3kHz) silence (160ms) Sound of a high-hat close (5.3kHz) silence (384ms)"
3B	"Sound of a bass drum (6.4kHz) silence (160ms) Sound of a bass drum (6.4kHz) silence (160ms) Sound of a high-hat close(6.4kHz) silence (384ms)"
3C	"Sound of a bass drum (8.0kHz) silence (160ms) Sound of a bass drum (8.0kHz) silence (160ms) Sound of a high-hat close (8.0kHz) silence (384ms)"
3D	"Sound of a bass drum (10.6kHz) silence (160ms) Sound of a bass drum(10.6kHz) silence (160ms) Sound of a high-hat close (10.6kHz) silence (384ms)"
3E	"Sound of a bass drum (12.8kHz) silence (160ms) Sound of a bass drum (12.8kHz) silence (160ms) Sound of a high-hat close (12.8kHz) silence (384ms)"
3E	"Sound of a bass drum (16.0kHz) silence (160ms) Sound of a bass drum (16.0kHz) silence (160ms) Sound of a high-hat close (16.0kHz) silence (384ms)"

DEVELOPMENT SUPPORT TOOLS

9

OKI Semiconductor

AR76-202

Voice Analysis and Editing Tool

GENERAL DESCRIPTION

This voice analysis and editing tool is operated on IBM/AT. It is provided with an English editor, and DOS/V that can accommodate Japanese requirements.

OKI Semiconductor

AR203

Voice Analysis and Editing Tool

GENERAL DESCRIPTION

This voice analysis and editing tool is used to translate voice into ADPCM codes to create a ROM for OKI's voice IC.

FEATURES

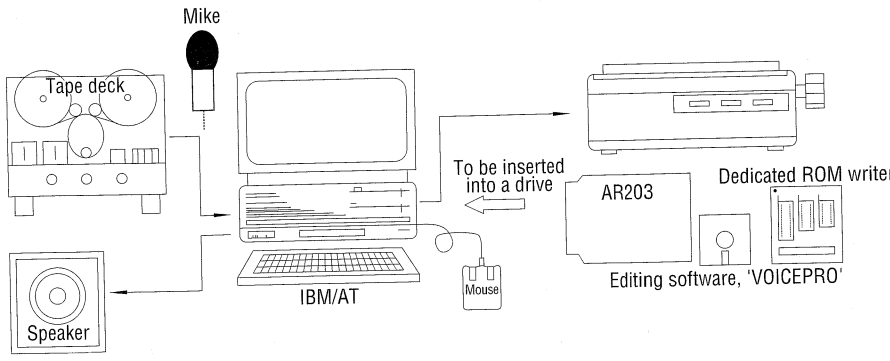
The voice analysis and editing tool is composed of a voice analysis and editing board, "AR203", with a dedicated ROM writer, and editing software, "VOICEPRO". When the board is used, it is to be inserted into a drive slot of IBM/AT.
The editing software enables analysis and editing by mouse operation as you watch displayed voice waveforms. Thus, even the beginner can readily use highly advanced technique to analyze and edit voice.

VOICE SYNTHESIS ICs

MSM6375 family (MSM6372, MSM6373, MSM6374, MSM6375, MSM6376, MSM63P74)
MSM6295
MSM6258
MSM5205
MSM6585
MSM6378A, MSM6379
MSM6388, MSM6588, MSM6688 (MSM6595, MSM6596, MSM6597)
MSM6650 family (MSM6650, MSM6652, MSM6653, MSM6654, MSM6655, MSM6656, MSM66P54*)

COMPONENTS OF VOICE ANALYSIS SYSTEM

Host computer	:	IBM/AT, or DOS/V
Color display	:	640 × 400 dots
Printer	:	Printer for IBM/AT
Mouse	:	Mouse for IBM/AT
Tape deck	:	To attain high-quality sound, it is recommended that an open reel tape deck or DAT be used.
Speaker	:	8 Ω and input of 2 or more watts
Voice analysis and editing tool	:	Voice analysis and editing board, AR203 (including a ROM writer), and editing software, VOICEPRO
* Option	:	P54 adapter. Required when writing to the MSM66P54 with the attached ROM writer. The other devices incorporating OTP (MSM6378A, MSM6379 and MSM63P74) can be loaded without the adapter.



DISPLAY SCREEN

"VOICEPRO" displays waveforms of voice to be played back and edited. The waveform display screens are composed roughly of an editing screen and a monitor screen. Each screen is provided with an overall screen for displaying a whole recorded waveform, and with a time scale for displaying the time since the start of recording a waveform. The amplitude and temporal axis can be changed at your disposal.

COMMANDS

Record

Converts original sound into PCM and stores the resulting sound into the memory. The sampling frequency can be selected in the range of 4 kHz to 48 kHz in the 0.1 kHz step. The maxi-mum recording time depends on the main memory or EMS allocation, being expressed coarsely by:

Maximum recording time (seconds) = size of allocation (bytes) /9/4 x fs (Hz)

Play

Tests and evaluates PCM or ADPCM sound.

Processing

Amplitude control	:	Expands or reduces a voice level.
Silent	:	Makes unnecessary part of voice and noise silent.
Insert silence	:	Inserts silence between units of voice.
Store a part of data	:	Specifies the range of voice data for paste onto another location, and stores it into the buffer memory.
Cut	:	Cuts unnecessary part of voice or the interval between units of voice. The cut contents are stored into the buffer memory. Using this function along with the "Paste" function enables waveforms to be moved.
Paste	:	Copies the contents of the buffer memory stored by "Store a part of data" and "Cut" to the specified position.
Fade	:	Smoothes abrupt changes in voice data.
Mixing	:	Adds contents of the buffer memory to voice data at the specified position.

Pitch change : Changes a voice pitch to implement effects similar to rapid and slow tape feeds.

Insert sine wave : Inserts a sine wave of an arbitrary frequency, size and length into any position of voice data.

Save
Writes edited voice data to a disk.

Load
Reads voice data to be edited from a disk.

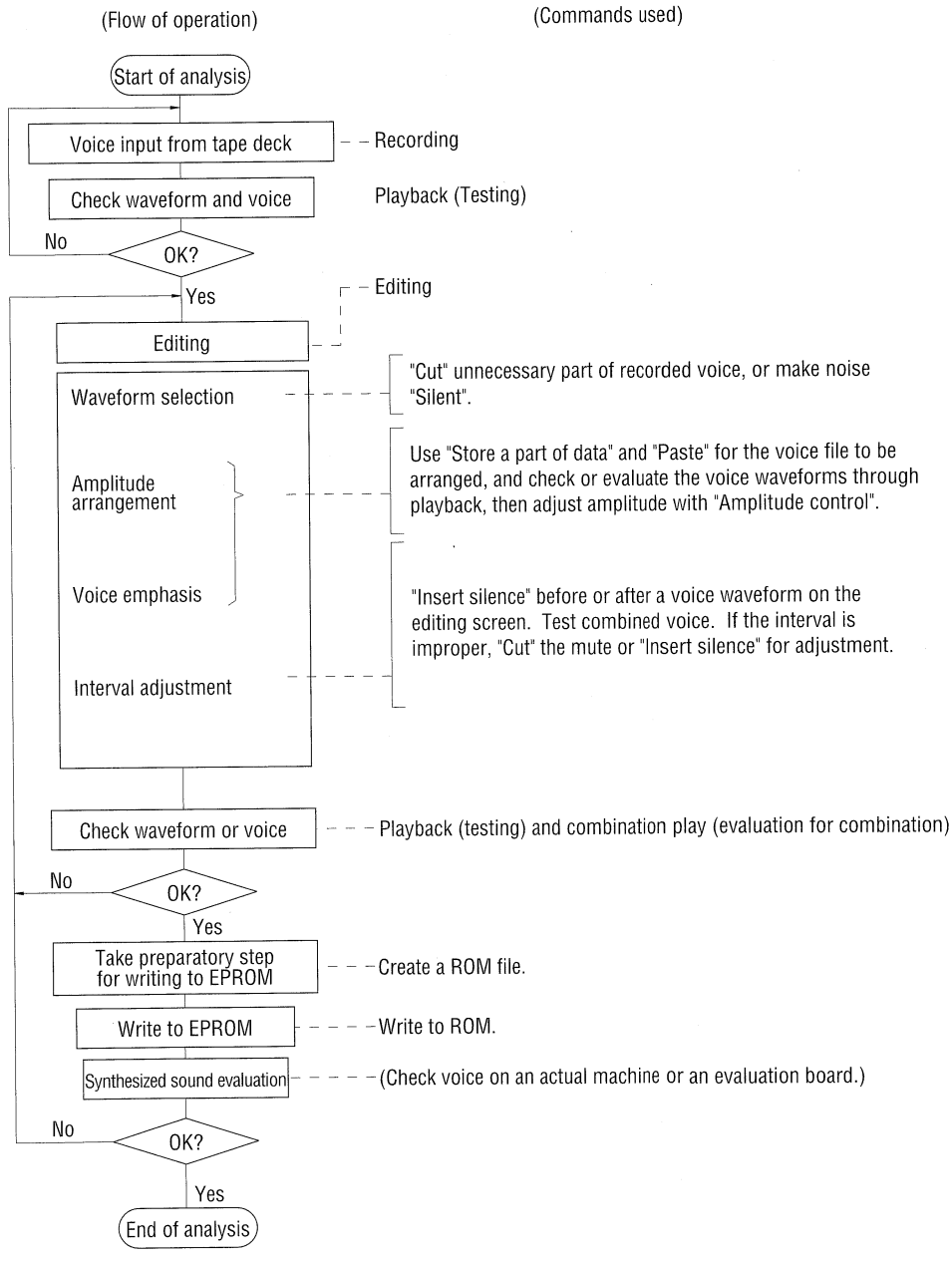
Combination Play
Combines two or more pieces of voice data to compare and evaluate voice continuation.

Melody Creation
Creates melody data based on input through staff notation. This function corresponds to the melody function supported by the MSM6650 family.
Up to triple chords can be created.

ROM File Creation
Converts an edited voice data file into the Intel HEX format and write the data to a disk.

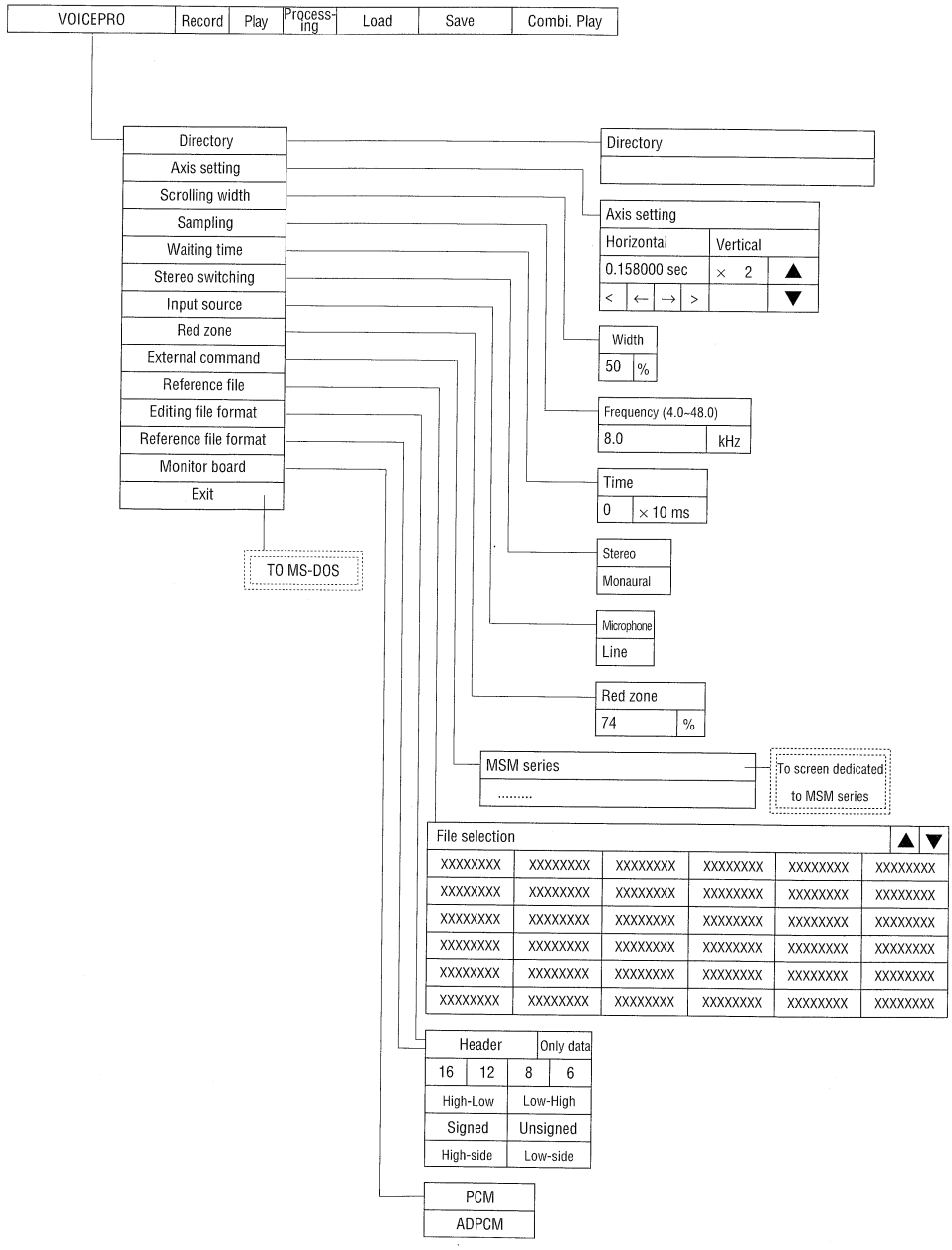
ROM Loading
Writes the voice data that has been converted into the Intel HEX format to PROM, MSM6378A, MSM6379, MSM63P74 or MSM66P54 the attached ROM writer.

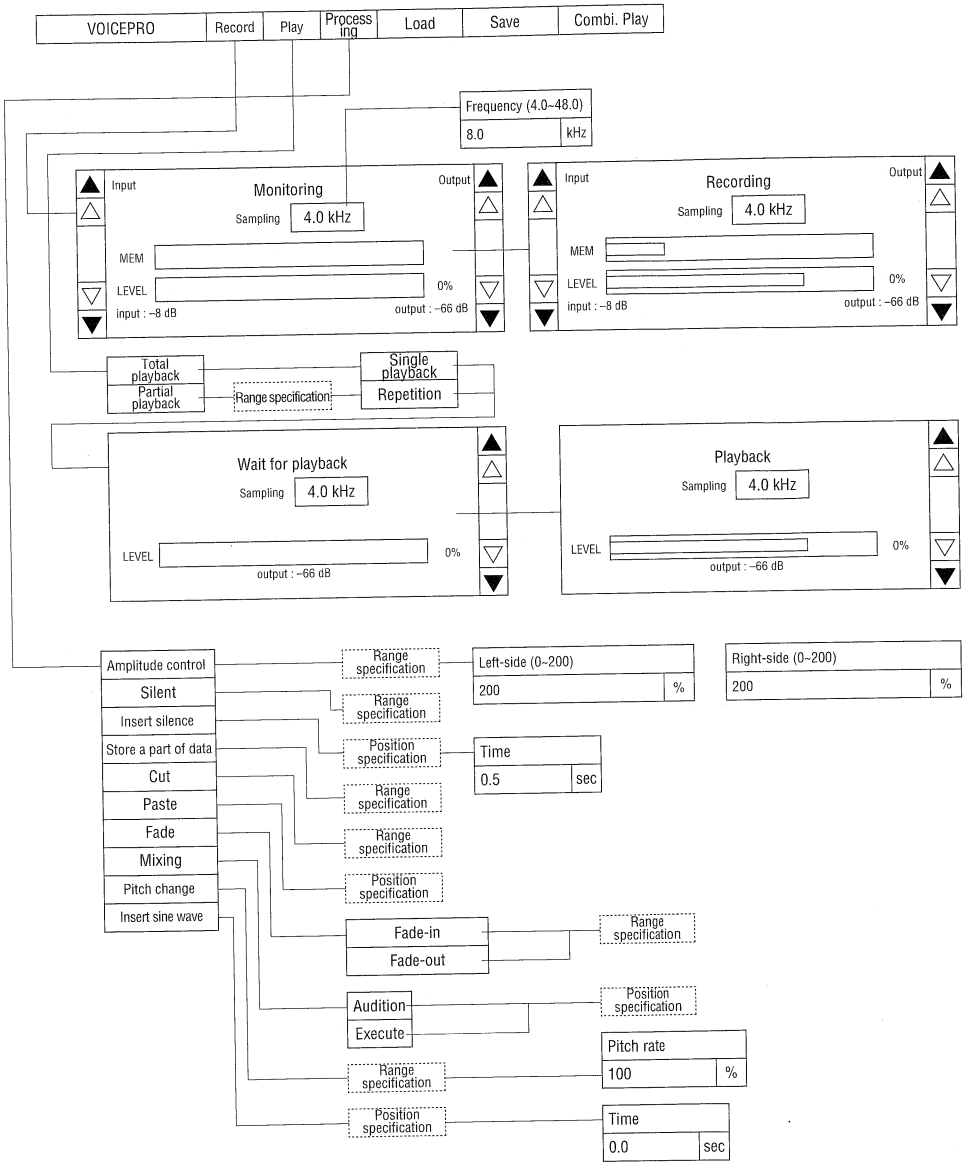
Typical flow of operation by VOICEPRO



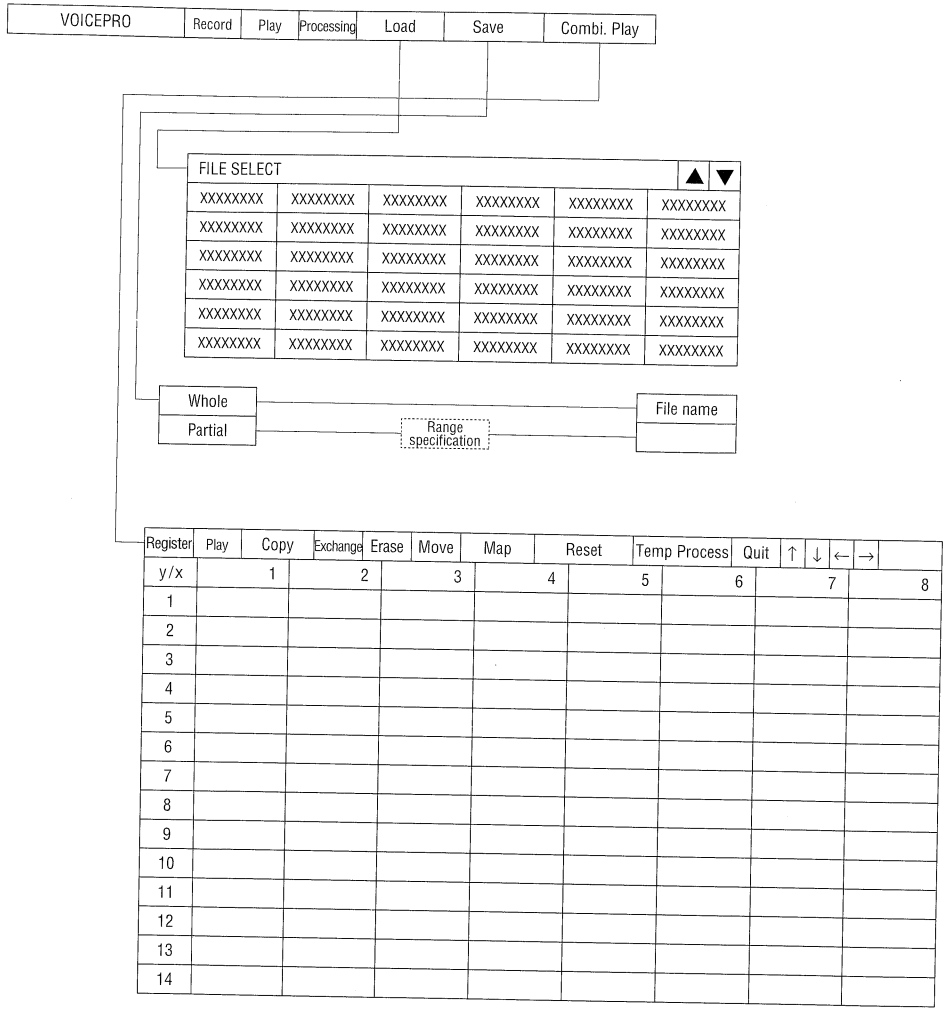
9

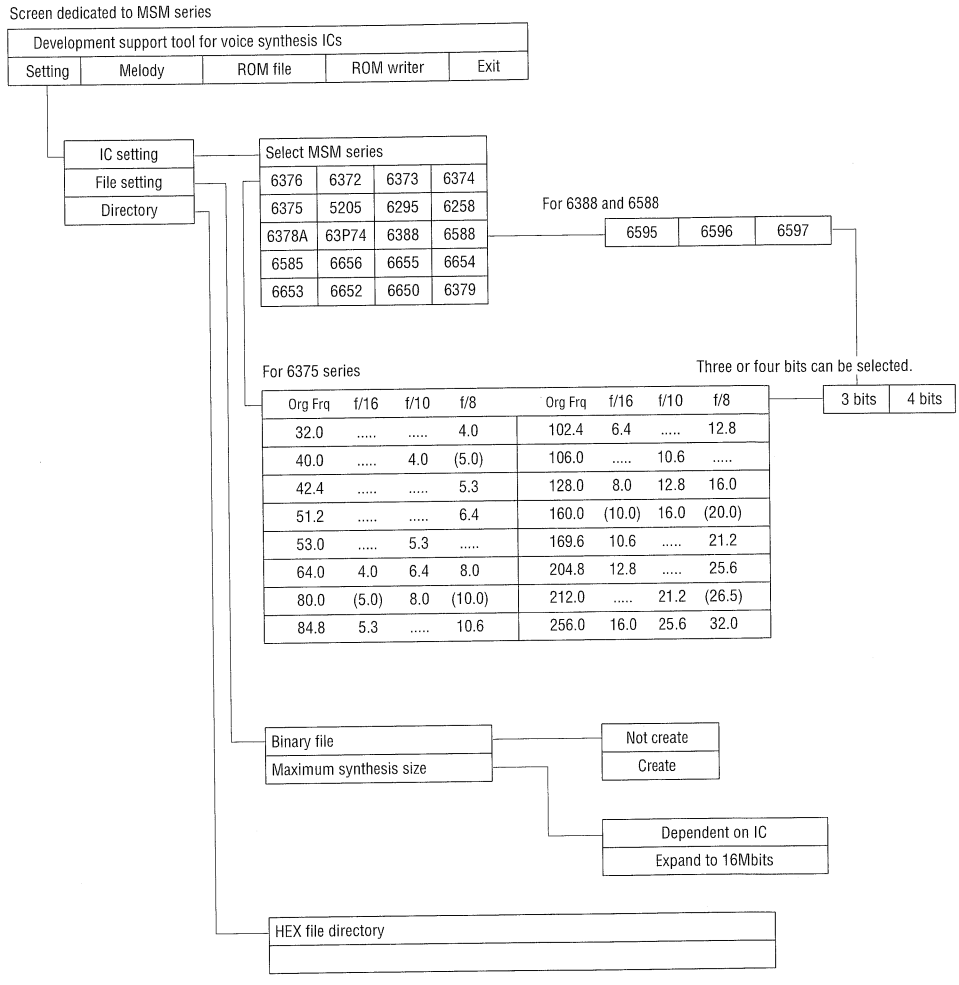
VOICEPRO menu configuration



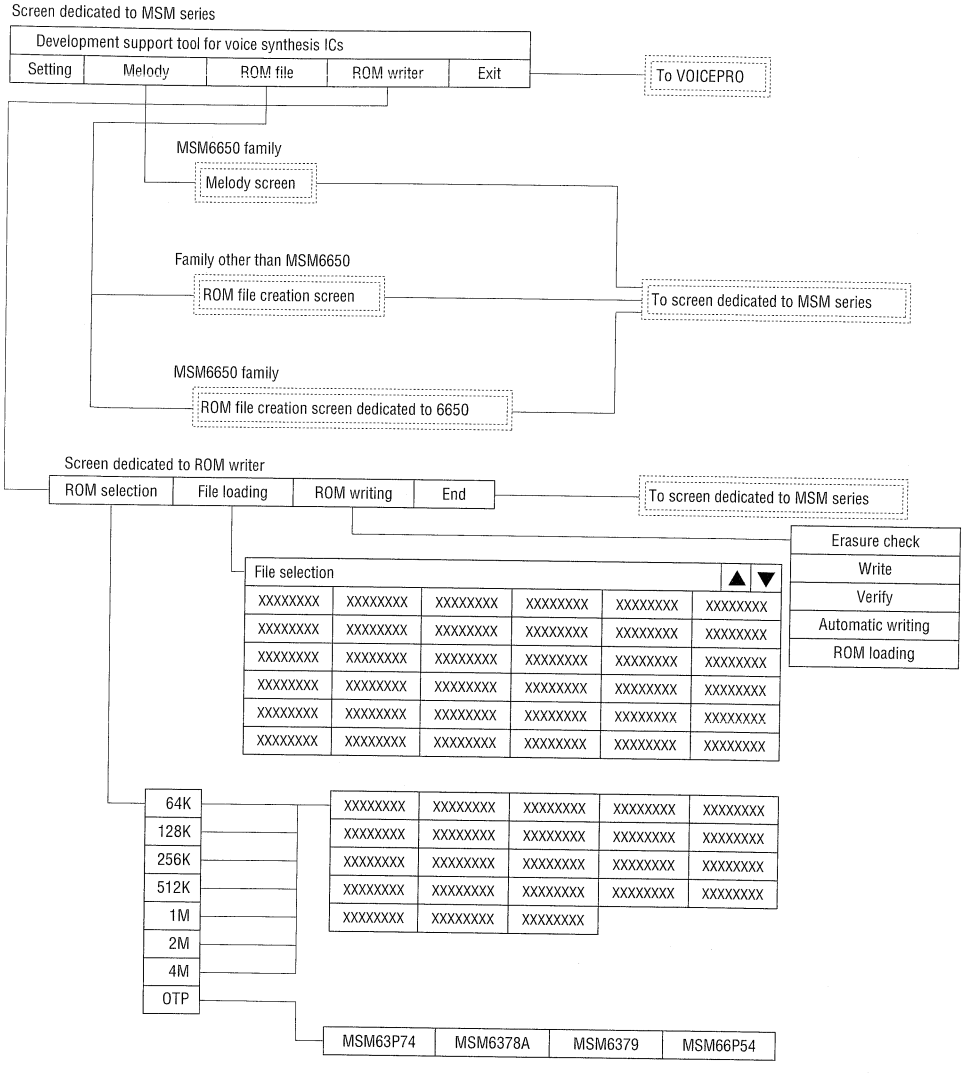

VOICEPRO
Record
Play
Processing
Load
Save
Combi. Play
Frequency (4.0~48.0)
8.0
kHz
Input
Monitoring
Output
Sampling
4.0 kHz
MEM
LEVEL
0%
input : –8 dB
output : –66 dB
Input
Recording
Output
Sampling
4.0 kHz
MEM
LEVEL
0%
input : –8 dB
output : –66 dB
Total playback
Partial playback
Range specification
Single playback
Repetition
Wait for playback
Sampling
4.0 kHz
LEVEL
0%
output : –66 dB
Playback
Sampling
4.0 kHz
LEVEL
0%
output : –66 dB
Amplitude control
Silent
Insert silence
Store a part of data
Cut
Paste
Fade
Mixing
Pitch change
Insert sine wave
Range specification
Left-side (0~200)
200
%
Right-side (0~200)
200
%
Position specification
Time
0.5
sec
Fade-in
Fade-out
Audition
Execute
Pitch rate
100
%
Time
0.0
sec

9


VOICEPRO
Record
Play
Processing
Load
Save
Combi. Play
FILE SELECT
XXXXXXXX
Whole
Partial
Range specification
File name
Register
Play
Copy
Exchange
Erase
Move
Map
Reset
Temp Process
Quit
y/x
1
2
3
4
5
6
7
8
9
10
11
12
13
14


Screen dedicated to MSM series
Development support tool for voice synthesis ICs
Setting
Melody
ROM file
ROM writer
Exit
IC setting
File setting
Directory
Select MSM series
6376 6372 6373 6374
6375 5205 6295 6258
6378A 63P74 6388 6588
6585 6656 6655 6654
6653 6652 6650 6379
For 6388 and 6588
6595 6596 6597
Three or four bits can be selected.
3 bits
4 bits
For 6375 series
Org Frq f/16 f/10 f/8 Org Frq f/16 f/10 f/8
32.0 .... 4.0 102.4 6.4 ..... 12.8
40.0 ..... 4.0 (5.0) 106.0 ..... 10.6 .....
42.4 .... 5.3 128.0 8.0 12.8 16.0
51.2 .... 6.4 160.0 (10.0) 16.0 (20.0)
53.0 ..... 5.3 ..... 169.6 10.6 ..... 21.2
64.0 4.0 6.4 8.0 204.8 12.8 ..... 25.6
80.0 (5.0) 8.0 (10.0) 212.0 ..... 21.2 (26.5)
84.8 5.3 ..... 10.6 256.0 16.0 25.6 32.0
Binary file
Maximum synthesis size
Not create
Create
Dependent on IC
Expand to 16Mbits
HEX file directory

9


Screen dedicated to MSM series
Development support tool for voice synthesis ICs
Setting
Melody
ROM file
ROM writer
Exit
To VOICEPRO
MSM6650 family
Melody screen
Family other than MSM6650
ROM file creation screen
To screen dedicated to MSM series
MSM6650 family
ROM file creation screen dedicated to 6650
Screen dedicated to ROM writer
ROM selection
File loading
ROM writing
End
To screen dedicated to MSM series
Erasure check
Write
Verify
Automatic writing
ROM loading
File selection
XXXXXXXX
64K
128K
256K
512K
1M
2M
4M
OTP
MSM63P74
MSM6378A
MSM6379
MSM66P54

9

OKI Semiconductor

ANAWRITER MK6

Voice Analysis and Editing Tool for MSM6378A/6379

GENERAL DESCRIPTION

ANAWRITER MK6 is a dedicated tool that loads OKI's MSM6378A (voice synthesis IC containing 256-Kbit OTP) and MSM6379 (voice synthesis IC containing 512-Kbit OTP) with voice analysis data. It can run on 90 to 250 V AC. Therefore, it can be used in any country without voltage modifications. This tool has two input jacks: microphone input (with built-in ALC) and line input jack.
Write time in an MSM6378A/6379 is eight seconds, including time for verification.
A ROM (EPROM) master can be made by preparing a backup using an external I/F. If a PARAWRITER is used with the master ROM, write and verify for ten MSM6378A/6379 can be simultaneously completed within 11 seconds.

FEATURES

- Voice analysis: OKI ADPCM
- Microphone input: 600 Ω, with built-in ALC
- Line input: 10kΩ, –10dB
- Recording monitor: Input level is displayed on a bar graph LED
- Playback monitor: Reproduced sound can be heard from a built-in speaker
- Functions: Record, playback, write, playback
- Options: Backup (master ROM generation tool), PARAWRITER (ten-ROM parallel writing tool)
- Supply voltage: 90 to 250V AC
- Write and verify time: 8.0 seconds

RECORDING TIME

Sampling frequency (kHz)	Recording time (MSM6378A/6379) (sec)
4	15.6/31.2
6	10.4/20.8
8	7.8/15.6
10	6.2/12.4
12	5.2/10.4
14	4.5/9.0
16	3.9/7.8

OPERATION

Refer to the diagram in the section MECHANICAL DIMENSIONS for the callout locations.

a. Power-on

Connect the AC power supply (1), and turn on the power switch (2).

- The power lamp (11) lights.
- "88" is displayed on the indicator (14). Then it changes to "4".
- The sampling lamp (9) lights.

b. Switch the sampling frequency

- Press the sampling frequency selector switch (15) to select another sampling frequency.
- The indicator (14) shows the selected sampling frequency.
- Each time the sampling frequency switch (15) is pressed, the sampling frequency changes as follows:

  $\rightarrow 4 \rightarrow 6 \rightarrow 8 \rightarrow 10 \rightarrow 12 \rightarrow 14 \rightarrow 16 \rightarrow$

- While a sampling frequency is indicated on the sampling indicator (14), the sampling lamp (9) remains on.

c. Record

Insert the microphone plug into the microphone input jack (6), attach a sound source to the input jack (7). When sound is entered, the level meter (4) works.

Press the record switch (16) to start recording.

At the same time, ADPCM analysis is performed.

- The lamp for the record switch (16) is lit.
- During recording, the lamp (10) remains on.
- The indicator (14) shows the residual recording time.

When recording is complete, the indicator (14) shows a sampling frequency again.

d. Playback (checking of recorded voice)

Press the switch (17) to begin voice reproduction. Sound volume can be adjusted using the monitor control (5). During playback, the lamp for the playback switch (17) lights.

e. Write to the MSM6378A/6379

Check the direction of the 6378A with the lever of TEXTOOL® (20) raised. Place the MSM6378A/6379 in the TEXTOOL® socket, and lower the lever.

Make sure that the MSM6378A/6379 is placed horizontally.

Press the MSM6378A/6379 write switch (18) to start writing.

During writing, the MSM6378A/6379 busy lamp (12) and write lamp (18) are lit. In eight seconds, write and verify are completed.

If the error lamp (13) comes on when writing is over, writing has not been done normally.

In this case, the indicator (14) shows an error code.

E0: The MSM6378A/6379 is not in the TEXTOOL® socket, or is not in the socket correctly.
E3: An error occurred during writing, and writing was aborted.

Any other error : A failure has occurred with the ANAWRITER.

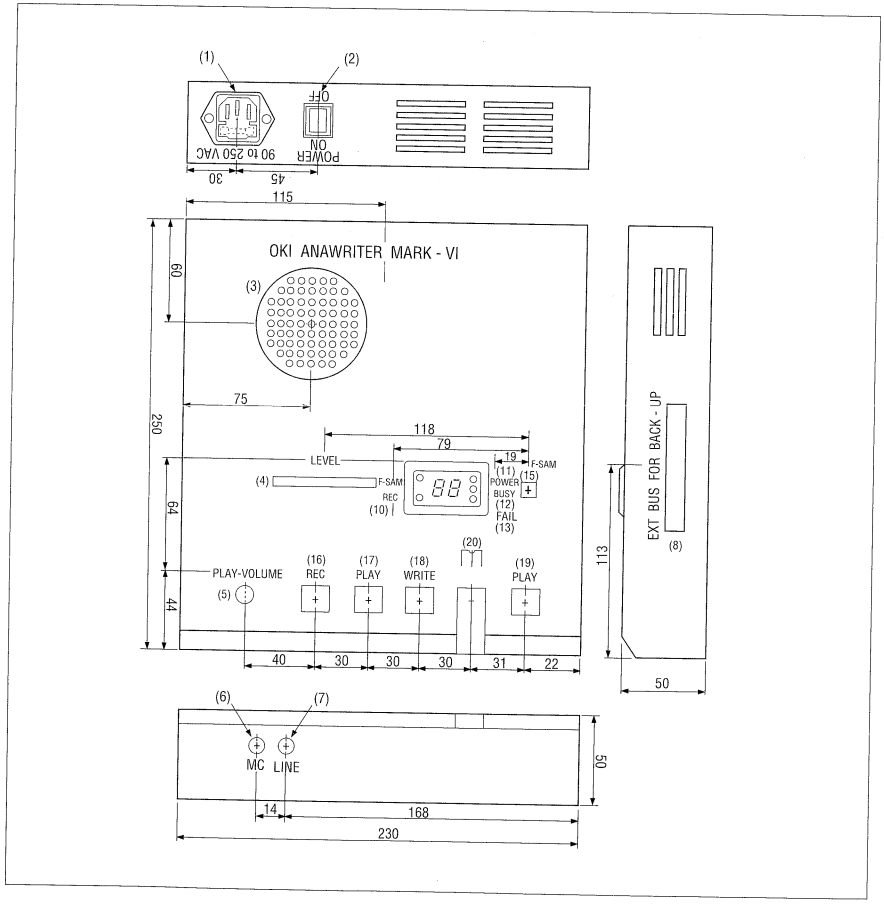
If any key is pressed when the indicator (14) display an error, the display is changed to a sampling frequency.

f. Reproduce from the MSM6378A/6379

Check the direction of the MSM6378A/6379 with the lever of TEXTOOL®(20) raised. Place it in the TEXTOOL® socket, and lower the lever to fix it.

Sound volume can be adjusted using the monitor control (5) in the same way as item d (playback). During voice reproduction, the lamp for the MSM6378A/6379 play switch (19) and the MSM6378A/6379 busy lamp (12) are lit.

MECHANICAL DIMENSIONS



OKI Semiconductor

BACKUP

EPROM Backup Tool for MSM6378A

GENERAL DESCRIPTION

BACKUP is an EPROM writer for an MSM27256 EPROM. It loads the EPROM with voice and other data, generated using the ANAWRITER MK2. BACKUP is connected to the ANAWRITER MK2 through a 40-pin flat cable.
The MSM6378A cannot read the voice data of the MSM6378A itself to write to another device.

FEATURES

- Applicable EPROMs : MSM27C256 or MSM27256
- Function switches : LOAD
  PLAY
  BLANK — Blank check
  WRITE — EPROM write
  VERIFY — EPROM verify
- Function light emitting diodes (LED) : BUSY
  FAIL
- Interface with the ANAWRITER MK2 : 40-pin flat cable

FUNCTION SWITCHES

LOAD Loads data from EPROM to the ANAWRITER MK2.

PLAY Reproduces voice data loaded into the ANAWRITER MK2. The switch has the same function as the ANAWRITER MK2 PLAY switch.

BLANK Used for blank check of EPROM (MSM27256).

WRITE Writes voice data generated in the ANAWRITER MK2 to the EPROM (MSM27256). This switch invokes three modes: blank, write, and verify.

VERIFY Compares data in the ANAWRITER MK2 with those in EPROM for verification.

FUNCTION LEDs

BUSY LED : It is lit during LOAD, BLANK, WRITE, and VERIFY.
It is not lit during PLAY.

FAIL LED : If this LED is lit:

- Upon blank check, the data in the EPROM was found not to be blank.
- A write error occurred during writing.
- A verify error occurred during verify.

OKI Semiconductor

PARAWRITER

Parallel Writing Tool for MSM6378A

GENERAL DESCRIPTION

The PARAWRITER writes data for up to ten MSM6378As at a time using a master EPROM (MSM27256), which is prepared with the EPROM BACKUP writer.

SPECIFICATIONS

Master ROM	:	MSM27C256 or MSM27256
Programmable device	:	MSM6378A
Writing time	:	11 seconds (with data written to ten MSM6378As simultaneously)
Function keys		
LOAD	:	Reads data from EPROM.
WRITE	:	Writes data to MSM6378A.
RESET	:	Resets an error lamp.
Buzzer		
Write error		Buzz..Buzz..Buzz
Normal end of writing		Beep
Upon loading		Beep
Upon resetting		Beep

FUNCTION KEYS

LOAD key	Loads data from a master EPROM (27256) to the PARAWRITER.
WRITE key	Writes data to up to ten MSM6378As simultaneously.
RESET key	Resets any error lamp one through ten.

FUNCTION LIGHT EMITTING DIODE (LED)

BUSY LED	Lit during loading/writing.

LEDs ONE THROUGH TEN

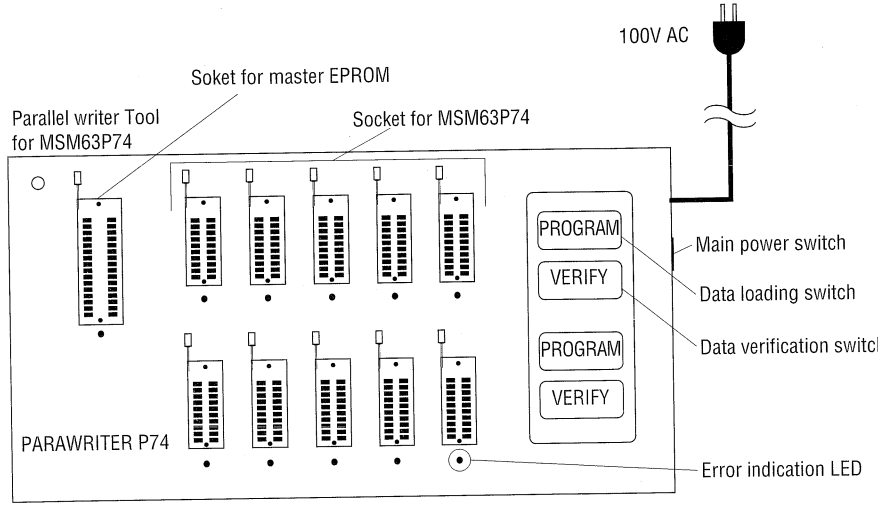
Any of the lamps one through ten is lit if the MSM6378A is not placed in the 16-pin TEXTOOL® socket, or if a write error occurs.

OKI Semiconductor

PARAWRITER P74

Parallel Writing Tool for MSM63P74

BOARD DESIGN



GENERAL DESCRIPTION

This unit loads (1 to 10) MSM63P74 devices with data for master EPROM (1 M) created by a voice analysis and editing tool (AR761/AR762/AR76-202/AR203).

DATA WRITING

Turn on the main power switch. (A short beep sounds.)
Set the master EPROM.
Insert the MSM63P74.
Pressing the data loading switch starts blank checking, followed by data loading and verification.
During this operation, the error indication LED is lit.

VERIFICATION

In the same way as for data loading, insert the master EPROM and the MSM63P74, and press the verification switch.

ERROR

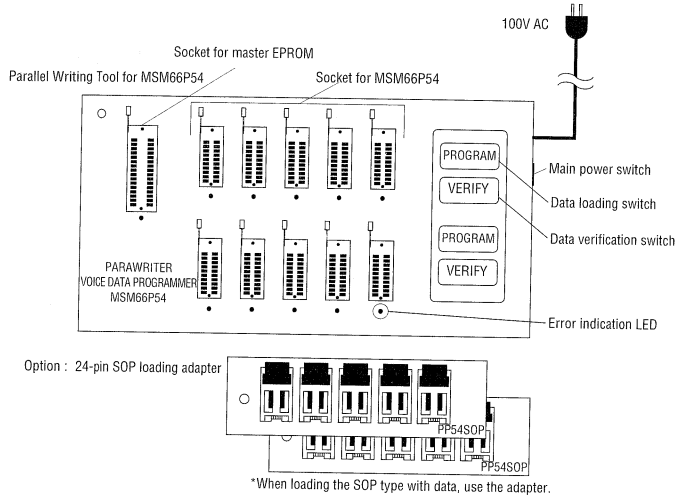
Upon the normal termination of loading and verification, the LED goes out with short beeps. If a device error has occurred, however, the LED blinks with beeps.
When devices for only part of the five sockets are loaded, error sound is generated as no devices are set at sockets, and the LEDs for the sockets blink. When the LEDs for the sockets where devices are set are extinguished, loading has been completed successfully.

OKI Semiconductor

PARAWRITER P54

Parallel Writing Tool for MSM66P54

BOARD DESIGN



GENERAL DESCRIPTION

This unit loads (1 to 10) MSM66P54 devices with data for master EPROM (1 M) created by a voice analysis and editing tool (AR761/AR762/AR76-202/AR203).

DATA WRITING

When loading the SOP type, set the SOP adapter set as an option. (The adapter is not needed for the DIP type.)
Turn on the main power switch. (A short beep sounds.)
Set the master EPROM.
Insert the MSM66P54.
Pressing the data loading switch starts blank checking, followed by data loading and verification.
During this operation, the error indication LED is lit.

VERIFICATION

In the same way as for data loading, insert the master EPROM and the MSM66P54, and press the verification switch.

ERROR

Upon the normal termination of loading and verification, the LED goes out with short beeps. If a device error has occurred, however, the LED blinks with beeps.
When devices for only part of the five sockets are loaded, error sound is generated as no devices are set at sockets, and the LEDs for the sockets blink. If the LEDs for the sockets where devices are set are extinguished, loading has been completed successfully.

DEMONSTRATION BOARDS

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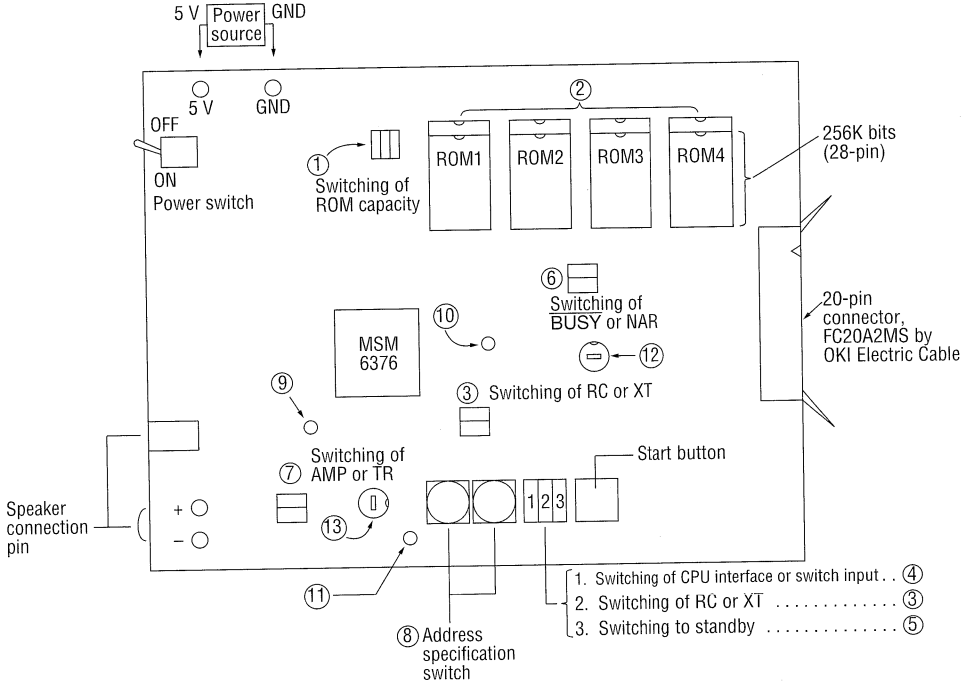
OKI Semiconductor

MSM6376 EVA BOARD

MSM6376 Evaluation Board

BOARD DESIGN



BOARD FEATURES

① ROM-capacity Switching Jumper

256K-bit and 1M-bit (× 8-bit) CMOS type EPROMs can be used. For a 256K-bit EPROM, bridge the lower pins. For a 1M-bit EPROM, bridge the upper pins.

Note : Use an Intel (27C010) equivalent type 1-Mbit EPROM.

② EPROM Socket

Insert EPROMs with the smaller address sequentially from the left. The EPROM socket has 32 pins. For 256K-bit EPROMs (28-pin), align them to the lower end.

③ RC/XT Selector Switch and Jumper

This switch selects RC oscillation or crystal oscillation. To operate the IC with RC oscillation, turn the DIP switch to OFF and set the jumper to the left. To operate the IC with crystal oscillation, turn the DIP switch to ON and set the jumper to the right.

④ CPU Interface/Input Interface Selector Switch

This switch sets operation to CPU or to the momentary button labeled ST.

When using only this evaluation board, select "Switch Input" (at the DIP switch to OFF). When connecting the evaluation board to a CPU, turn the DIP switch to ON. When the CPU is connected, all necessary signals are connected to the 20-pin connector. The connector pins are arranged as shown below.

Connector Pin No.	Signal	Connector Pin No.	Signal
1	DV_{DD}	11	I5
2	DV_{DD}	12	I6
3	DV_{DD}	13	$\overline{2CH}$
4	NC	14	$\overline{RESET}$
5	NC	15	$\overline{ST}$
6	I0	16	$\overline{RCS}$
7	I1	17	$\overline{BUSY}$/NAR
8	I2	18	GND
9	I3	19	GND
10	I4	20	GND

Note: Leave NC lines connections open. Set the $\overline{RCS}$ signal at Pin 16 to Low level.

⑤ Standby Selector Switch

When the standby selector switch is set to ON and the board is not activated within three seconds after the voice is terminated, the board enters the standby state. (In the standby state, all the functions of the IC stop.)

⑥ $\overline{BUSY}$/NAR Switching Jumper

When the jumper is turned to the left side, the $\overline{BUSY}$ signal is output from the 20-pin connector. When the jumper is turned to the right side, the NAR signal is output from the 20-pin connector. Refer to the data sheet for the timing of the $\overline{BUSY}$ or NAR signal.

⑦ AMP/TR Switching Jumper

To amplify an analog signal provided by the output pin AOUT with the transistor, turn the jumper to the right side. To amplify an analog signal provided by the output pin AOUT with the amplifier, turn the jumper to the left side.

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⑧ Address Specification Switch

When using only this demonstration board, select a word to be reproduced by this HEX switch. The left side is for MSB and the right side is for LSB. When 0F is set, for example, 0001111 is set in I6 to I0. When connecting the board to the CPU, set the address to 00 and remove the capacitor 0.1 µF (C18) near the start button.

⑨ DA Converter Output Pin (without LPF)

⑩ Input Frequency Check Pin

⑪ GND Pin

⑫ Variable Resistor (VR2) for adjusting the frequency of RC oscillation

⑬ Variable Resistor for volume control (shared by the amplifier and transistor)

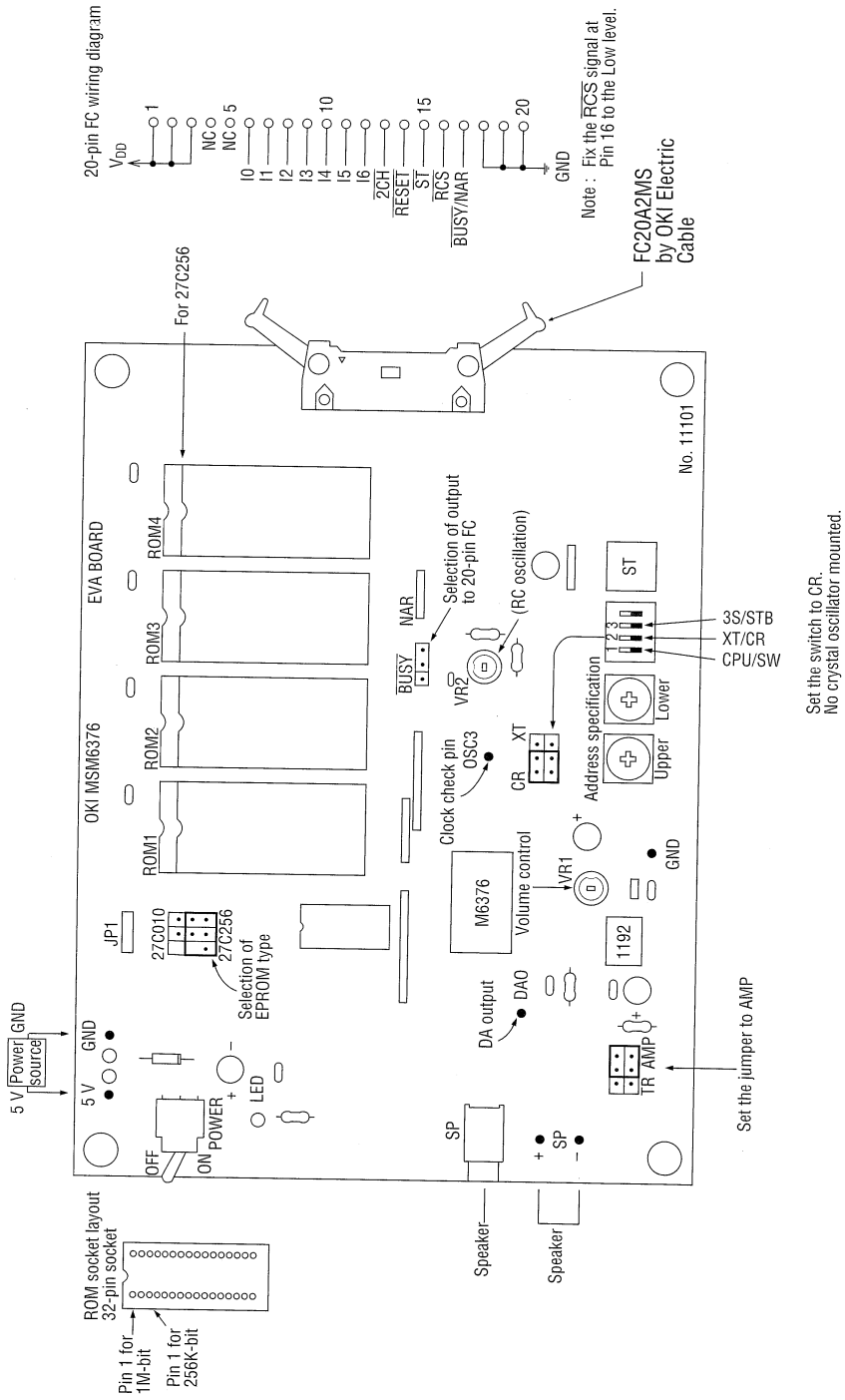
Note: Use a CMOS type 27C256 or 27C010 EPROM. When an NMOS type 27256 or 27010 EPROM is used, the supply current of the EPROM fluctuates, causing noise.

VOICE PLAYBACK PROCEDURE

1. Set the address specification switch.

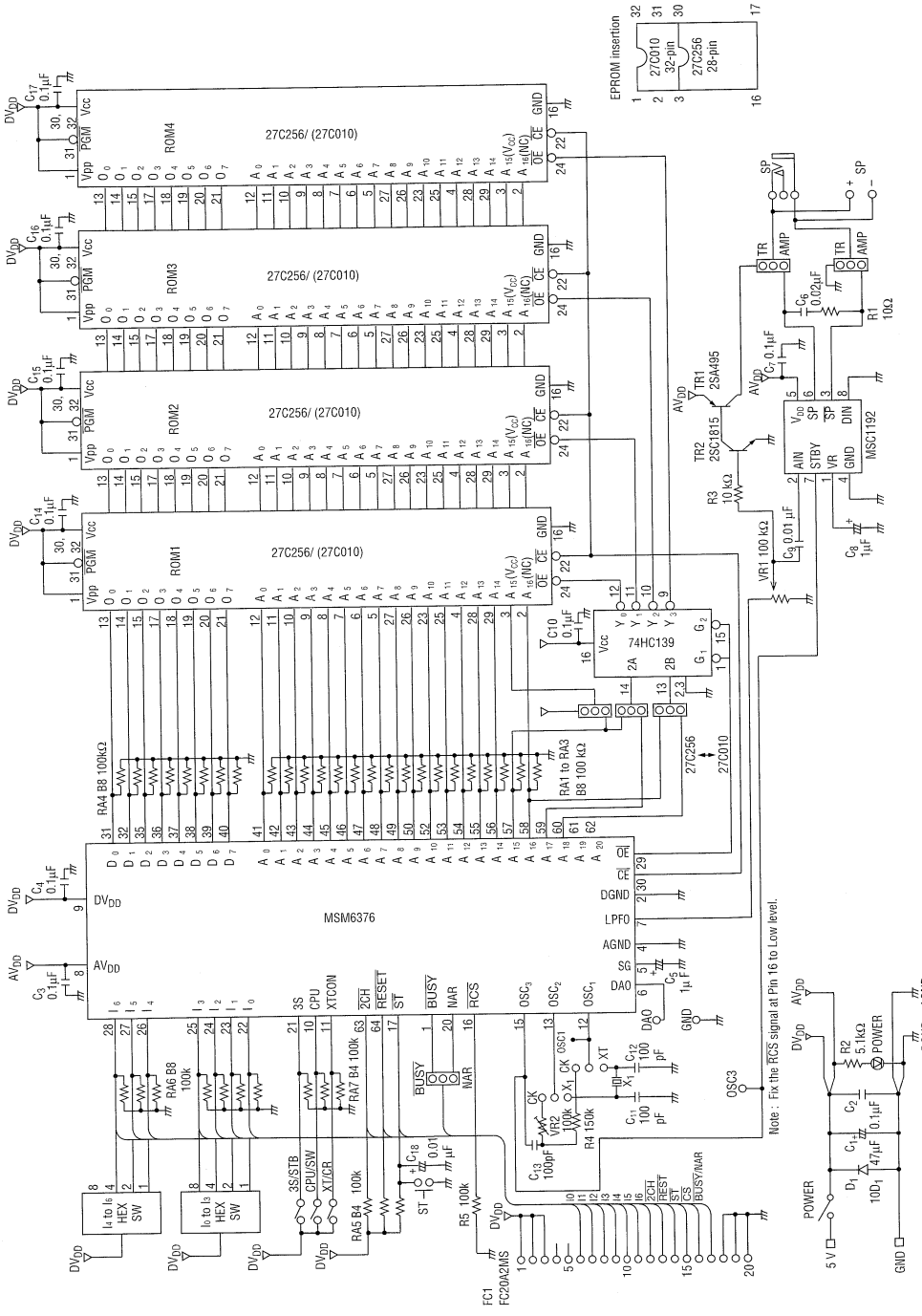
2. Press the start button.

BOARD DETAILS



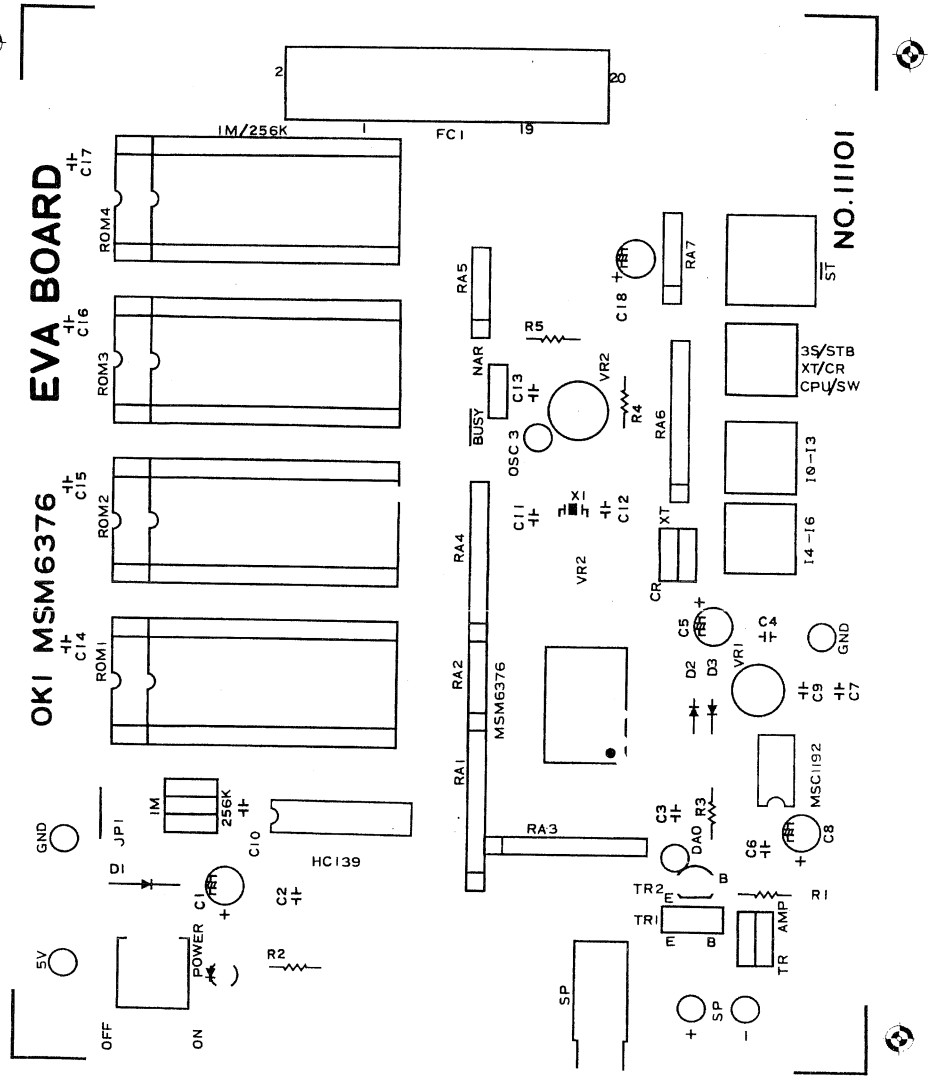
10

CIRCUIT DIAGRAM

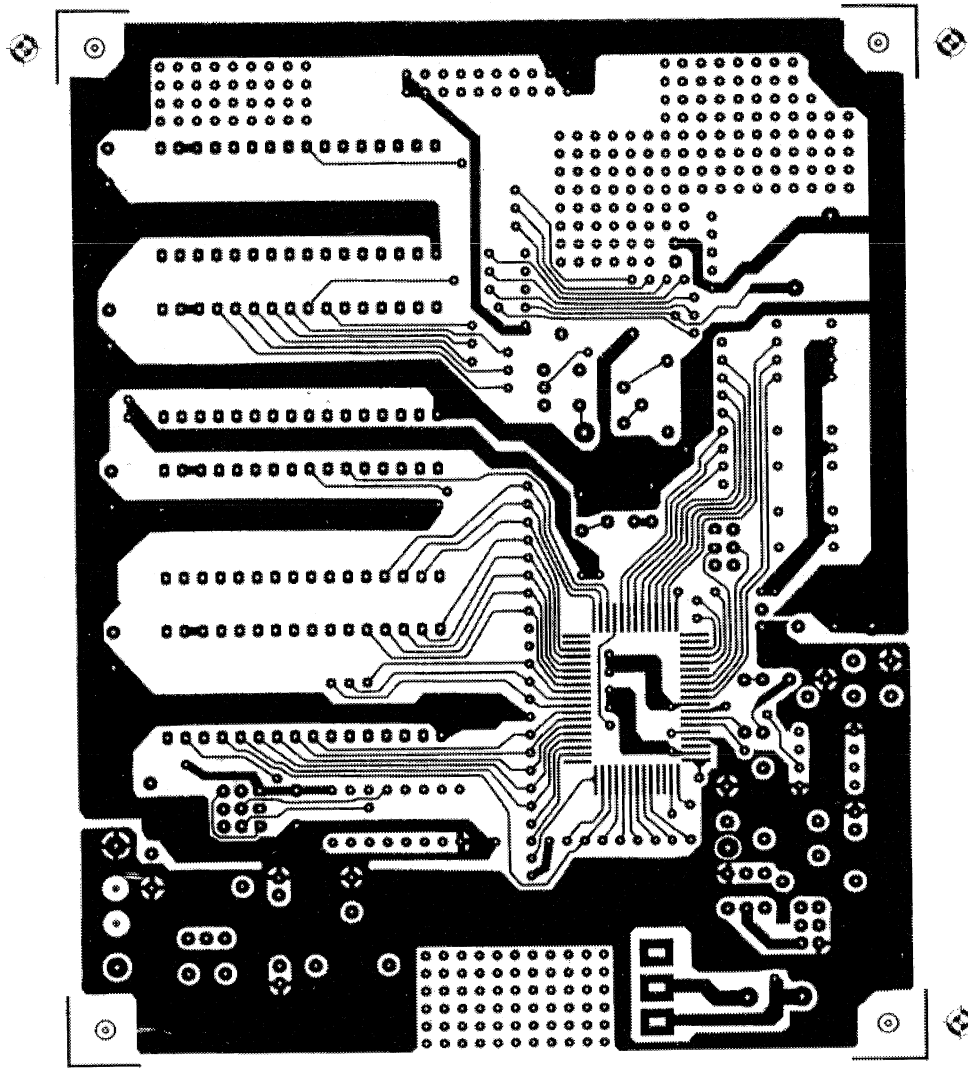


PATTERN LAYOUT

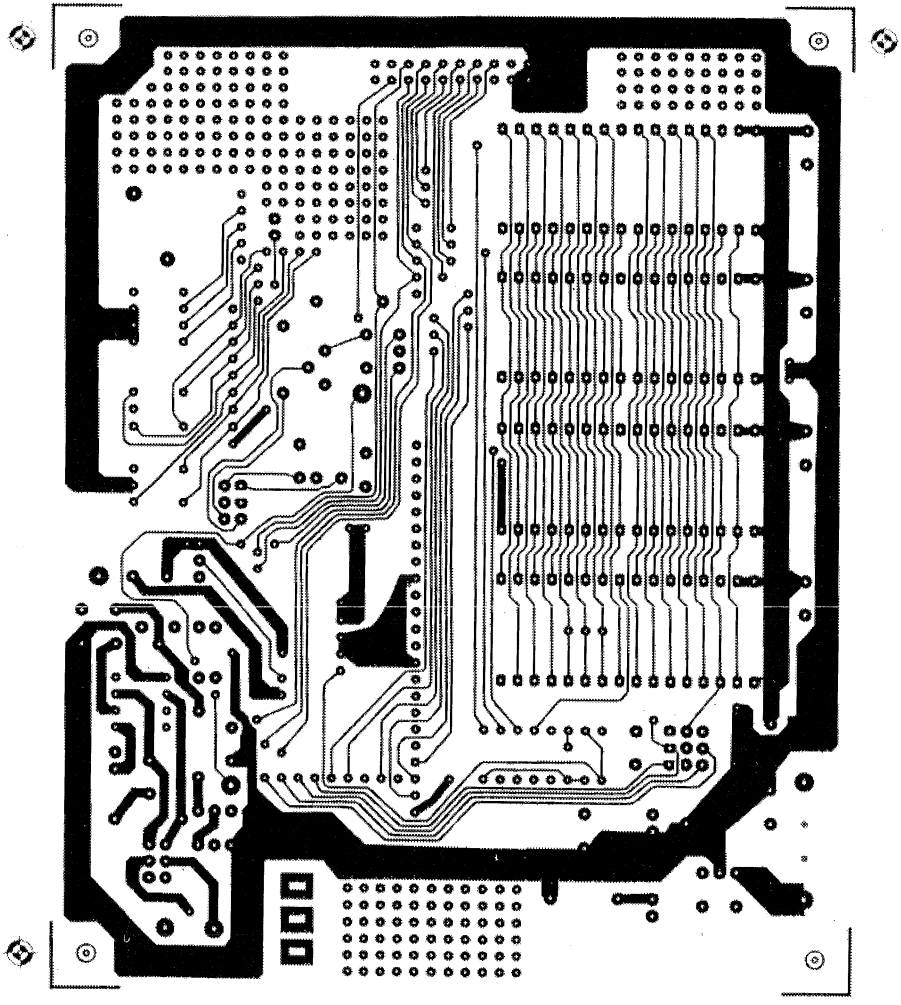
Silk Screen



Mounting Side



Solder Side

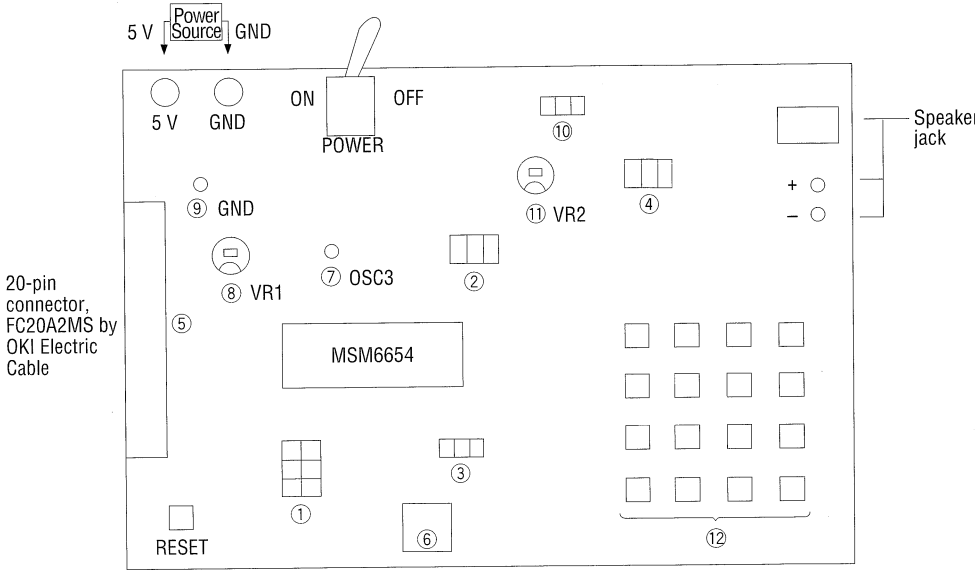


OKI Semiconductor

MSM6654 DEMO BOARD

MSM6654 Demonstration Board

BOARD DESIGN



BOARD FEATURES

①, ② Standalone/microcontroller interface switching jumpers and XT/$\overline{CR}$ switching jumpers
The jumpers in ① are used to select the operation by a standalone mode or by a microcontroller interface mode. The jumpers in ② are used to select RC oscillation or crystal oscillation. When a standalone mode is used, for RC oscillation, set the jumpers in ① to the lower right side and set the three jumpers in ② to the lower side. For crystal oscillation, set the jumpers in ① to the upper right side and set the three jumpers in ② to the upper side. When a microcontroller is used, only RC oscillation is settable. Set the jumpers in ① to the upper left side and set the three jumpers in ② to the upper side.

③ $\overline{BUSY}$/NAR switching jumper
When the jumper is turned to the right side, the $\overline{BUSY}$ signal is output from pin 17of the 20-pin connector. When the jumper is turned to the left side, the NAR signal is output from the same pin. When a standalone computer is used, turn the jumper to the right side.

④ AMP/TR switching jumpers
To amplify an analog signal which is output from AOUT, with transistors, set the two jumpers to the right side. To amplify it with an amplifier, turn the two jumpers to the left.

⑤ 20-pin connector
All necessary signals are connected to the 20-pin connector when a microcontroller is used. The connector pins are arranged as shown below.

Connector pin No.	Signal	Connector pin No.	Signal
1	DV_{CC}	11	I5
2	DV_{CC}	12	I6
3	DV_{CC}	13	$\overline{CH}$
4	NC	14	$\overline{RESET}$
5	NC	15	$\overline{ST}$
6	I0	16	$\overline{CS}$
7	I1	17	$\overline{BUSY}$/NAR
8	I2	18	GND
9	I3	19	GND
10	I4	20	GND

⑥ Address specification switch
When a standalone mode is used, select a word to be played by this HEX switch. 0~7 in this HEX switch correspond to A0~A2 in binary data. When a microcontroller is used, set the HEX switch to 0.

⑦ Frequency check pin (OSC3)
This pin monitors and checks the oscillation frequency.

⑧ Speaker amplifier volume (VR1 shared by AMP/TR)
Turn the volume switch to the right to increase the sound volume. Turn the volume switch to the left to reduce the sound volume.

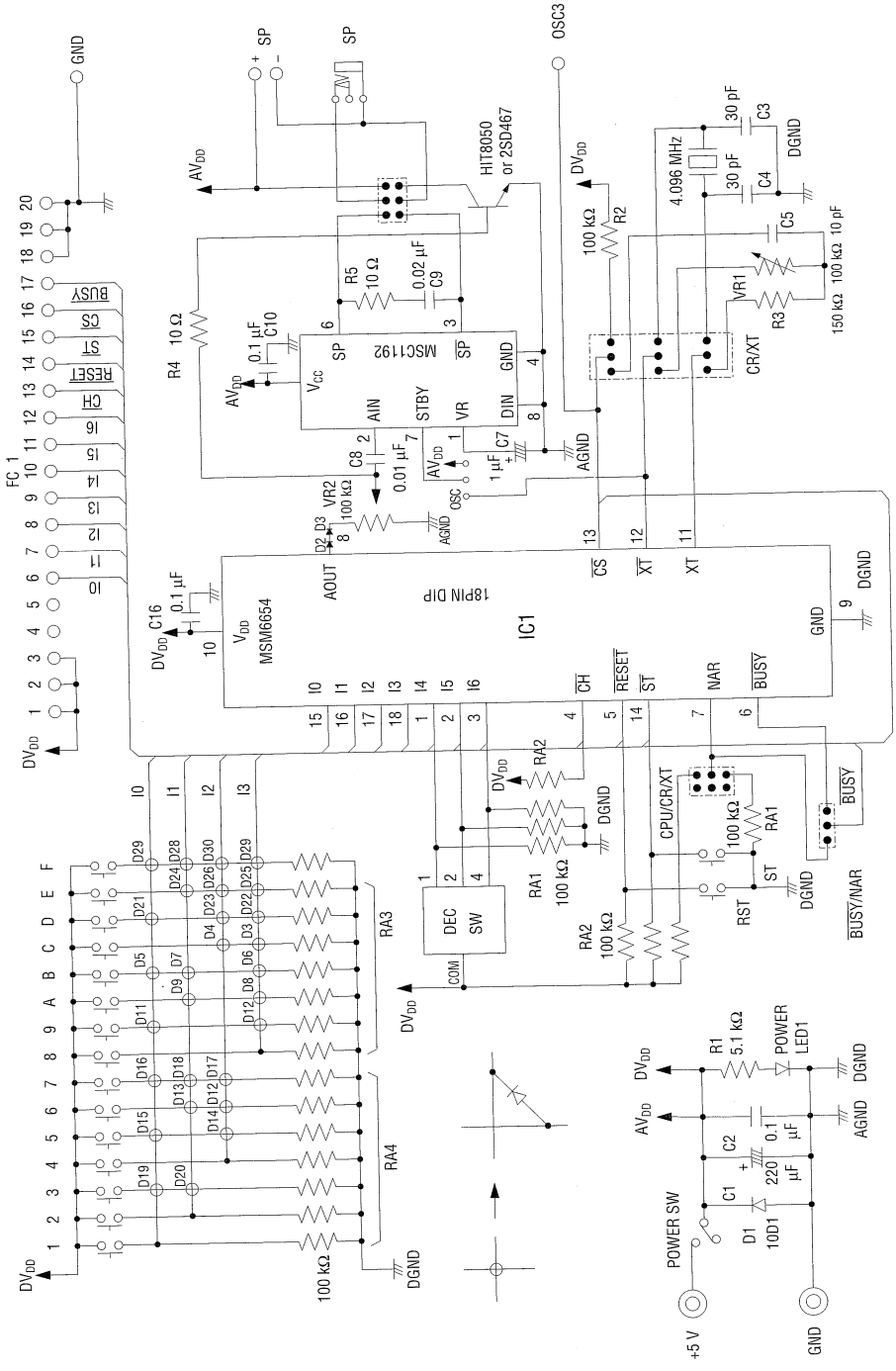
⑨ GND pin

⑩ OSC/VDD switching jumper
Set the jumper to the left side.

⑪ Variable resistor (VR2) for adjusting the frequency of RC oscillation.
This variable resistor can change the frequency of RC oscillation. When the resistor is turend to the right, the frequency goes low. When the resistor is turned to the left, the frequency goes high. In this case, the frequency can be monitored by pin 7.

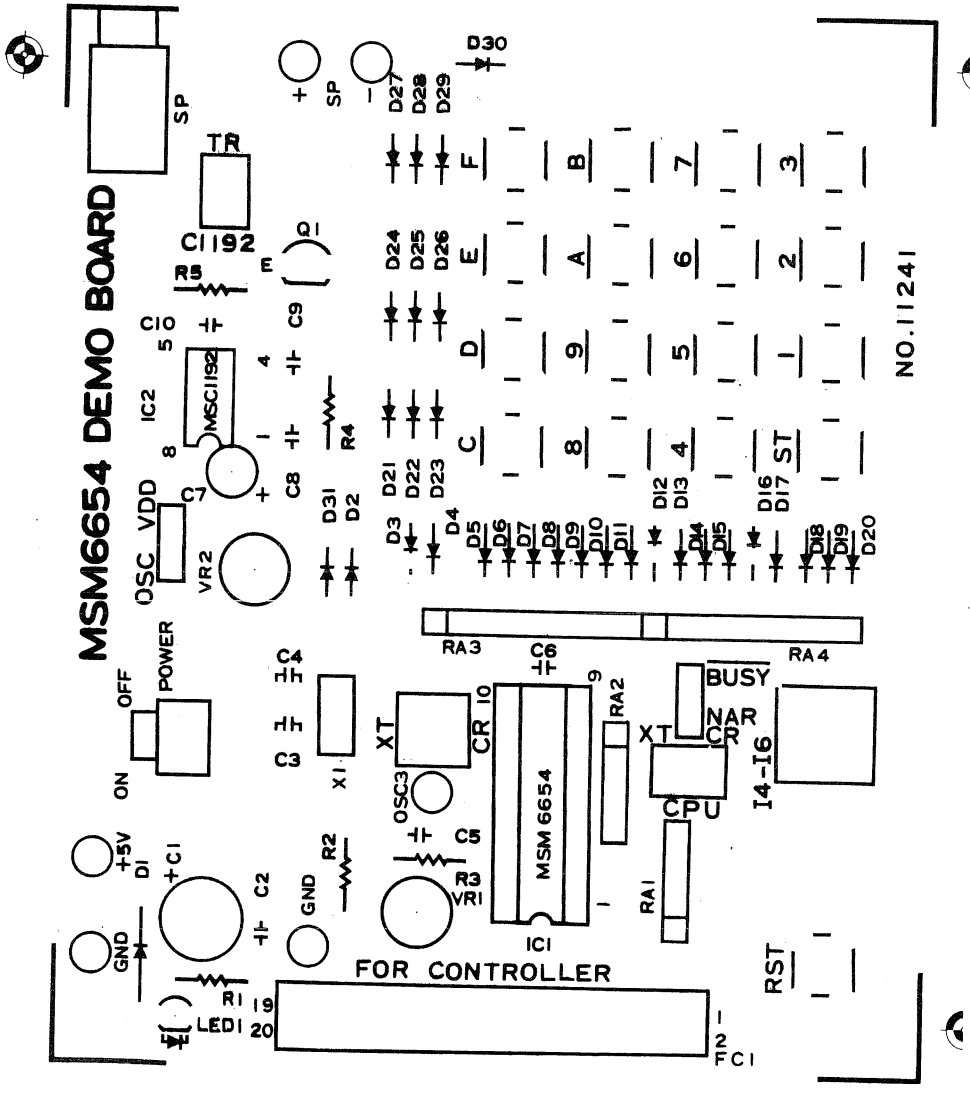
⑫ Complete SW input interface
When a standalone computer is used, press the 1~F buttons to play voices correspon-ding to 1~F of SW3~SW0. Press the lower left ST button (random voice playback button) to play voices that are randomly selected from 31 types of phrases corresponding to A0 and SW3~SW0. But, when the ST switch is pressed while turning the power ON or during the input of $\overline{RESET}$, firstly voice playback is made starting from the 1st phrase and beyond secondly it is made randomly.

CIRCUIT DIAGRAM

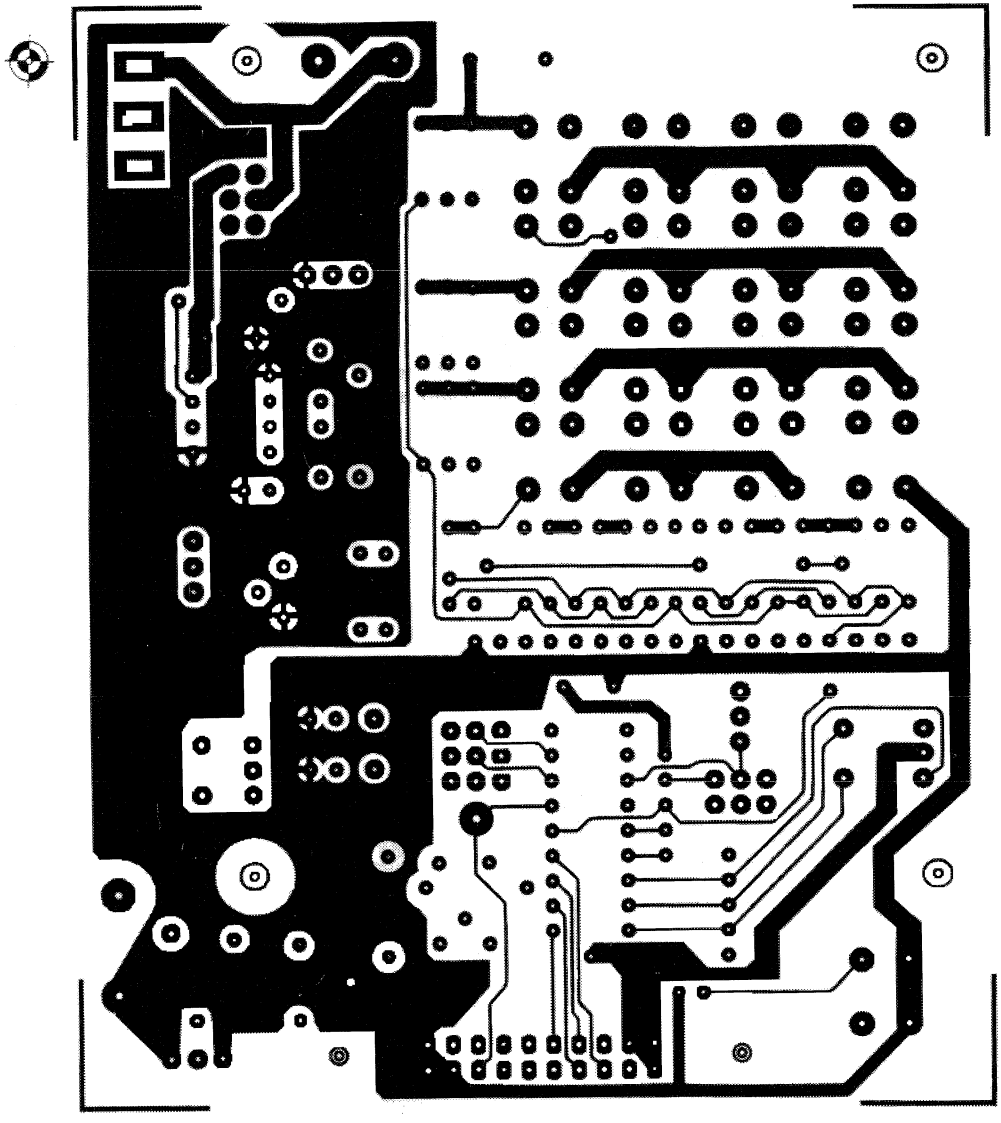


PATTERN LAYOUT

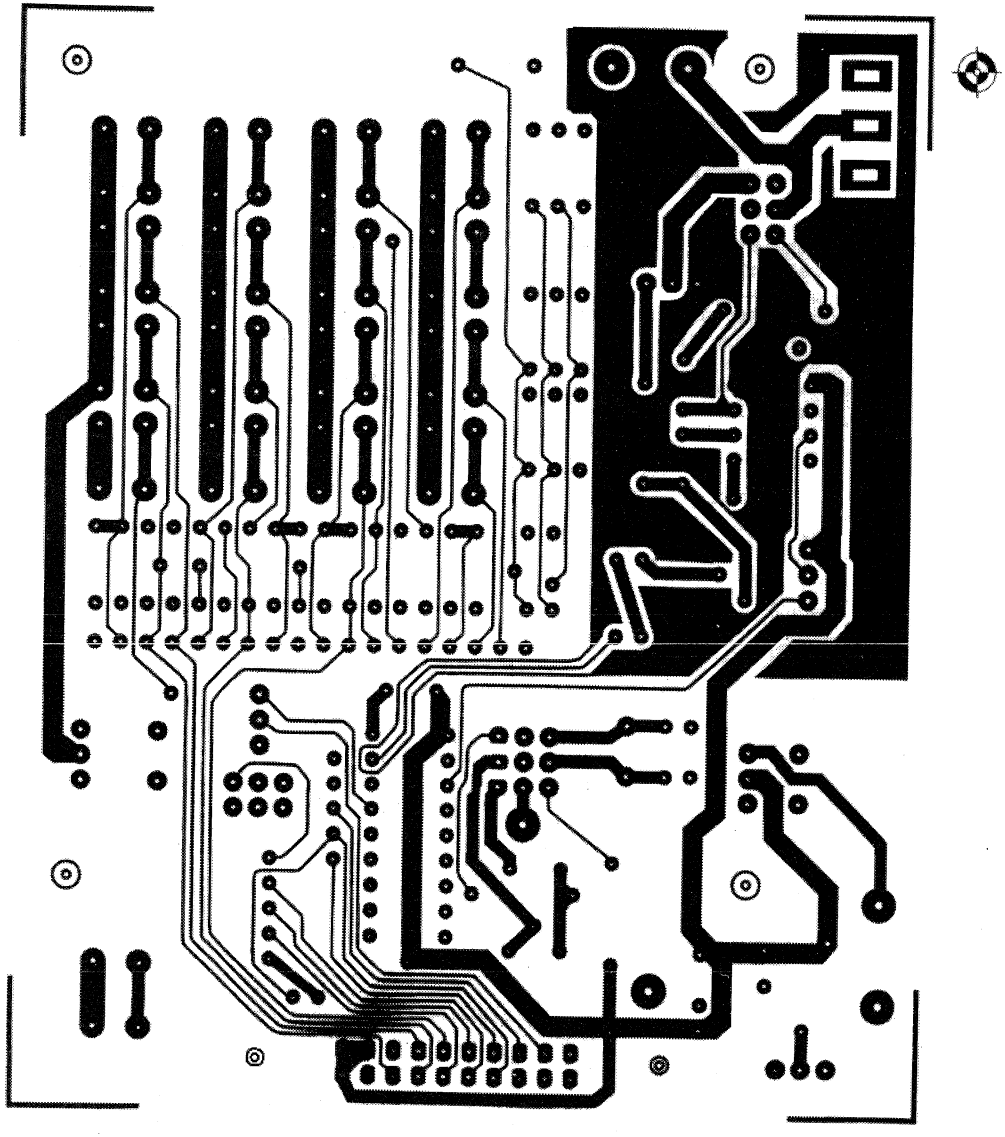
Silk Screen



Mounting Side



Solder Side

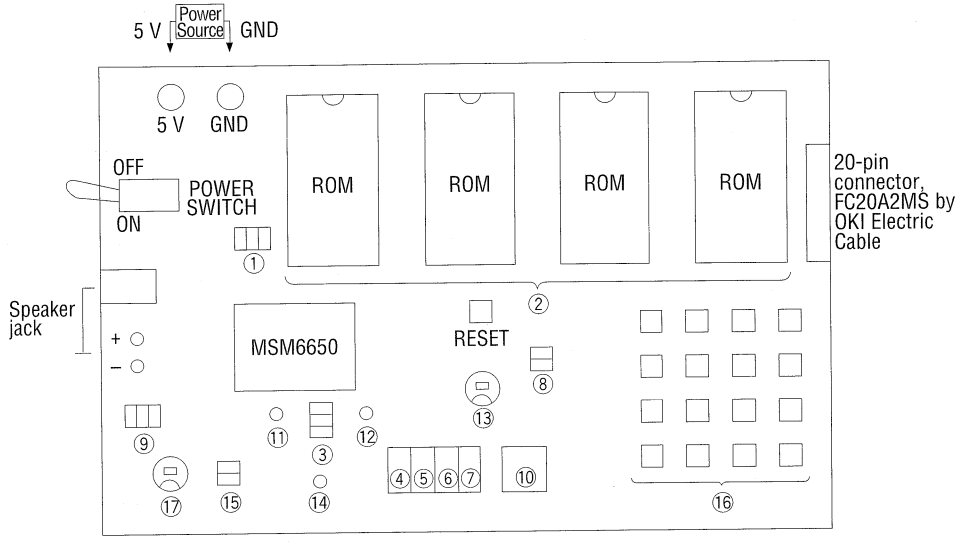


OKI Semiconductor

MSM6650 EVA BOARD

MSM6650 Evaluation Board

BOARD DESIGN



BOARD FEATURES

① ROM capacity switching jumpers
1M-bit and 4M-bit CMOS type EPROMs can be used. For a 1M-bit EPROM, set the three jumpers to the lower pins. For a 4M-bit EPROM, set them to the upper pins.

② EPROM socket
Insert EPROMs fabricated by voice analysis, sequentially from the left.

③, ④ XT/$\overline{\text{CR}}$ selector switch and jumpers
This switch selects RC oscillation or crystal oscillation. To operate the IC with RC oscillation, turn the DIP switch to the lower side and set the two jumpers in ③ to the upper side. To operate the IC with crystal oscillation, turn the DIP switch to the upper side and set the two jumpers in ③ to the lower side.

⑤ Stand-alone/microcontroller selector switch
This switch selects the operation by a stand-alone mode or by a microcontroller interface mode. For a stand-alone mode, turn the DIP switch to the lower side. For a microcontroller, turn the DIP switch to the upper side. When the microcontroller is connected, all necessary signals are connected to the 20-pin connector. The connector pins are arranged as shown below. If the standalone computer is used, turn the SIRI switch ⑥ to the lower side.

Connector pin No.	Signal	Connector pin No.	Signal
1	DV_{DD}	11	I5
2	DV_{DD}	12	I6
3	DV_{DD}	13	$\overline{CH}$
4	NC	14	$\overline{RESET}$
5	NC	15	$\overline{ST}$
6	I0	16	$\overline{CMD}$
7	I1	17	$\overline{BUSY}$/NAR
8	I2	18	GND
9	I3	19	GND
10	I4	20	GND

⑥ Serial input interface/parallel input interface selector switch
When a microcontroller is used, this switch selects the serial inputs of addresses and command data or the parallel inputs of them. For the serial inputs, turn the switch to the upper side. For the parallel inputs, turn the switch to the lower side.

⑦ Standby selector switch
When the switch is turned to the lower side and the board is not activated toward the next phrase within 0.2 second after the voice is terminated, the board enters the standby state. (In the standby state, all the functions of the IC are stopped.)

⑧ $\overline{BUSY}$/NAR switching jumper
When the jumper is turned to the upper side, the $\overline{BUSY}$ signal is output from the 20-pin connector. When the jumper is turned to the lower side, the NAR signal is output from the 20-pin connector. When a standalone computer is used, set the jumper to the upper side.

⑨ AMP/TR switching jumpers
To amplify an analog signal which is output from AOUT, with transistors, set the two jumpers to the left side. To amplify it with an amplifier, turn the two jumpers to the right.

⑩ Address specification switch
When a stand-alone computer is used, select a word to be reproduced by this HEX switch. 0 to 7 in this HEX switch correspond to A0 to A2 in binary data. When a microcontroller is used, set the HEX switch to 0.

⑪ LPF output pin
This pin outputs a voice signal passed through the low path filter. When the DA converter is selected by option, this pin works as the DA converter pin.

⑫ Frequency check pin (OSC3)
This pin monitors and checks the oscillation frequency.

⑬ Variable resistor (VR2) for adjusting the frequency of RC oscillation.
This variable resistor can change the frequency of RC oscillation. When the resistor is turned to the right, the frequency goes low. When the resistor is turned to the left, the frequency goes high. In this case, the frequency can be monitored by the OSC3.

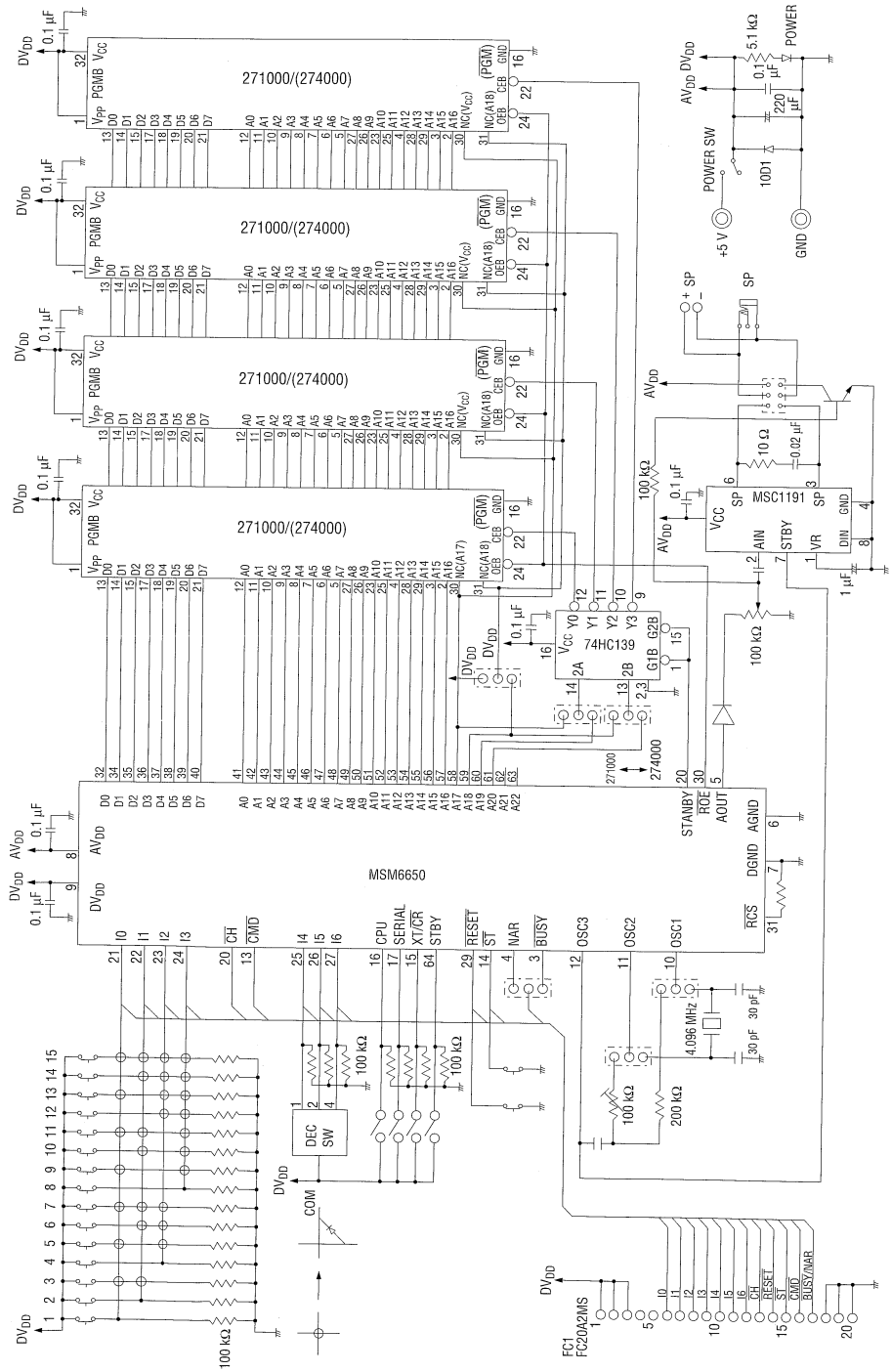
⑭ GND pin

⑮ OSC/GND switching jumper
Set the jumper to the up side.

⑯ Complete SW input interface
When a stand-alone mode is used, press the 1 to F buttons to play voices corresponding to 1 to F of SW3 to SW0. Press the lower left ST button (random voice playback button) to play voices that are randomly selected from 31 types of phrases corresponding to A0 and SW3 to SW0. But, when the ST switch is pressed while turning the power ON or during the input of $\overline{\text{RESET}}$, firstly voice playback is made starting from the 1st phrase and beyond secondly it is made randomly.

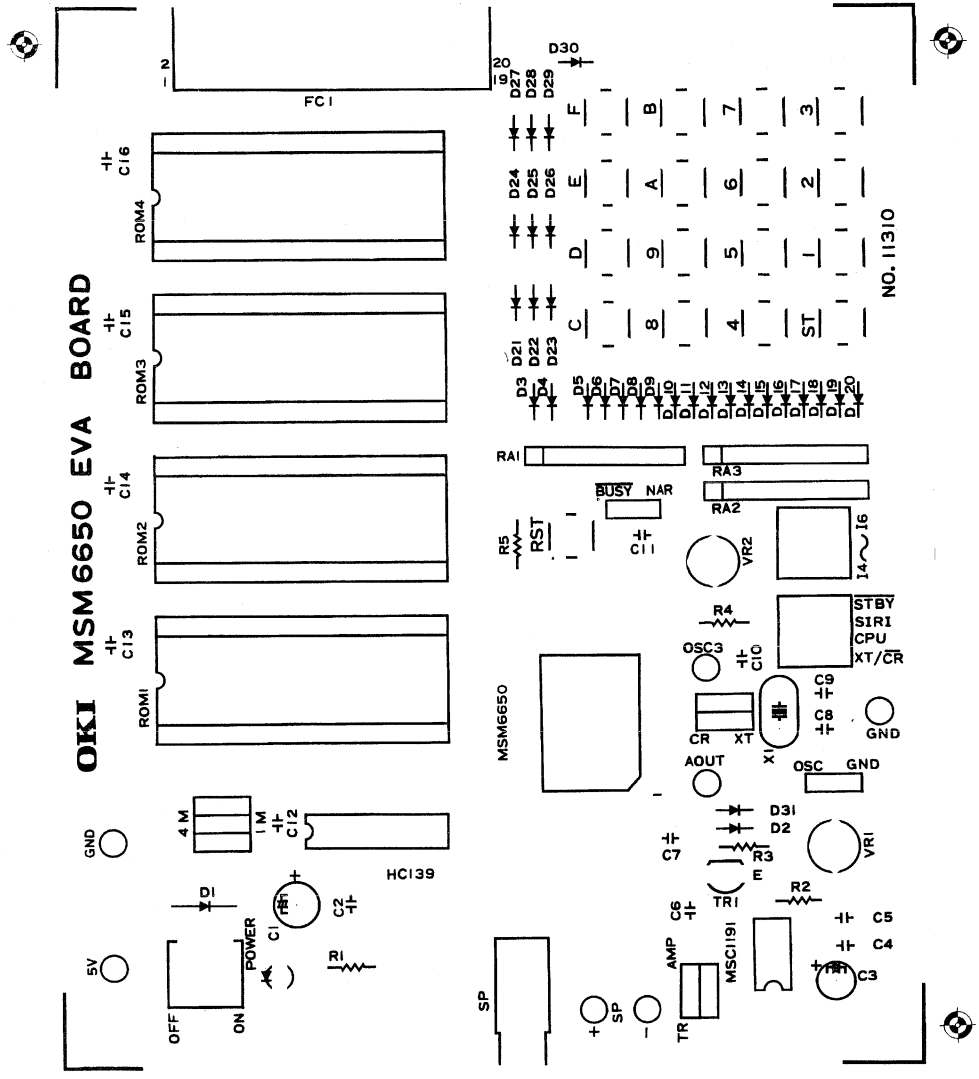
⑰ Speaker amplifier volume (VR1 shared by AMP/TR)
Turn the volume switch to the right to increase the sound volume. Turn the volume switch to the left to reduce the sound volume.

CIRCUIT DIAGRAM

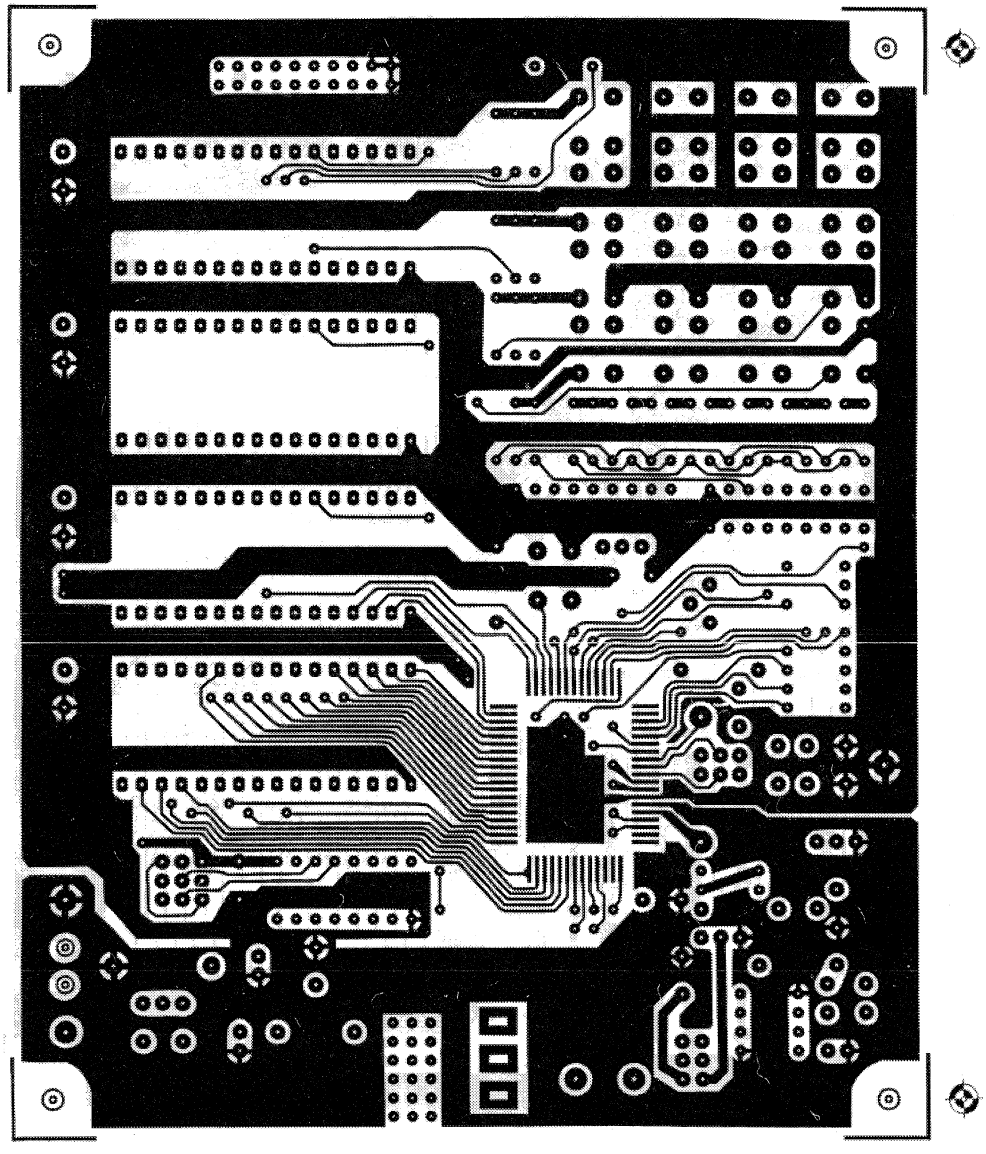


PATTERN LAYOUT

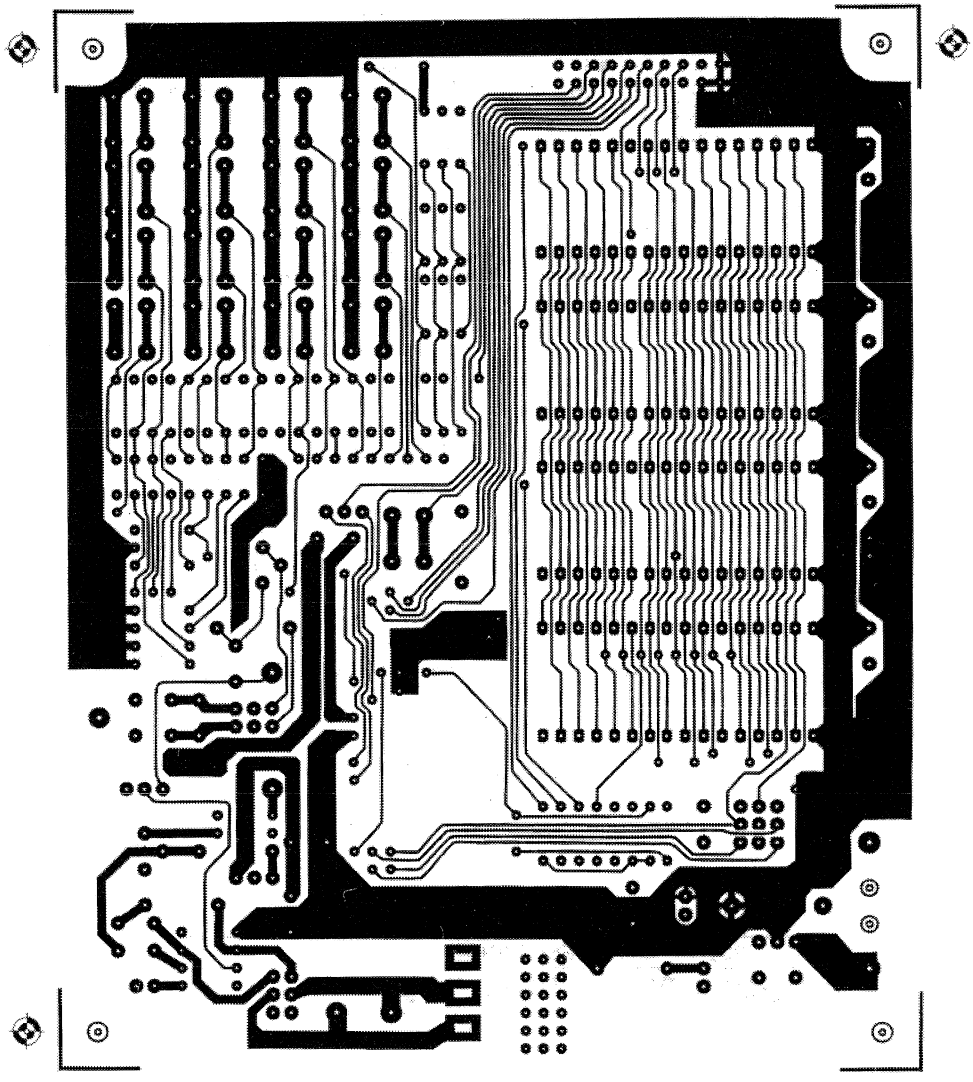
Silk Screen



Mounting Side



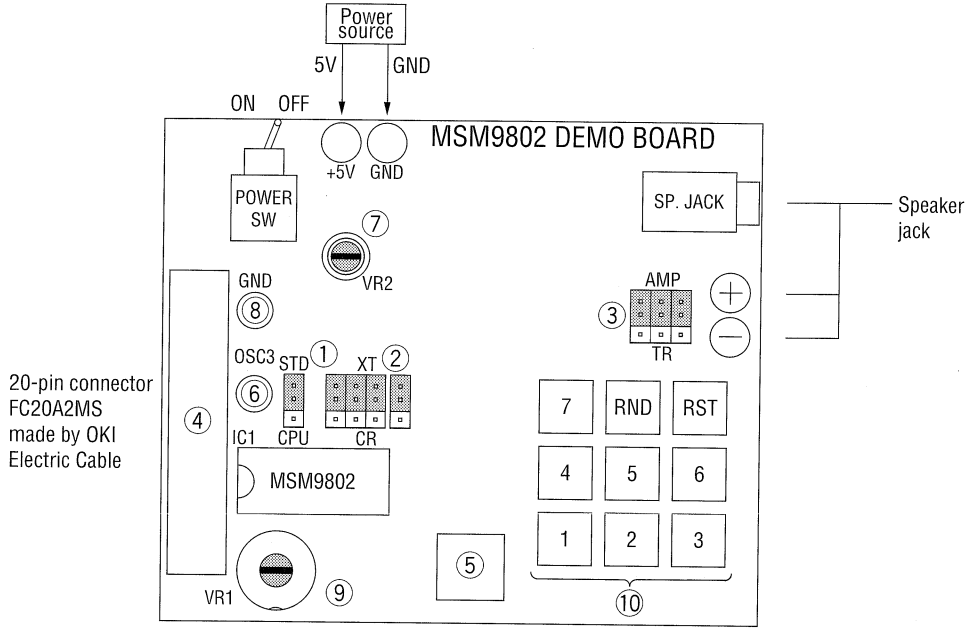
Solder Side



MSM9802 DEMO BOARD

MSM9802 DEMONSTRATION BOARD

BOARD OUTLINE



HOW TO USE BOARD

① Stand-alone/microcontroller interface selection jumper
The stand-alone/microcontroller selection jumper is used to select the operation in stand-alone mode or the operation by a microcontroller interface. For the stand-alone operation, set the jumper wire up (to STD). For the operation by a microcontroller interface, set the jumper wire down (to CPU).

② Ceramic oscillation/RC oscillation selection jumper
The ceramic oscillation/RC oscillation selection jumper is used to select the operation by ceramic oscillation or by RC oscillation. For the operation by ceramic oscillation, set four jumper wires up (to XT). For the operation by RC oscillation, set four jumper wires down (to RC).

③ AMP/TR selection jumper
To amplify the analog signal output from AOUT by the amplifier IC (MSC1157) on the board, set three jumpers up (to AMP). To amplify by the transistor, set three jumpers down (to TR).

④ 20-pin connector
Signals necessary for operation using the microcontroller are connected to the 20-pin connector. Connector pin assignment is as follows:

Connector pin No.	Signal	Connector pin No.	Signal
1	V_{DD}	11	I5/A2
2	V_{DD}	12	XT/$\overline{CR}$
3	V_{DD}	13	NC
4	CPU/$\overline{STD}$	14	$\overline{RESET}$
5	NC	15	$\overline{ST/RND}$
6	I0/SW0	16	OSC3
7	I1/SW1	17	NAR/$\overline{BUSY}$
8	I2/SW2	18	GND
9	I3/A0	19	GND
10	I4/A1	20	GND

⑤ Address setting switch
When used in stand-alone mode, select a playback word using this HEX switch. 0-7 in this HEX switch correspond to A0-A2 in binary data. When a microcontroller is used, set the HEX switch to 0.

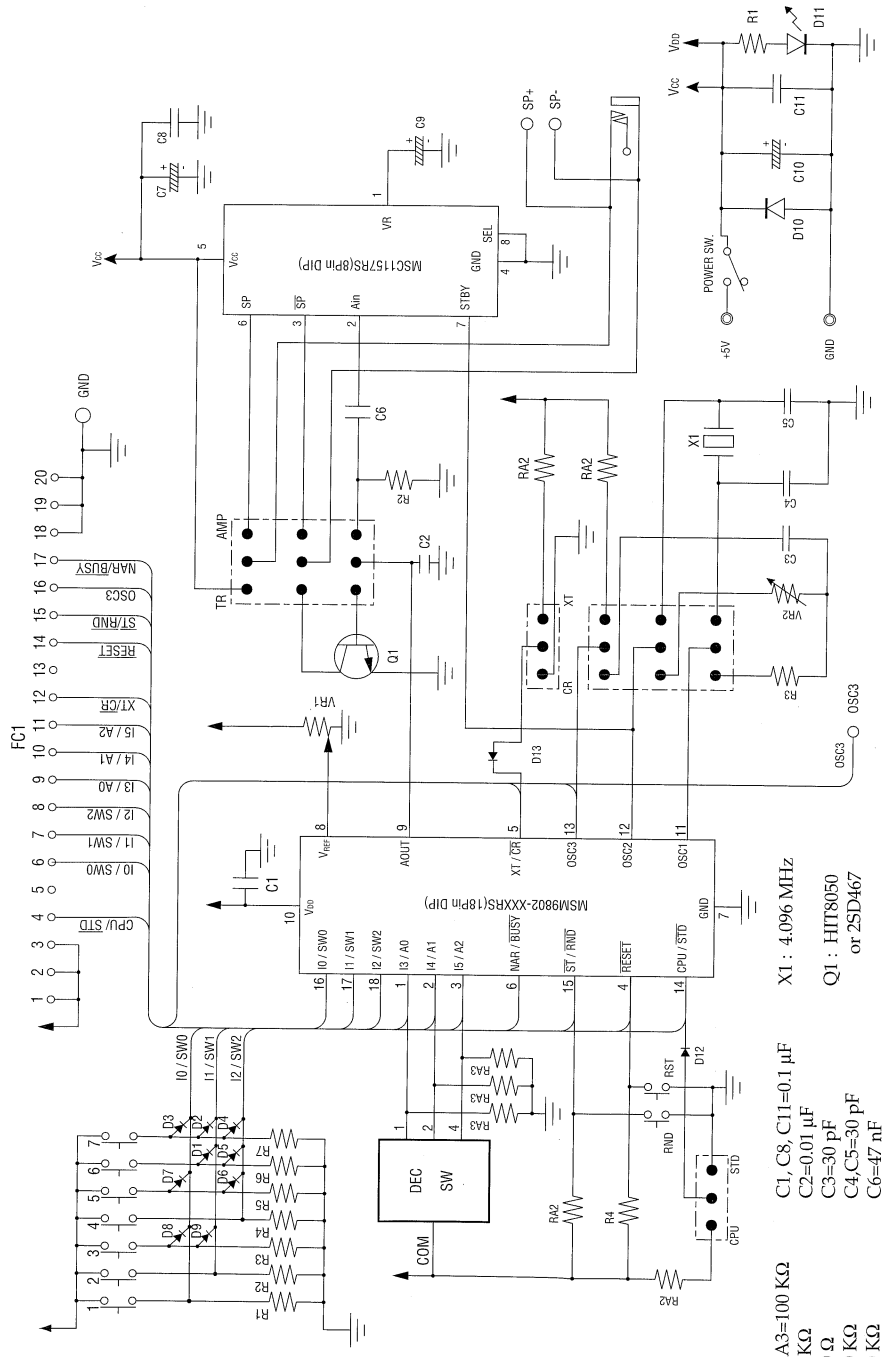
⑥ Frequency check pin (OSC3)
This pin is used to monitor the oscillation frequency of RC oscillation.

⑦ Variable resistor (VR2) for adjusting the frequency of RC oscillation.
This variable resistor can change the frequency of RC oscillation. When the resistor is turned clockwise, the frequency decreases. When the resistor is turned counterclockwise, the frequency increases. The frequency can be monitored by the check pin of ⑥. Adjust the oscillation frequency to 256 kHz normally.

⑧ GND pin

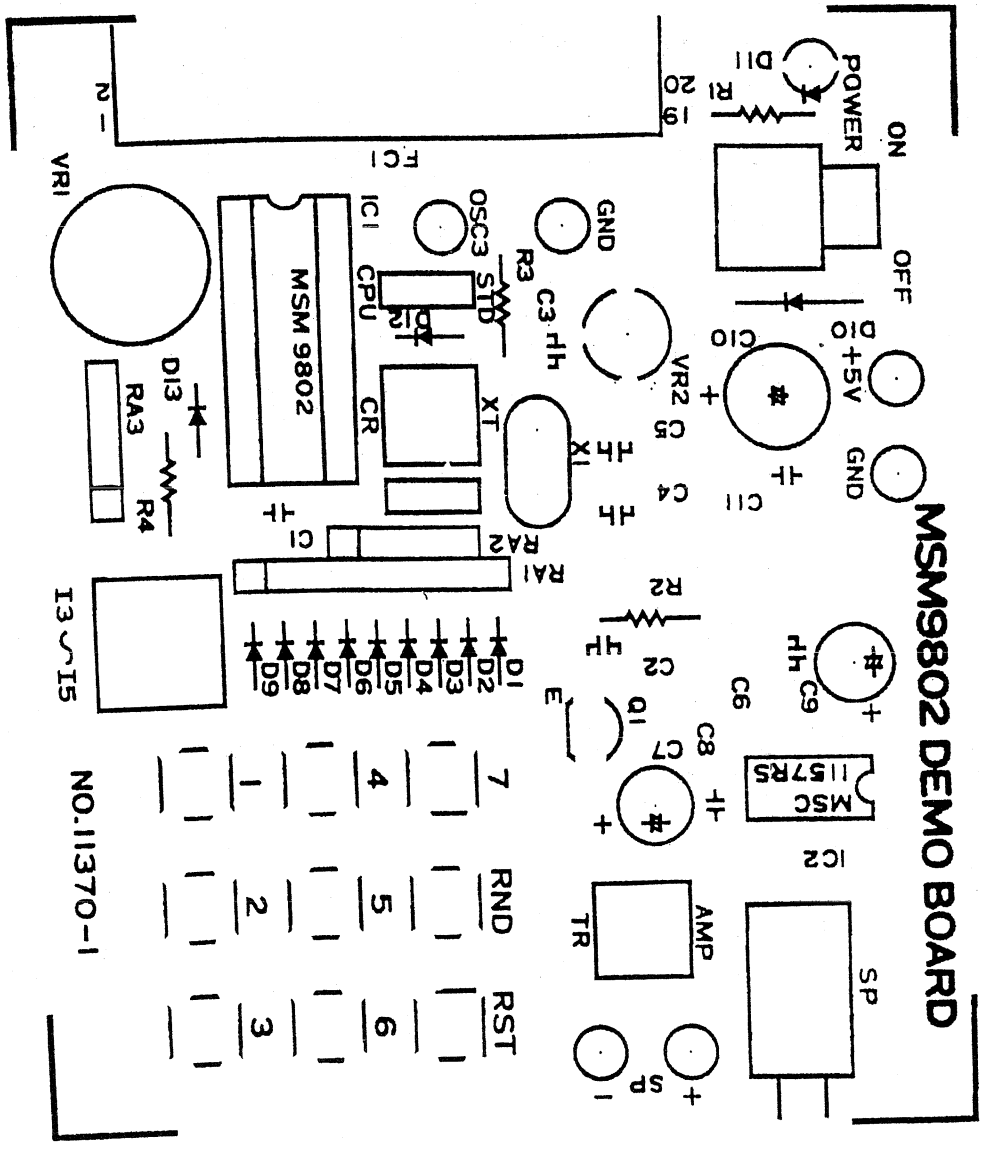
⑨ Speaker output volume (VR1 used on a common base by AMP/TR)
This volume is used to adjust the sound level. When the VR is turned counterclockwise, the sound turns down. The V_{REF} pin is used for sound volume adjustment. For the maximum sound volume, the GND level is input to the V_{REF} pin. For the minimum sound volume, the V_{DD} level is input.

⑩ Playback SW input interface
When the stand-alone mode is used, press the 1-7 switches to playback voices corresponding to 1-7 of SW2-SW0. Press the RND switch on the center (random voice playback switch) to playback a voice randomly selected from 15 phrases corresponding to A0, SW2-SW0.
If the RND switch is pressed immediately after power on or RESET signal input, the voice of the first phrase is played back first, then a random phrase is generated in the second time onward.

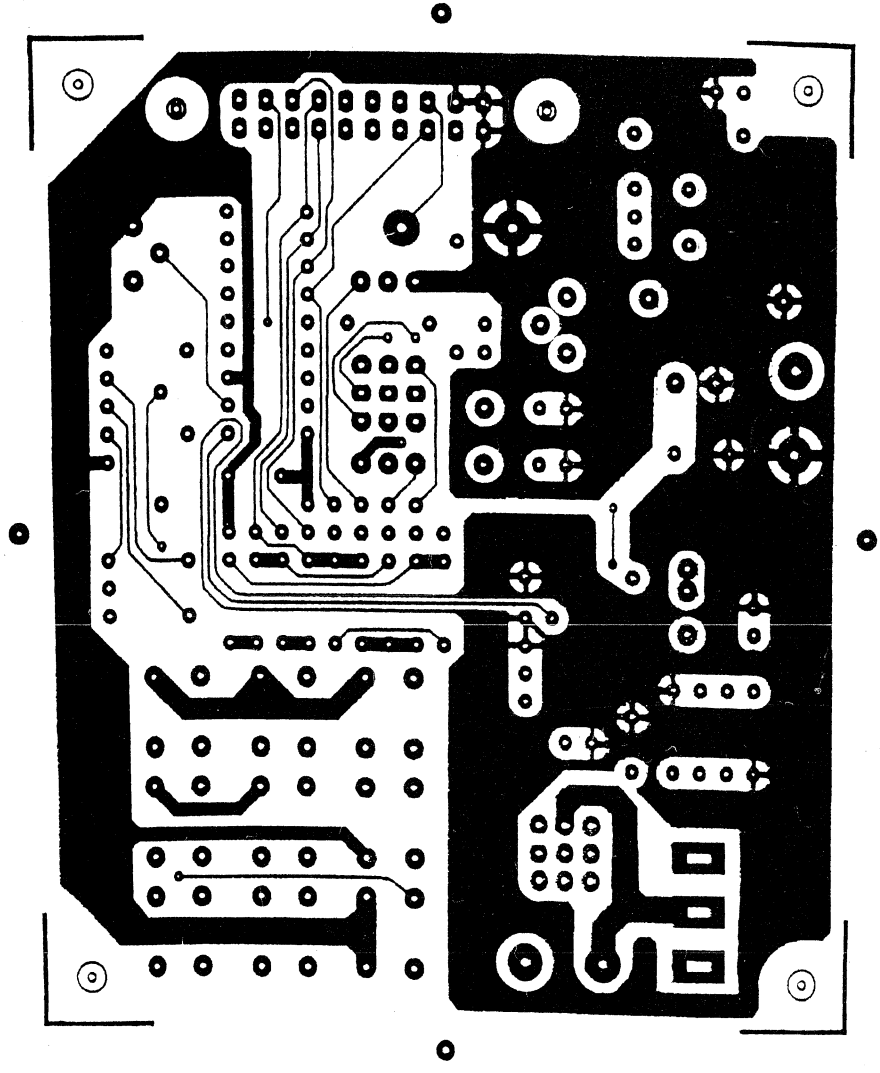

MSC1157RS(8Pin DIP)
MSM9802-XXXRS(18Pin DIP)
FC1
AMP
DEC SW
COM
POWER SW.
+5V
GND
Vcc
VDD
SP+
SP-
RA1~RA3=100 KΩ
R1=5.1 KΩ
R2=240 Ω
R3=150 KΩ
R4=100 KΩ
VR1, VR2=100 KΩ
C1, C8, C11=0.1 µF
C2=0.01 µF
C3=30 pF
C4,C5=30 pF
C6=47 nF
C7=10 µF
C9=4.7 µF
C10=220 µF
X1 : 4.096 MHz
Q1 : HIT8050
or 2SD467
D10 : 10D1

DEMONSTRATION BOARD LAYOUT

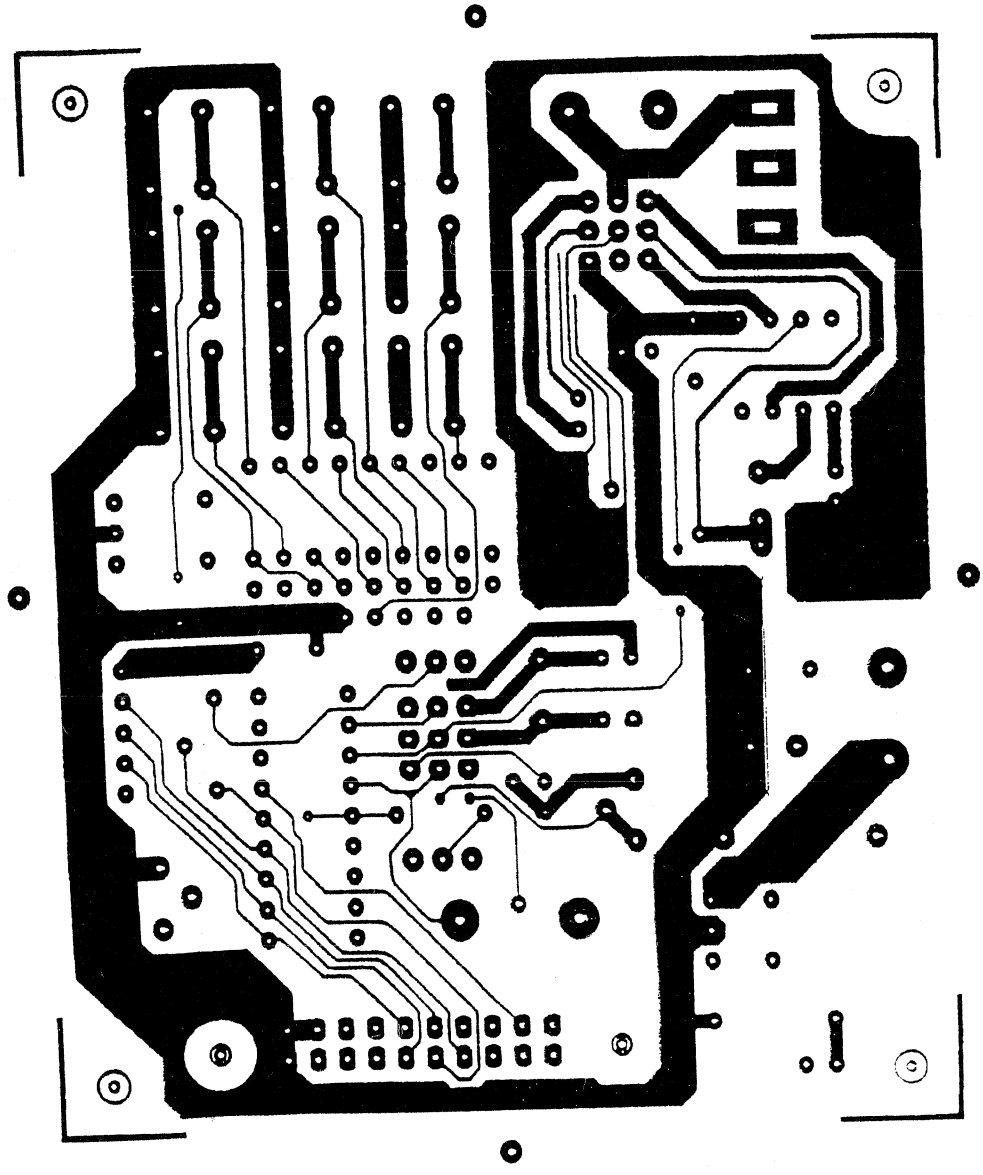
Silk Drawing



Component side



Solder Side



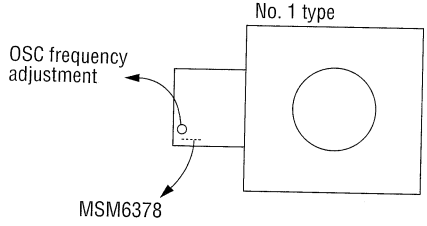
OKI Semiconductor

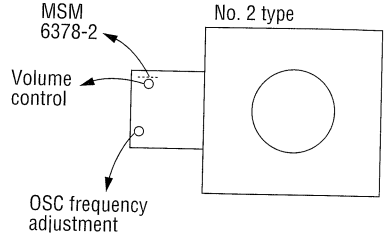
MSM6378A DEMO BOARD

MSM6378A Demonstration Board

There are two types of MSM6378A (OTP ROM built-in voice synthesis IC) demonstration boards. The demonstration board using a transistor as a speaker amplifier is the No. 1 type and the board using MSC1191 is the No. 2 type. (Only No. 2 types are being manufactured at present.)

BOARD DESIGN





VOICE REPRODUCTION PROCEDURE

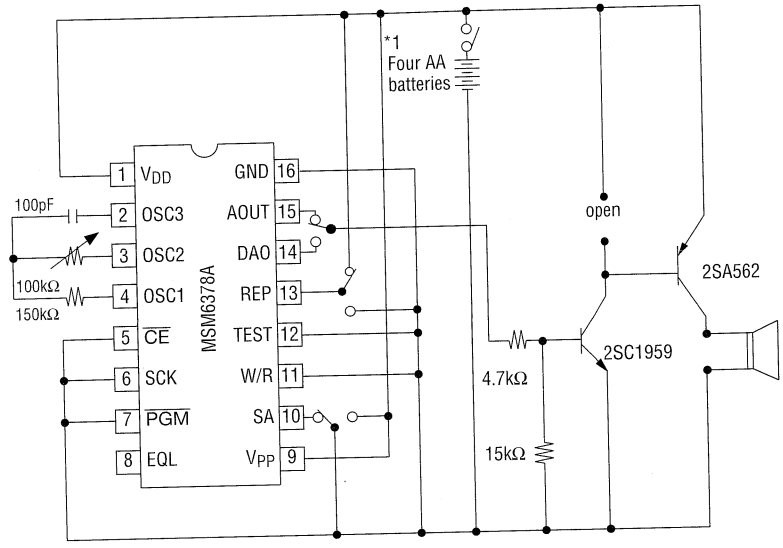
When the power switch is pressed, the voice is output repeatedly.

SPECIFICATIONS

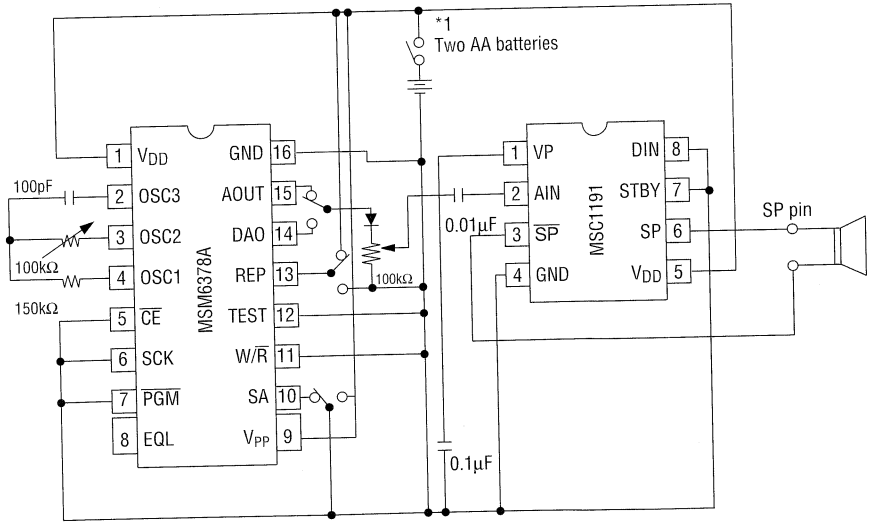
- Power source:
  No. 1 type: ..... Four AA batteries
  No. 2 type: ..... Two AA batteries
  (The guaranteed power supply range for accurate reproduction through the internal LPF is from +2.7V to +5.5V.)
- Sampling frequency: 8 kHz
- Pin option:
  Repeated output: ..... REP = H
  Output pin: ..... AOUT (LPF output)
- Power amplifier:
  No. 1 type: ..... 2 transistors,
  No. 2 type: MSC1191
- Speaker: 8Ω, 2W

CIRCUIT DIAGRAM

No. 1 Type



No. 2 Type



*1 The guaranteed voltage of LPF output of MSM6378 ranges from 2.7V to 5.5V.

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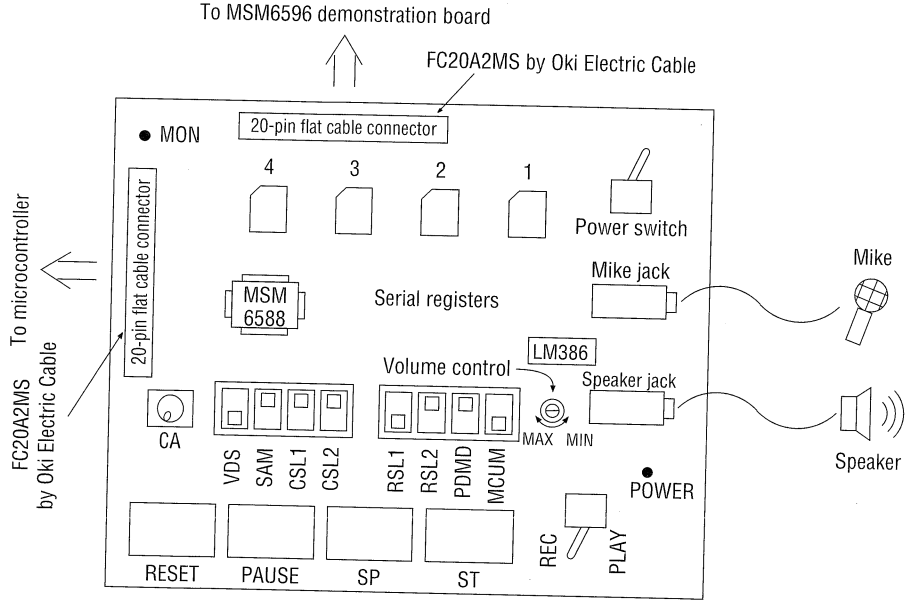
MSM6588 DEMO BOARD

MSM6588 Demonstration Board

BOARD DESIGN



CONDITIONS SETTING PROCEDURE

Set the recording conditions with the two DIP switches and one rotary switch. After setting the switches, recording for 85 seconds can be done using the two serial registers of 1M-bit at 8 kHz sampling (3-bit ADPCM 8 kHz sampling).

1. Set MCUM of the DIP switch to OFF.
   The MSM6588 enters the stand-alone mode. (When the MCUM is set to ON the MSM6588 enters the microcontroller interface mode.)

2. Set RSL1 and RSL2 of the DIP switches as shown in the table below depending on the number of serial registers mounted.

RSL2	OFF		ON	
RSL1	OFF	ON	OFF	ON
Number of serial registers	256K or 512K-bit 1pc.	1M-bit 1pc.	1M-bit 2pcs.	1M-bit 4pcs.

3. Specify the control mode and channel number for recording by CSL1 and CSL2 of the DIP switch.

CSL2	OFF		ON	
CSL1	OFF	ON	OFF	ON
Control mode	Fixed mode			Fixed mode
Number of channels	8-word	4-word	2-word	8-word

Fixed mode:

The recording time of each channel is the time equivalent of the memory capacity equally divided by the memory capacity of the external serial registers and the number of channels.

The recording of each channel can be obtained from the following equations.

$$\text{Recording time} = \frac{1.024 \times 1024\ (\text{K bit}) \times \text{Number of serial registers}}{\text{Sampling frequency (kHz)} \times 3\ (\text{bit}) \times \text{Number of channels}}\ (\text{sec})$$

For example, the recording time for each channel with two serial registers on two channels at the sampling frequency of 8 kHz (RSL1=OFF, RSL2=ON, CSL1=OFF, CSL2=ON and SAM=ON) is as shown below.

$$\text{Recording time} = \frac{1.024 \times 1024\ (\text{K bit}) \times 2}{8\ (\text{kHz}) \times 3 \times 2} \fallingdotseq 44\ (\text{sec})$$

Flex mode:

The recording time of each channel becomes available within the range of the memory capacitor for the external serial registers and is recorded to ch0, ch1, ... and ch7.

4. Set the rotary switch (CA) to the channel to be recorded.

CA	Fixed Mode			Flex Mode
	8-word	4-word	2-word	8-word
0	ch0	ch0	ch0	ch0
1	ch1			ch1
2	ch2	ch1		ch2
3	ch3			ch3
4	ch4	ch2	ch1	ch4
5	ch5			ch5
6	ch6	ch3		ch6
7	ch7			ch7

5. Specify the sampling frequency at SAM of the DIP switch.

SAM	OFF	ON
Sampling frequency f_{samp}	$\frac{f_{osc}}{768}$ (5.3 kHz)	$\frac{f_{osc}}{512}$ (8.0 kHz)

The frequencies within the parentheses are at the original oscillation f_{OSC}=4.096 MHz.

6. Set the PDMD of the DIP switch to ON.

OFF: The MSM6588 enters the power-down state except recording and playback.
ON: The MSM6588 always enters the stand-by state. The time lag up to starting the playback decreases after input.

7. Select whether or not the voice is activated by VDS with the DIP switch.

OFF: Ordinary mode, the voice is not activated.
ON: The voice is activated.

Note: When the activation of the voice is required, use the DC stabilized power supply without using the battery driving power. In the case of the battery, the power fluctuation of a few mV in starting the recording is amplified and results in determining that there is sound.

RECORDING PROCEDURE

1. Turn the toggle switch on the upper right of the demonstration board to ON to engage power. The LED on the lower left of the demonstration board lights.

2. Set the conditions as specified in the Conditions Setting Procedure section.

3. Set the toggle switch on the lower right of the demonstration board to REC to select the recording mode.

4. Press the ST button and record the voice via the mike. During recording, the LED (MON) on the demonstration board lights.

5. When the voice is recorded to the last of the channel memory, the recording automatically finishes. To stop recording halfway through, press the SP button.

PLAYBACK PROCEDURE

1. Set the toggle switch on the lower right of the demonstration board to PLAY to select the playback mode.

2. Press the ST button to start the playback. During the playback, the LED (MON) comes on.

3. When the playback is complete, the recording is automatically terminated. To stop the playback halfway through, press the SP button again.

4. Use the volume control to adjust the playback volume.

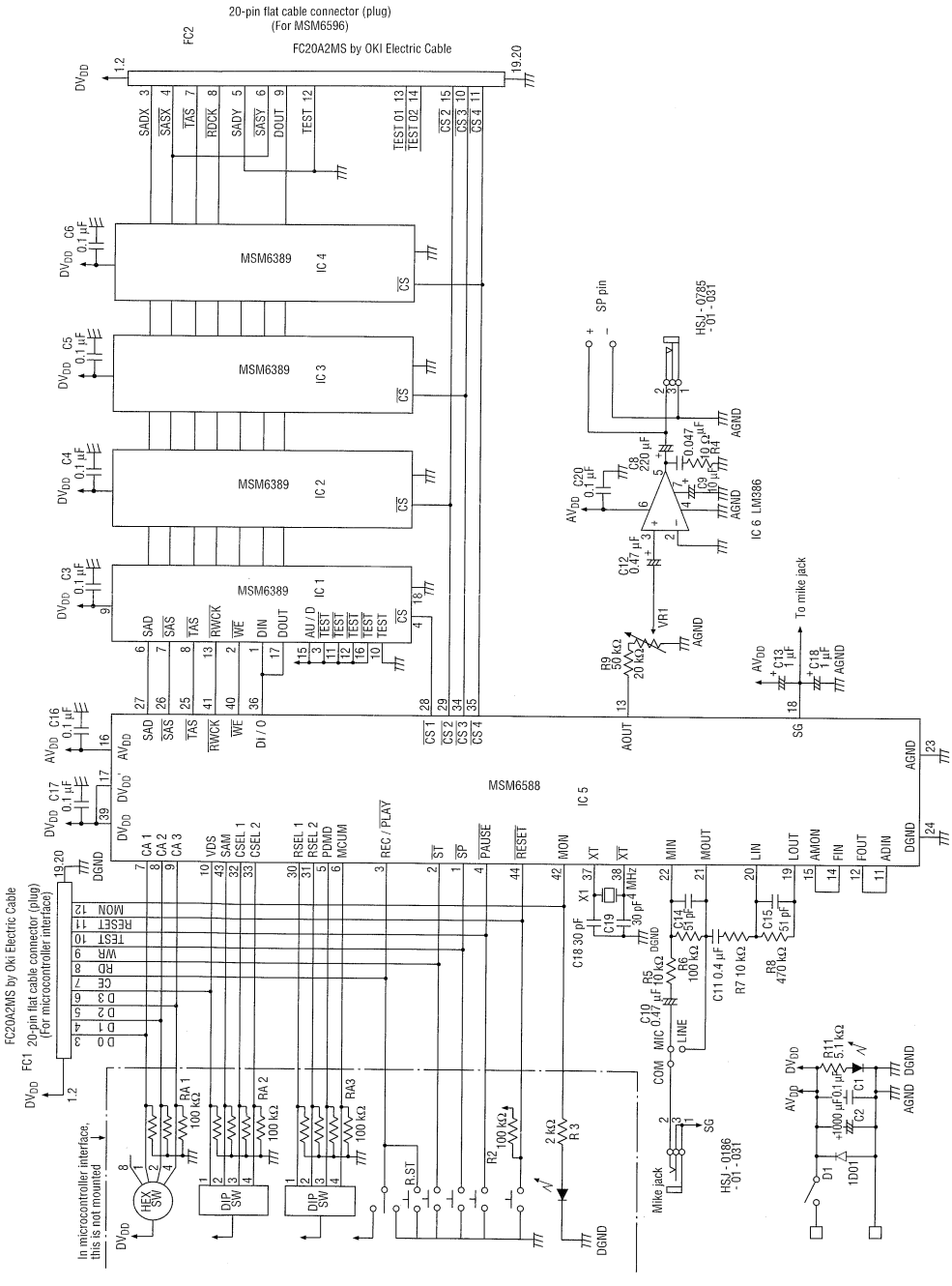
PAUSE PROCEDURE OF RECORD/PLAYBACK

1. When the PAUSE button is pressed during record/playback, the record/playback pauses.

2. Press the ST button again, and the playback starts again.

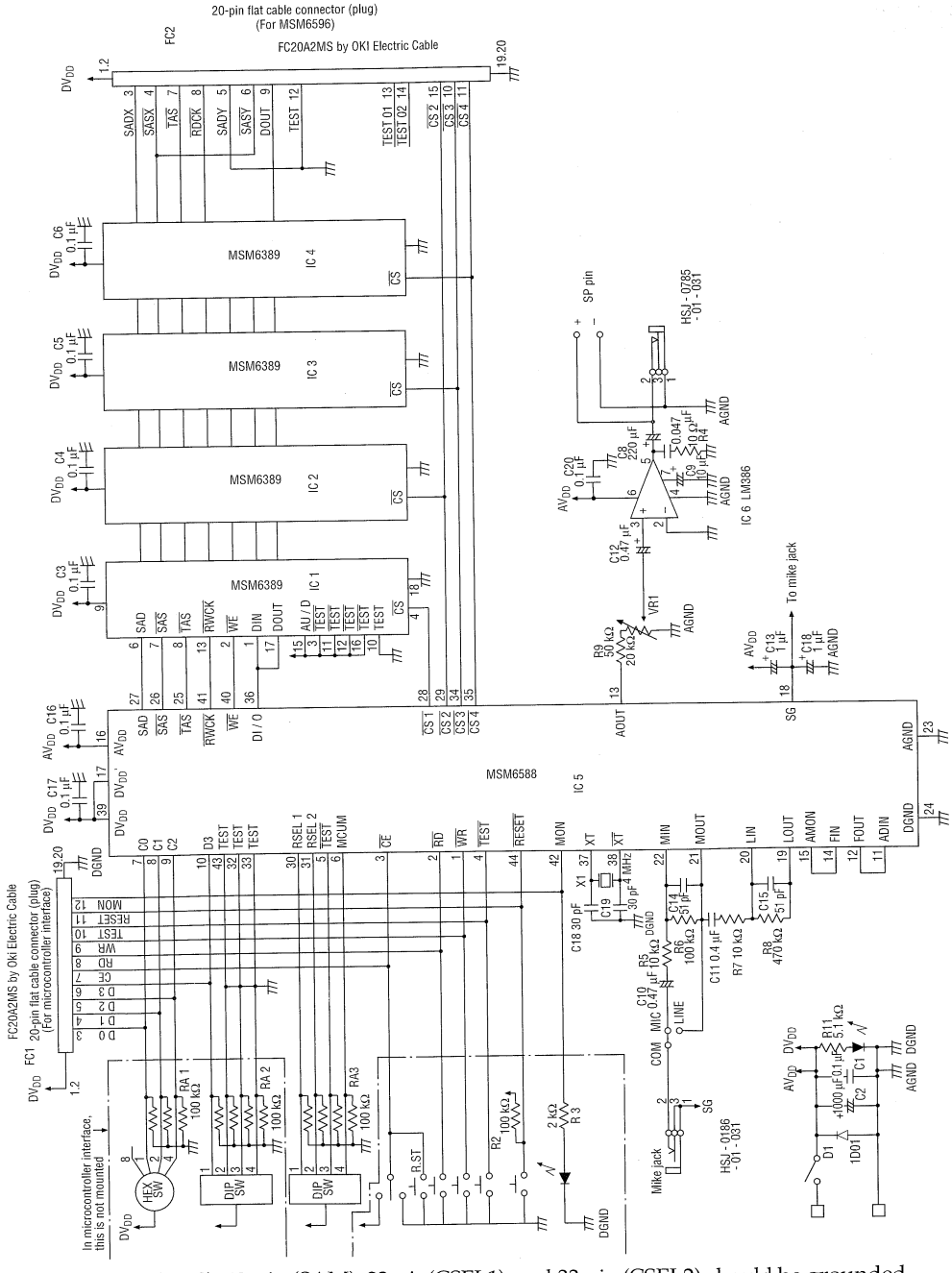
CIRCUIT DIAGRAMS

Stand-alone Type



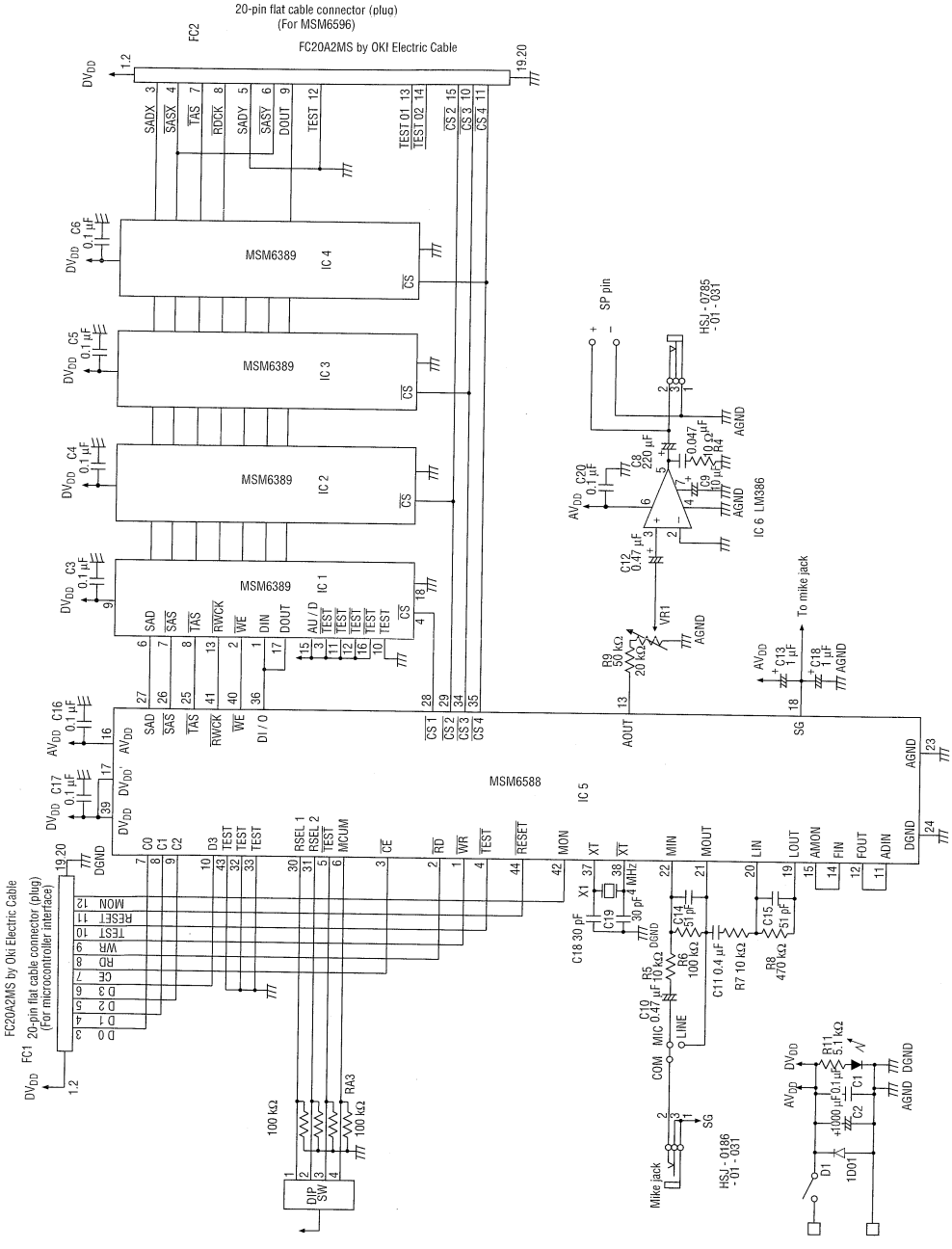
Microcontroller Interface Mode

Change method for microcontroller interface mode



Note: 10-pin (VDS), 43-pin (SAM), 32-pin(CSEL1), and 33-pin (CSEL2) should be grounded.

Microcontroller Type



SETTING PROCEDURE OF CONDITIONS (Microcontroller Type)

Set the recording conditions by one DIP switch.

Set the RSL1 and RSL2 of DIP switch as listed below according to the number of serial registers to be mounted.

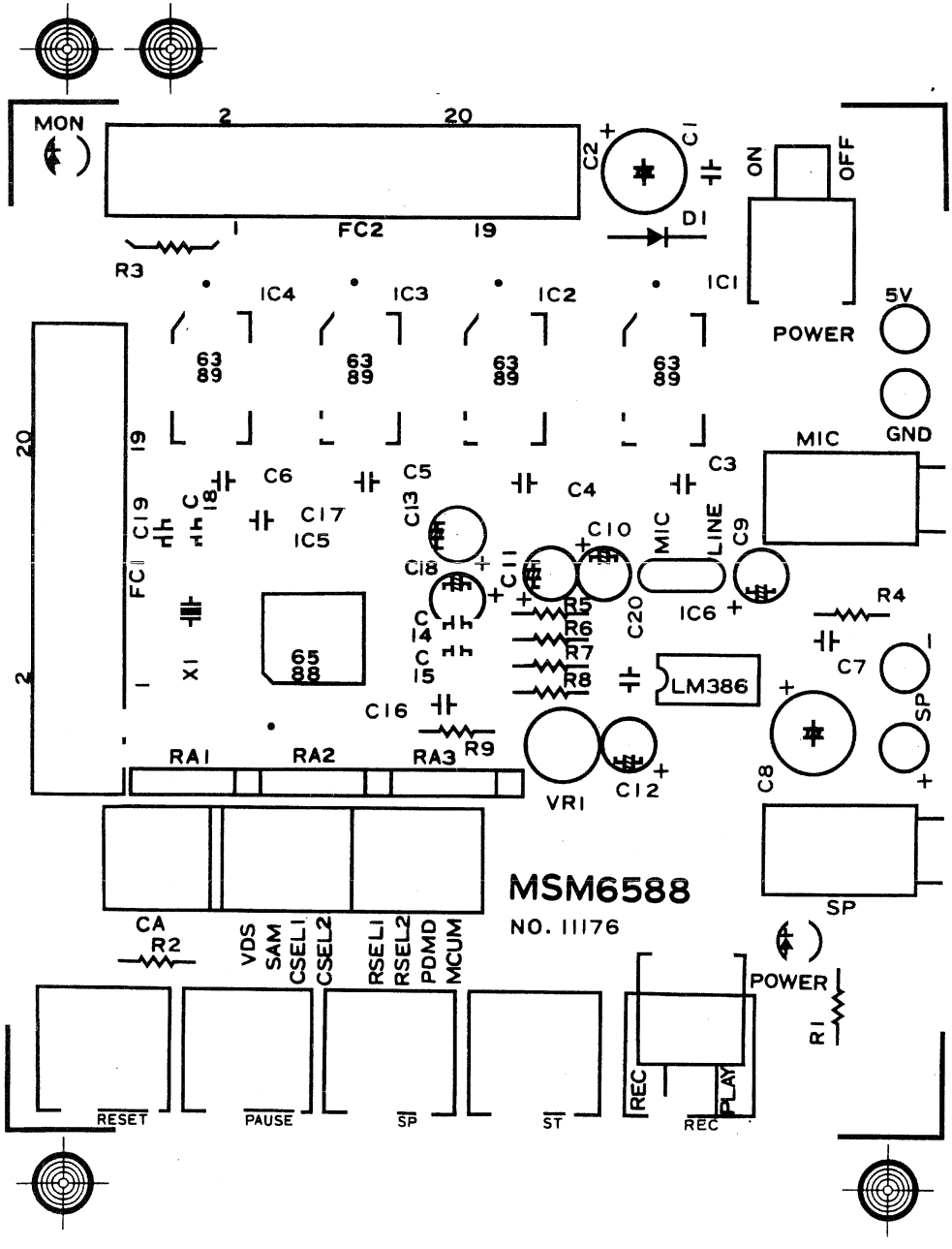
RSL2	OFF		ON	
RSL1	OFF	ON	OFF	ON
Number of Serial Registers	256Kbits or 512Kbits 1 piece	1Mbits 2 pieces	1Mbits 3 pieces	1Mbits 4 pieces

Set the PDMD of DIP switch to ON side.

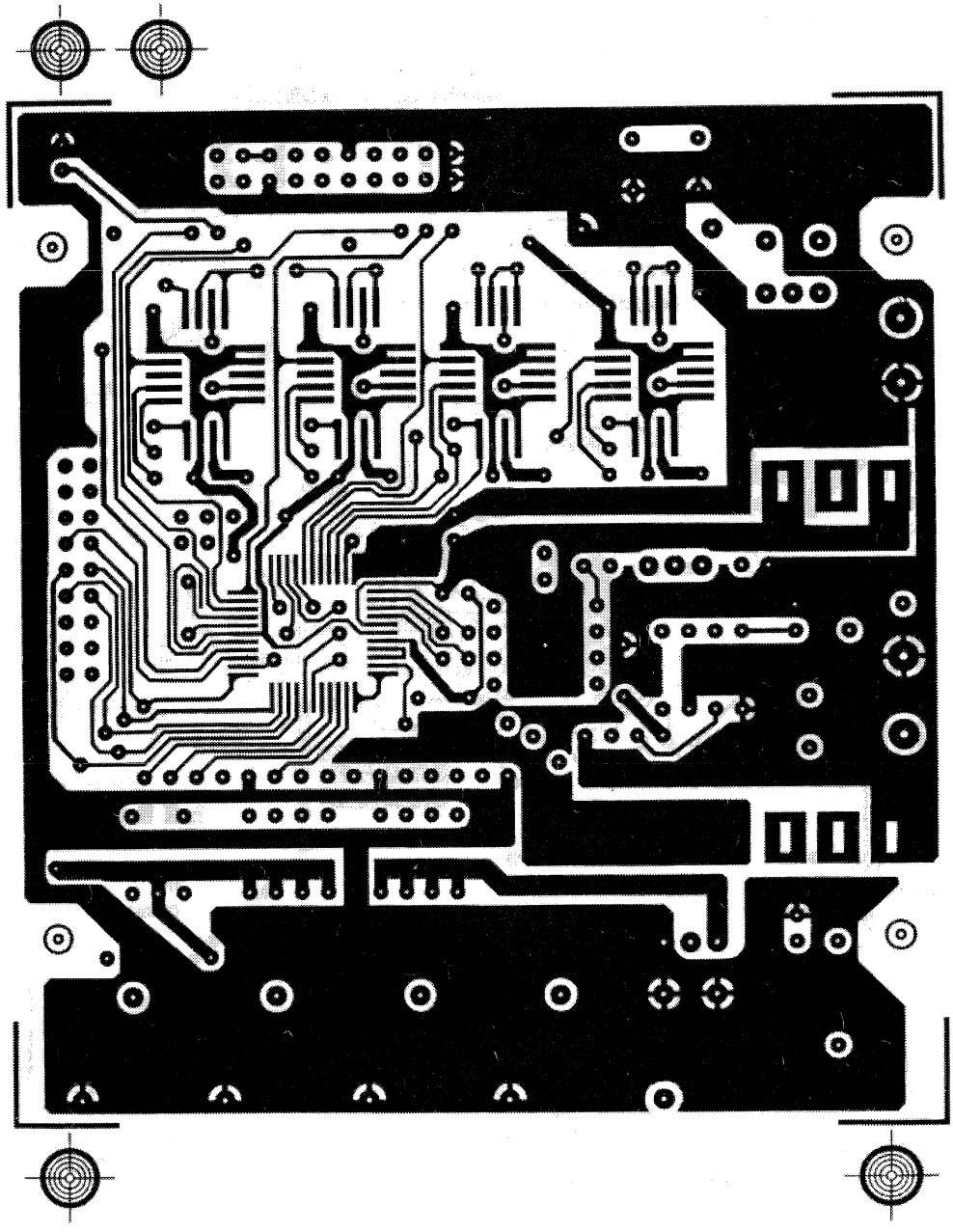
Set the MCUM of DIP switch to NO side.

PATTERN LAYOUT

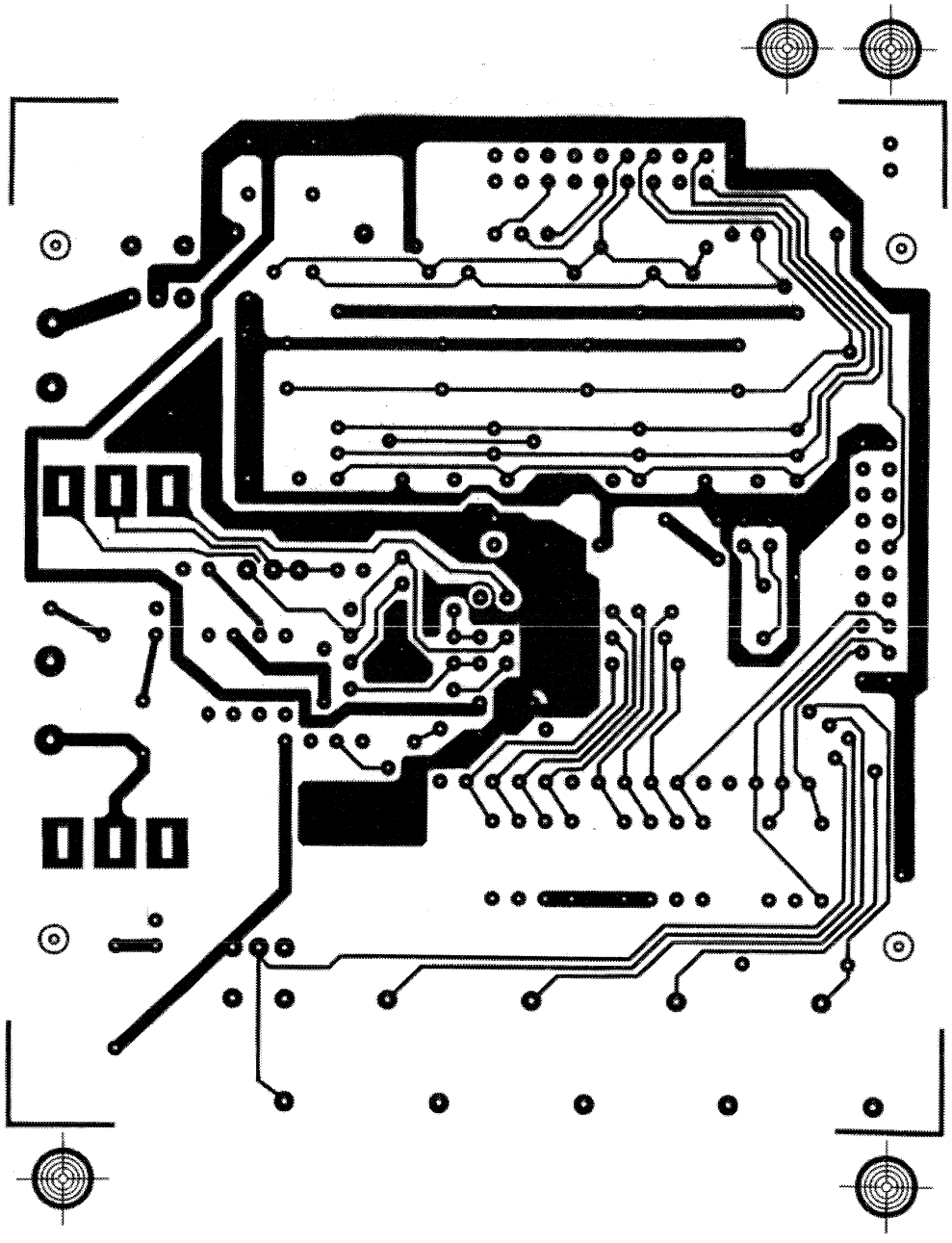
Silk Screen



Mounting Side



Solder Side

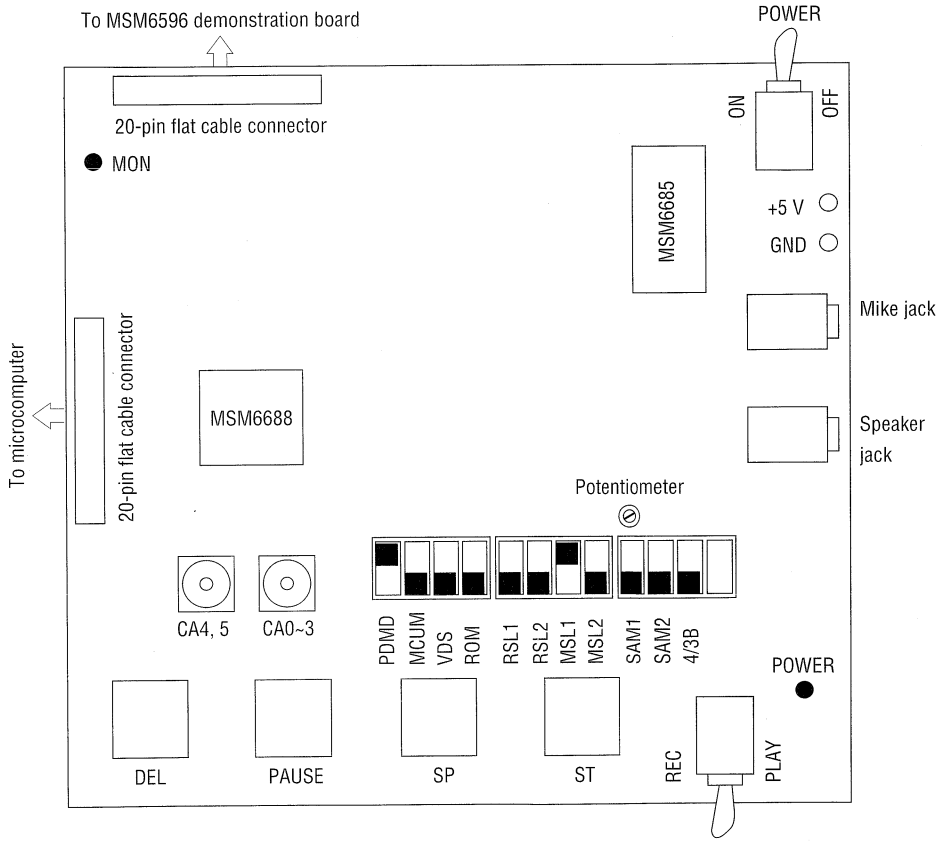


OKI Semiconductor

MSM6688 DEMO BOARD

MSM6688 Demonstration Board

BOARD DESIGN



CONDITION SETTING

Two HEX switches and three DIP switches are used to set recording conditions.

1. Normally, turn on dip switch PDMD.
   OFF: The device is automatically turned off except for recording and playback.
   ON : The device is not turned off and is on standby except for recording and playback.

2. Turn off dip switch MCUM.
   OFF: Sets up the stand-alone mode.
   ON : Sets up the microcomputer interface mode. (Note)

Note: The microcomputer interface mode cannot be set up merely by turing on dip switch MCUM. Refer to the section of "WHEN USINGIN MICROCOMPUTER INTERFACE MODE" when using this demonstration board in microcomputer interface mode.

3. Use dip switch VDS to specify whether to initiate with voice.
   OFF: Normal mode where recording is not initiated with voice
   ON : Voice initiation

Note: Voice initiation requires the use of a regulated power supply instead of a battery. When a battery is used, the voltage variation of several mV during the start of recording is amplified and, thus, results in voice detection.

4. Turn off dip switch ROM.
   OFF: Sets up the recording and playback mode.
   ON : Sets up the ROM playback mode.

5. Use dip switches RSL1 and RSL2 to set the number of serial registers to be connected externally.

RSL2	OFF	OFF	ON	ON
RSL1	OFF	ON	OFF	ON
Number of serial registers	1	2	3	4

6. Turn on dip switch MSL1 and turn off MSL2.

7. Use dip switches SAM1 and SAM2 to select the sampling frequency.

SAM2	SAM1	Sampling frequency
OFF	OFF	f_{OSC}/1024 (4.0 kHz)
OFF	ON	f_{OSC}/768 (5.3 kHz)
ON	OFF	f_{OSC}/640 (6.4 kHz)
ON	ON	f_{OSC}/512 (8.0 kHz)

* A value in parentheses is applied when f_{OSC} is 4.096 MHz.

8. Use dip switch 4/3B to select the bit rate.
   OFF: 3-bit ADPCM
   ON : 4-bit ADPCM

9. Use the HEX switch (CA) to select a channel for recording and specify a phrase.

CA4, 5	CA0~3	Phrase number	Remarks
0	0	Ch 00	For deletion of all phrases
0	1 : F	Ch 01 : Ch 0F	Applicable to recording and playback, and to ROM playback (63 phrases)
1	0 : F	Ch 10 : Ch 1F	
2	0 : F	Ch 20 : Ch 2F	
3	0 : F	Ch 30 : Ch 3F	

RECORDING

1. Turn on the power switch. The LED (POWER) on the demonstration board lights.
2. Set HEX switches CA4, 5 and CA0-3 at "00".
3. Press the DEL button to delete all phrases.
4. Set conditions according to the above condition setting.
5. Place the REC/PLAY switch in the REC position to set up the recording mode.
6. Press the ST button to record voice through the mike.
7. Upon the exhaustion of the whole memory capacity, recording is terminated automatically. To suspend recording, press the SP button.

Note: If the whole memory capacity has been used for recording, the other phrases cannot be recorded.

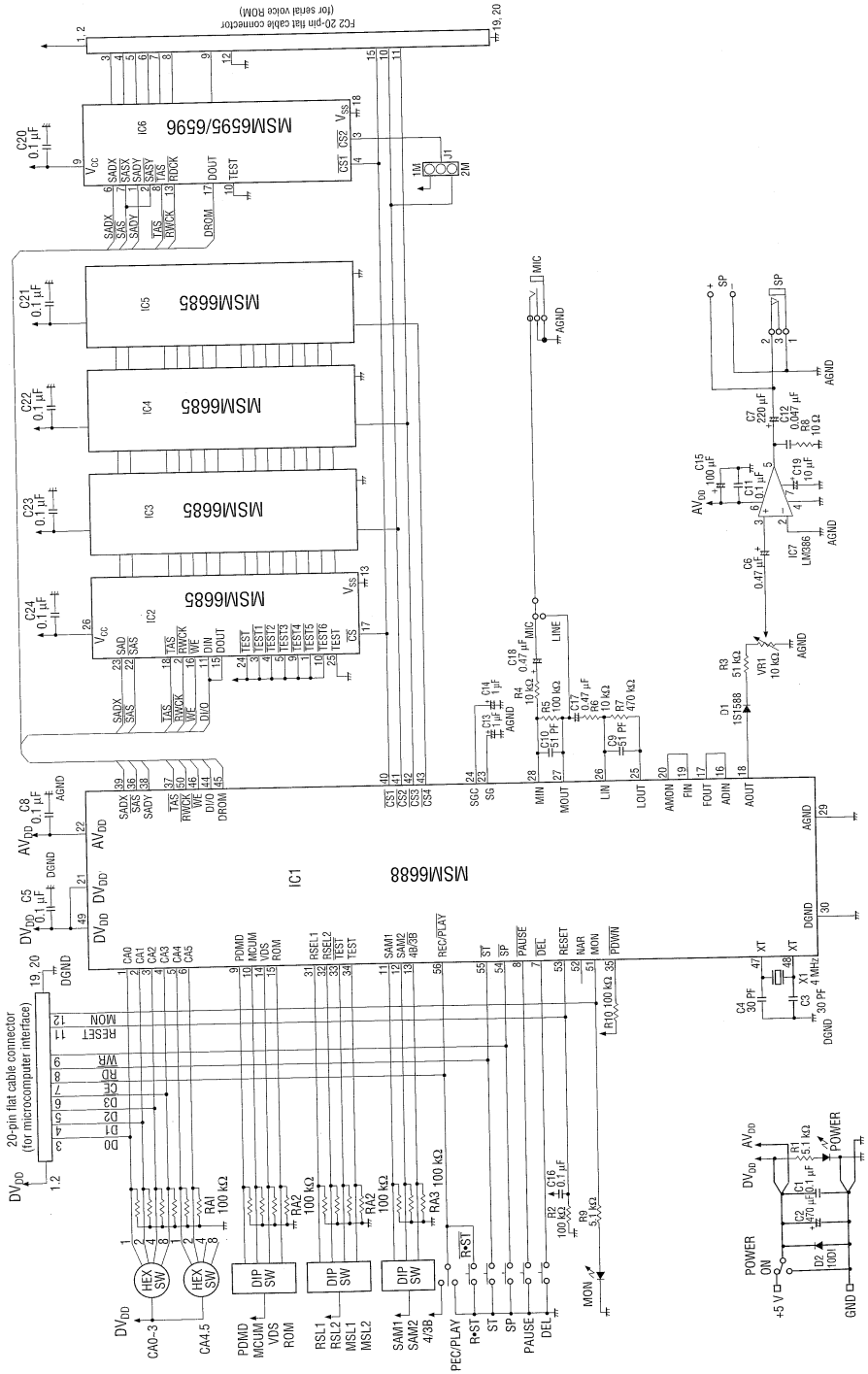
PLAYBACK

1. Place the REC/PLAY switch in the PLAY position to set up the playback mode.
2. Pressing the ST button starts playback. During playback, the LED (MON) is lit.
3. The playback of a whole recording results in automatic termination. To suspend playback, press the SP button.
4. The volume of playback can be adjusted by the potentiometer.

SUSPENDING RECORDING AND PLAYBACK

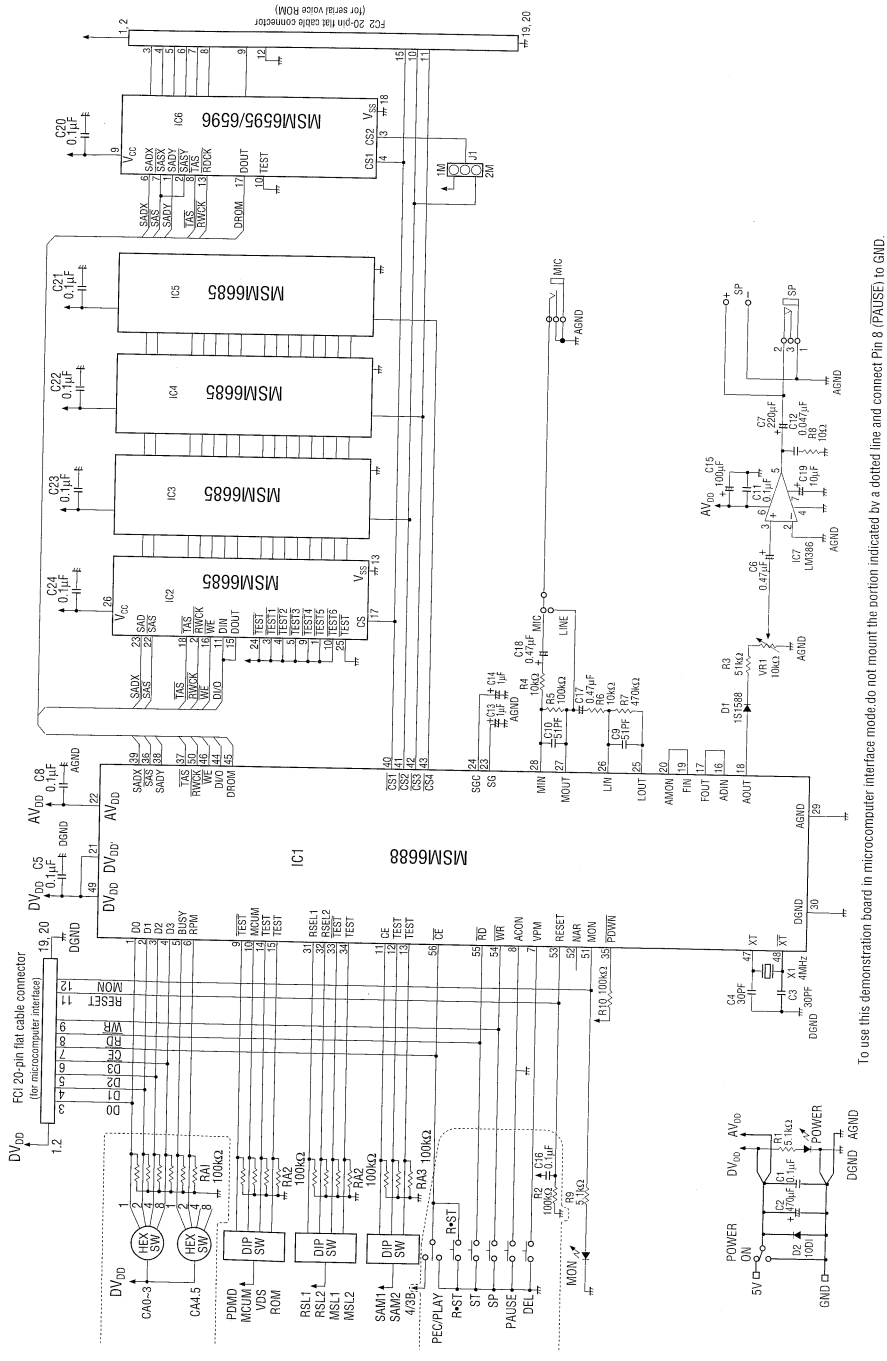
1. Pressing the PAUSE button during recording or playback causes the recording or playback to be suspended.
2. Pressing the ST button restarts recording and playback.

CIRCUIT DIAGRAM

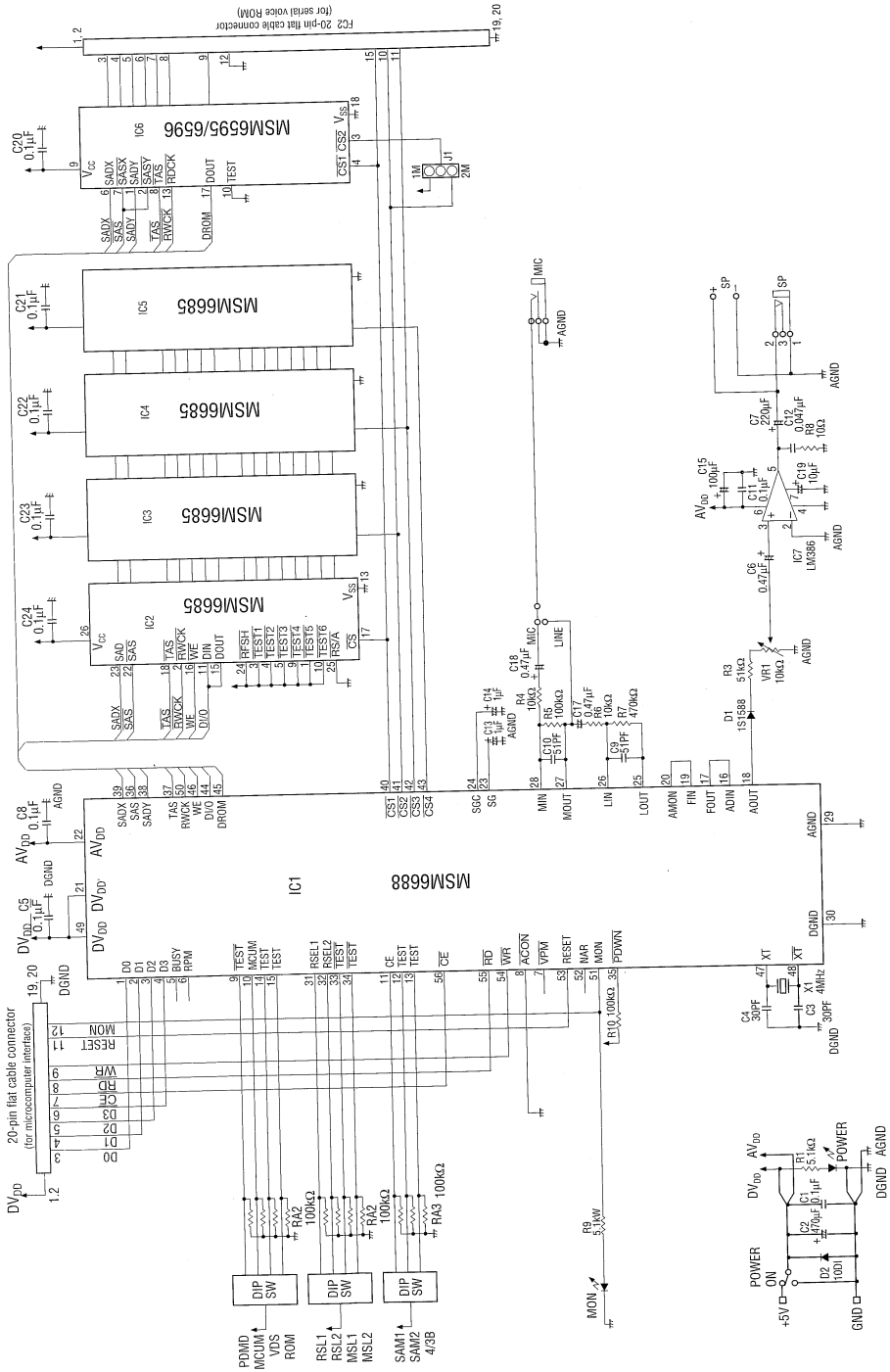


WHEN USING IN MICROCOMPUTER INTERFACE MODE

How to Change Setting from stand-alone Mode to Microcommputer Interface Mode



Circuit Diagram(Microcomputer Interface Mode)



Condior Setting

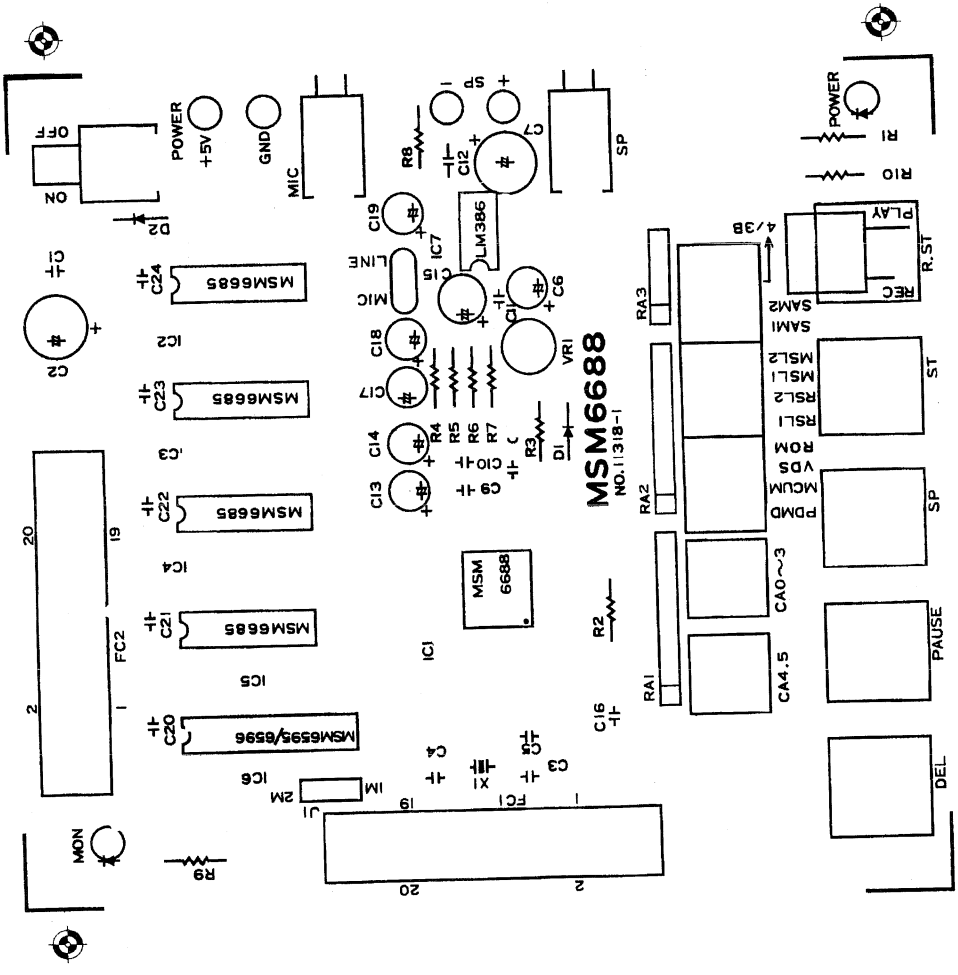
Three DIP switches are used to set recording conditions.
Turn on dip switch PDMD.
Turn on dip switch MCUM.
OFF: Sets up the stand-alone mode.
ON: Sets up the microcomputer interface mode.
Turn off dip switch VDS.
Turn off dip switch ROM.
Use dip switches RSL1 and RSL2 to set the number of serial registers to be connected externally.

RSL2	OFF	OFF	ON	ON
RSL1	OFF	ON	OFF	ON
Number of serial registers	1	2	3	4

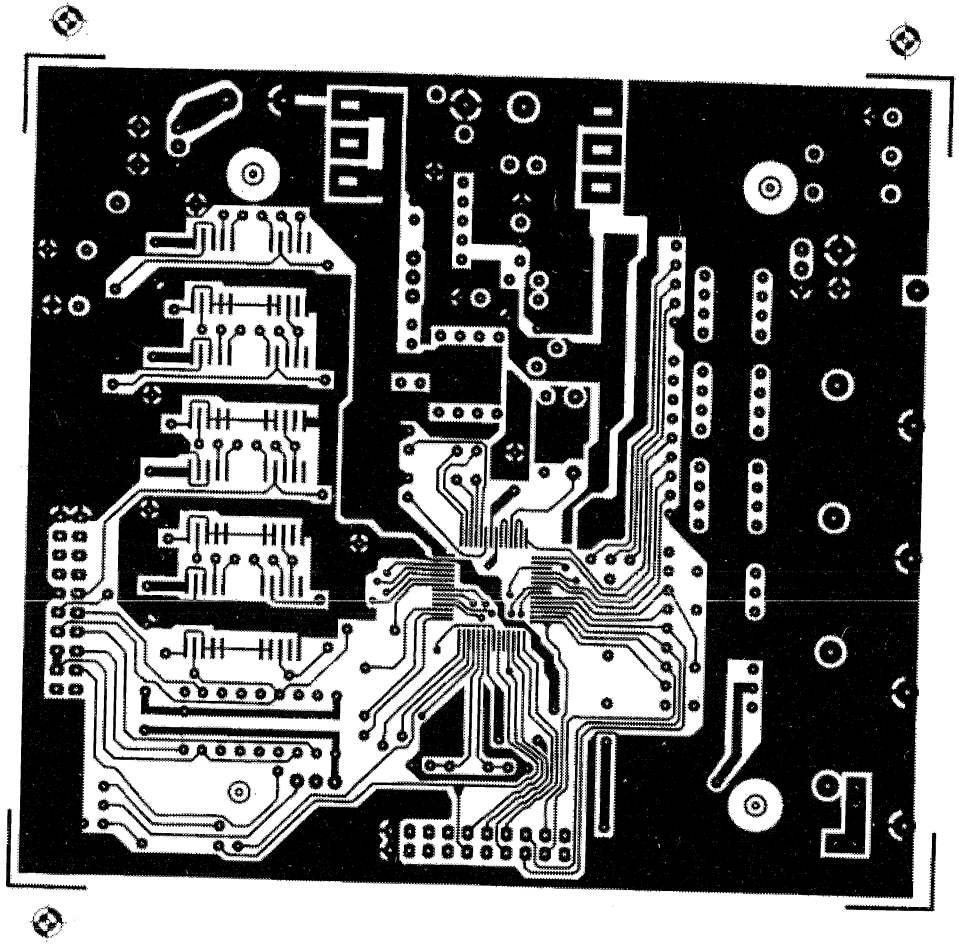
Turn on dip switch MSL1 and turn off MSL2
Turn on dip switch SAM1 and turn off dip switch SAM2.
Turn off dip switch 4/3B.

PATTERN LAYOUT

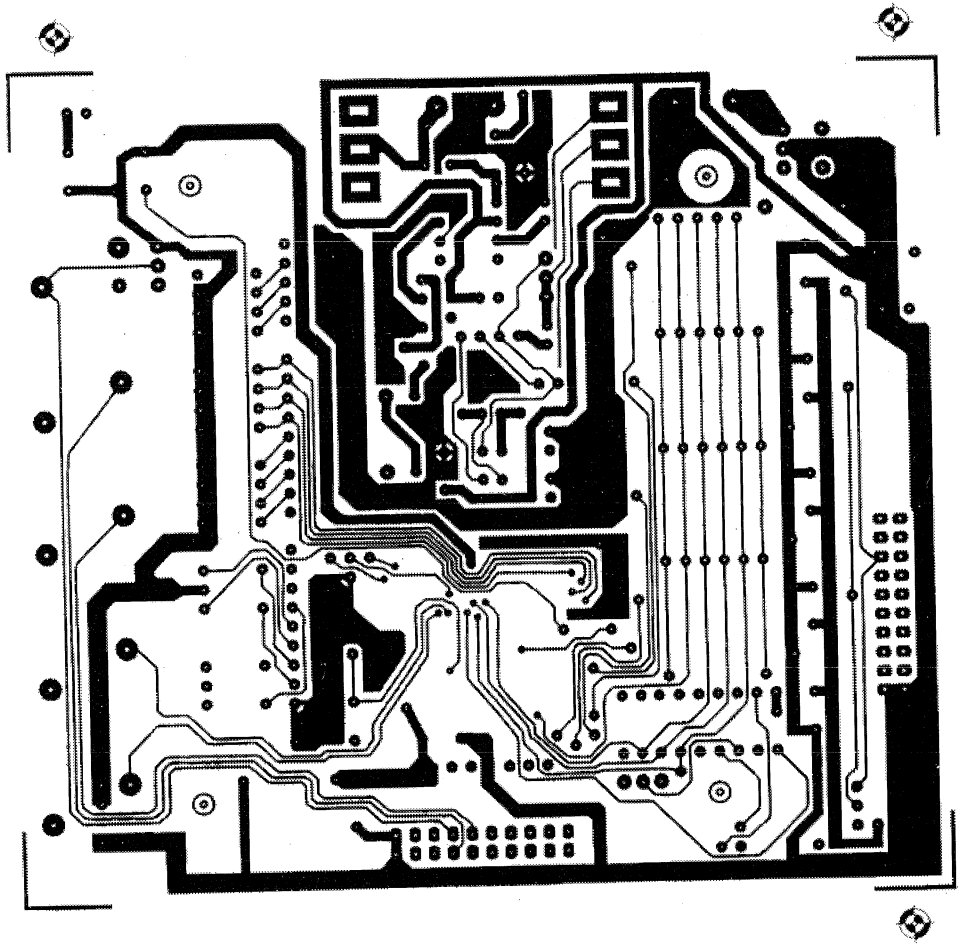
Silk Screen



Mounting Side



Solder Side

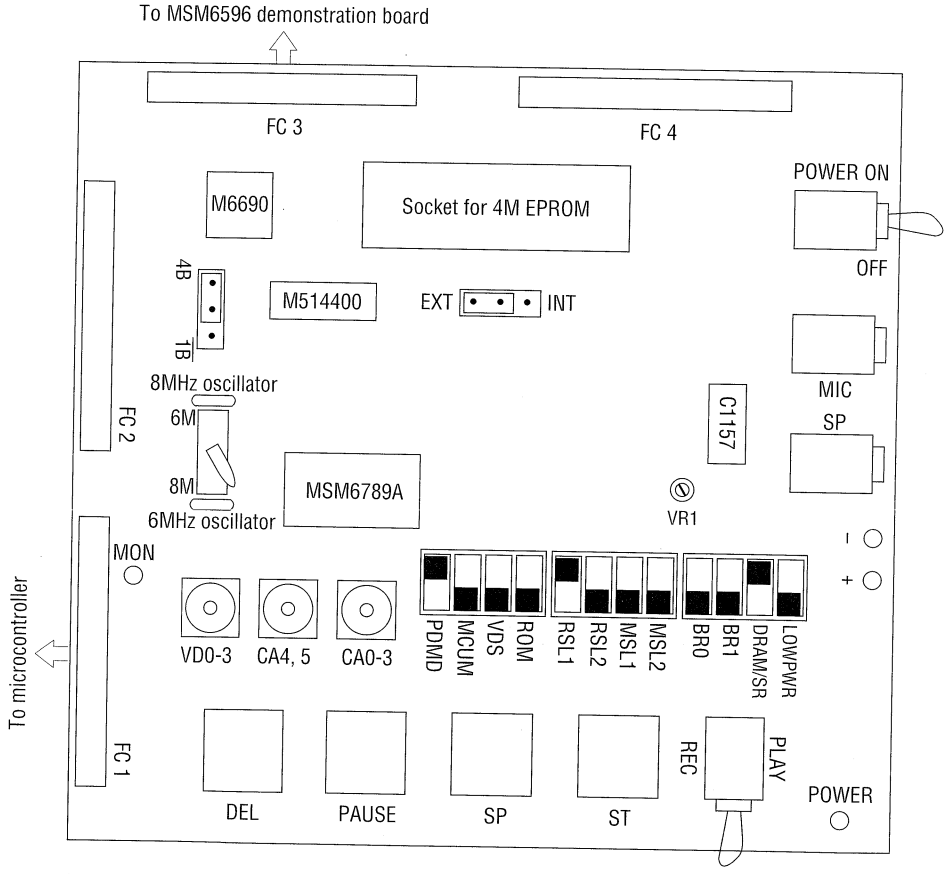


OKI Semiconductor

MSM6789A DEMO BOARD

MSM6789A Demonstration Board

1. BOARD DESIGN



2. CONDITION SETTING PROCEDURE

Three HEX switches and three DIP switches are used to set recording conditions.

2-1 Normally turn ON dip switch PDMD.

OFF The MSM6789A enters power down status automatically, except during recording/playback.

ON The MSM6789A enters standby status, not power down status, except during recording/playback.

2-2 Set DIP switch MCUM to OFF.

OFF The MSM6789A enters standalone mode.

ON The MSM6789A enters microcomputer interface mode.

Note: The microcomputer interface mode is not selected only by setting DIP switch "MCUM" to "ON" side.
Refer to section 10 when using this device in microcomputer interface mode.

2-3 Select voice detect start recording or mute recording funciton using the DIP switch VDS, and set voice detect level/mute level using HEX switch VD0-3.

VDS OFF Mute record function.
VDS ON Voice detect recording.
VDS0-3 Mute level/voice detect level setting.

Note: For normal recording, set DIP switch DVS to "OFF" and switch VD0-3 to "0".

2-4 Select recorded phrase reproduction or ROM phrase reproduction using the DIP switch ROM.

OFF Recorded phrase playback is selected.
ON ROM phrase playback is selected.

2-5 Select external memory to be connected by DIP switch DRAM/SR. Also select the type of external DRAM to be connected using short plug (4B/1B). (Normally set DIP switches to ON and short plug to "4B".

OFF Serial register
ON DRAM
4B x 4-bit type DRAM
1B x 1-bit type DRAM

2-6 Set DIP switch RSL1 to ON, RSEL2 to OFF, and both MSL1 and MSL2 to OFF.

2-7 Select the bit rate using DIP switches BR0 and BR1 and original oscillation select switch. The relationship between bit rate, original oscillation frequency and BR0 and BR1 switches is as follows.

Original oscillating frequency	BR0	BR1	Bit rate
8 MHz	OFF	OFF	16.0 kbps
	ON	OFF	12.6 kbps
	OFF	ON	10.0 kbps
6 MHz	OFF	OFF	12.0 kbps
	ON	OFF	9.5 kbps
	OFF	ON	7.5 kbps

* Both BR0 and BR1 cannot be ON at the same time.

2-8 Select CAS before RAS refresh cycle in power down status using the DIP switch LOWPWR.

2-9 Set HEX switch (CA) to the channel used for recording.
This specifies the phrase.

CA4, 5	CA0-3	Phrase number	Remarks
0	0	Ch 00	For deleting all phrases
0	1	Ch 01	Applicable to recorded phrase playback and ROM phrase playback (63 phrases)
:	:	:	
:	:	:	
:	F	Ch 0F	
1	0	Ch 10	
:	:	:	
:	:	:	
:	F	Ch 1F	
2	0	Ch 20	
:	:	:	
:	:	:	
:	F	Ch 2F	
3	0	Ch 30	
:	:	:	
:	:	:	
:	F	Ch 3F	

2-10 Set the voice detect levels for voice detect start/mute recording using HEX switch VD0-3.

3. RECORDING PROCEDURE

3-1 Turn the power switch on. The LED (POWER) on the demonstration board lights.

3-2 Set HEX switches CA4, 5 and CA0-3 to "00", and VD0-3 to "0".

3-3 Press the DEL button to delete all phrases.

3-4 Set each condition according to 2. Condition Setting Procedure.

3-5 Set REC/PLAY switch to REC to select recording mode.

3-6 Press the ST button and record voice via the microphone.

3-7 When voice is recorded until the end of memory capacity, recording automatically ends. To quit recording, press the SP button.

Note: When voice is recorded to the end of the memory capacity, no other phrases can be recorded.

4. PLAYBACK PROCEDURE

4-1 Set the REC/PLAY switch to PLAY to select playback mode.
4-2 Press the ST button to start playback. MON (light emitting diode) is lit during playback.
4-3 Playback automatically ends when playback for an entire recording is over. To quit playback, press the SP button.
4-4 Adjust the playback volume by volume control.

5. VOICE DETECT RECORDING/PLAYBACK PROCEDURE

5-1 Set the DIP switch VDS to ON.
5-2 Set the voice detect level using HEX switch VD0-3.
The remainder of the procedure is the same as normal recording/playback.

6. MUTE RECORDING/PLAYBACK PROCEDURE

6-1 Set DIP switch VDS to OFF.
6-2 Set the voice detect level using the VD0-3 HEX switch.
The remainder of the procedure is the same as normal recording/playback.

7. PAUSE PROCEDURE OF RECORDING/PLAYBACK

7-1 When the PAUSE button is pressed during recording/playback, recording/playback pauses.
7-2 Press the ST button to restart recording/playback.

8. ROM PLAYBACK PROCEDURE

8-1 Use short plug (EXT/INT) to select whether EPROM is connected externally or whether it is mounted on the board.
8-2 If INT is selected, connect the 4 Mb EPROM to the socket on the board.
* Do not use a ROM other than 4 Mb EPROM.
8-3 If EXT is selected, connect the MSM6506 demonstration board to FC3 of the 20-pin connector.
8-4 Select a channel for playback using HEX switches CA4, 5 and CA0-3. (See the address list on a next page.)
8-5 Press the ST button to start playback. The LED (MON) is lit during playback. To quit playback, press the SP button.
8-6 If the PAUSE button is pressed during ROM playback, ROM playback pauses.
8-7 Press the ST button to restart ROM playback.

Channel	Phrase	Bit rate (kbps)	Channel	Phrase	Bit rate (kbps)
00	Stop code	—	20	Sound effects 3	12
01	Japanese	16	21	Sound effects 3	10
02	Japanese	12	22	Barking of dog	16
03	Japanese	10	23	Barking of dog	12
04	Chinese	16	24	Barking of dog	10
05	Chinese	12	25	Roar of lion	16
06	Chinese	10	26	Roar of lion	12
07	English	16	27	Roar of lion	10
08	English	12	28	Lowing of cattle	16
09	English	10	29	Lowing of cattle	12
0A	French	16	2A	Lowing of cattle	10
0B	French	12	2B	Greetings in eight languages	16
0C	French	10	2C	Greetings in eight languages	12
0D	Spanish	16	2D	Greetings in eight languages	10
0E	Spanish	12	2E	Sound effects 1	PCM
0F	Spanish	10	2F	Sound effects 2	PCM
10	Italian	16	30	Sound effects 3	PCM
11	Italian	12	31	Barking of dog	PCM
12	Italian	10	32	Roar of lion	PCM
13	Korean	16	33	Lowing of cattle	PCM
14	Korean	12	34	Music	PCM
15	Korean	10	35	Female voice (Japanese)	16
16	German	16	36	Female voice (English)	16
17	German	12	37	Female voice (Japanese)	10
18	German	10	38	Female voice (English)	10
19	Sound effects 1	16	39	Female voice (Japanese)	12
1A	Sound effects 1	12	3A	Female voice (English)	12
1B	Sound effects 1	10	3B	Female voice (Japanese)	7.5
1C	Sound effects 2	16	3C	Female voice (English)	7.5
1D	Sound effects 2	12	3D		
1E	Sound effects 2	10	3E		
1F	Sound effects 3	16	3F		

For using CH39 to CH3C, set the oscillator to 6 MHz.

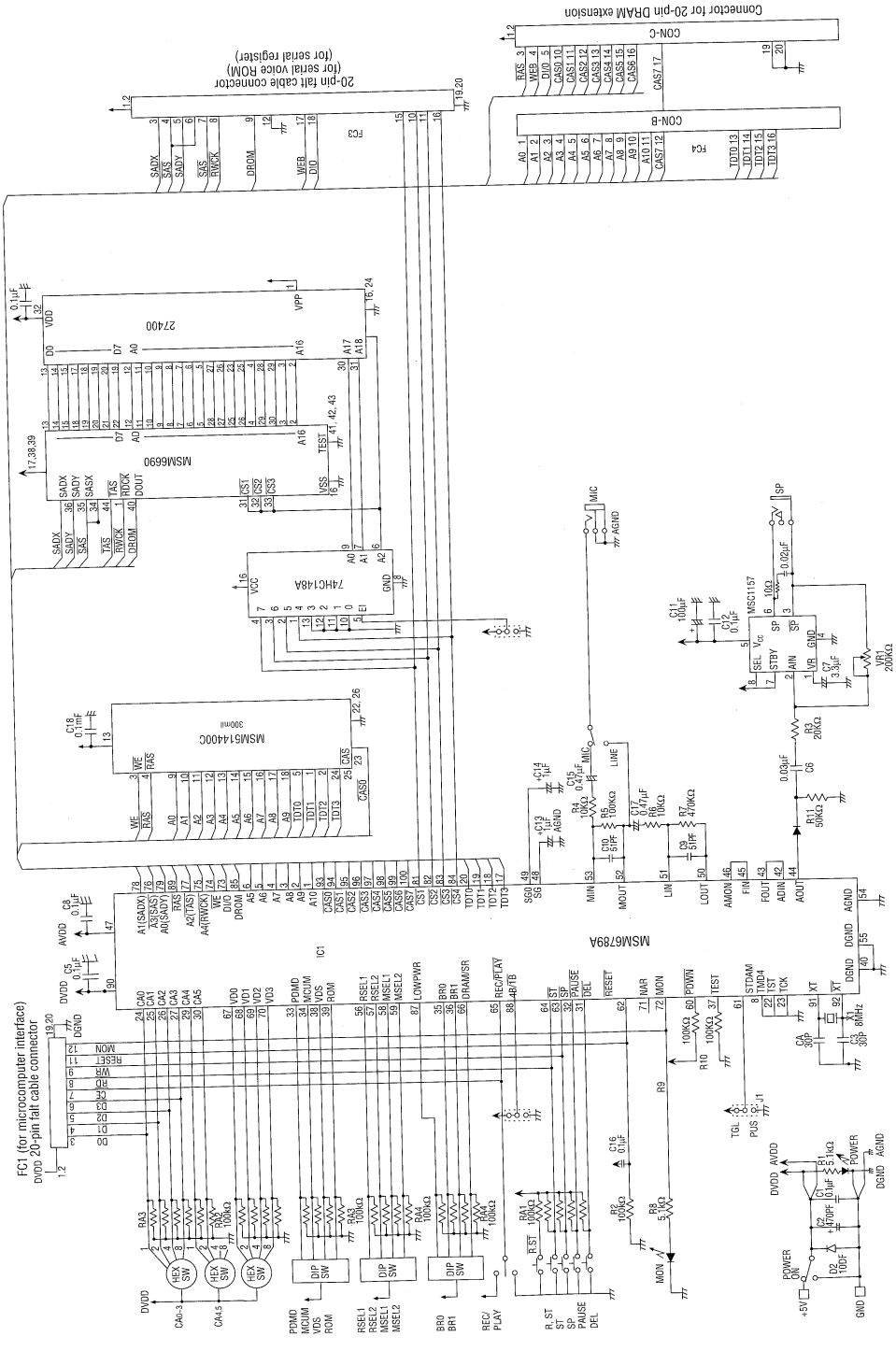


Figure 9. Stand alone mode circuit diagram

10. IN CASE OF MICROCOMPUTER INTERFACE MODE

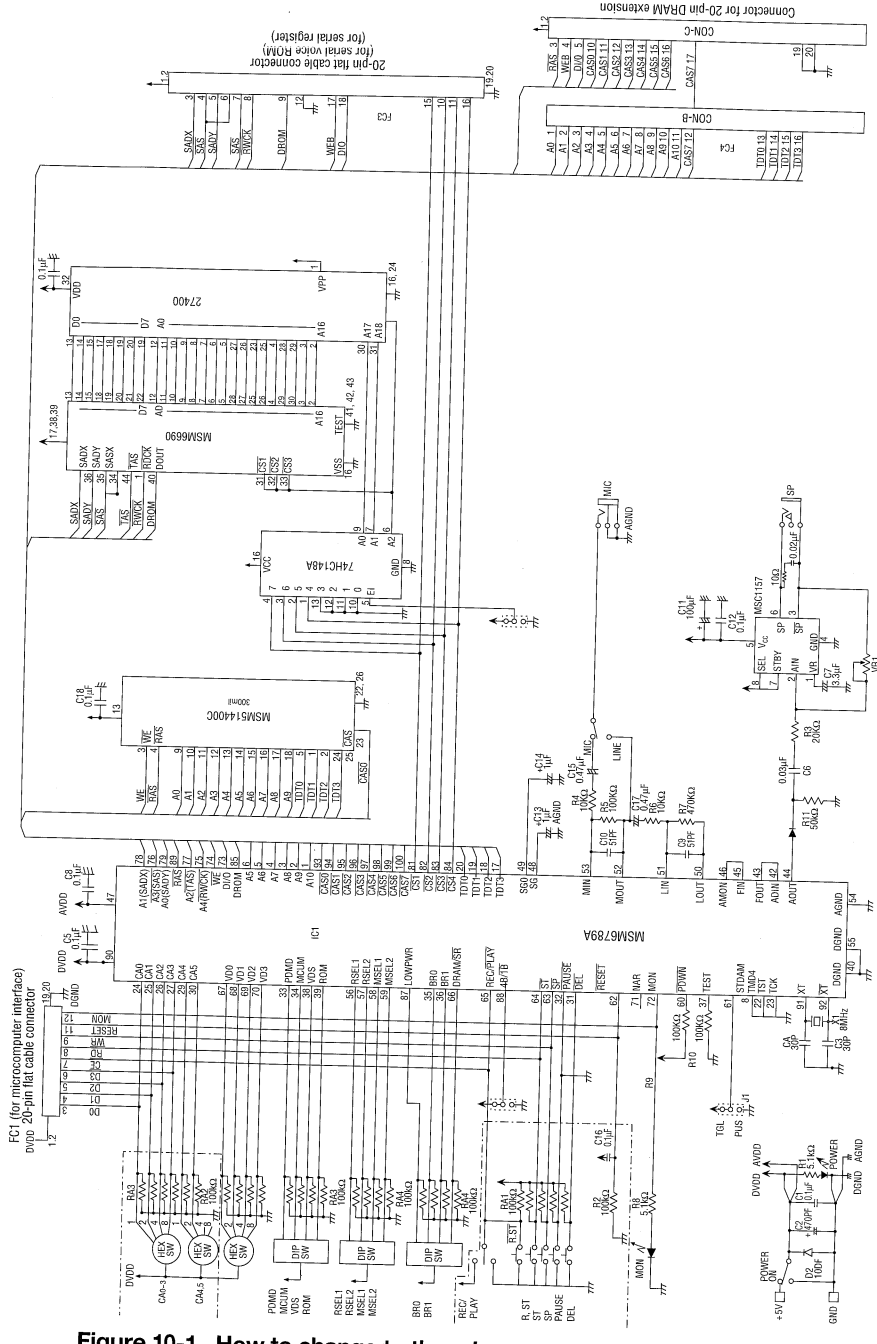


Figure 10-1. How to change to the microcomputer interface mode.

Note: Dotted portions are not mounted.
$\overline{\text{PAUSE}}$ pin is connected to GND.

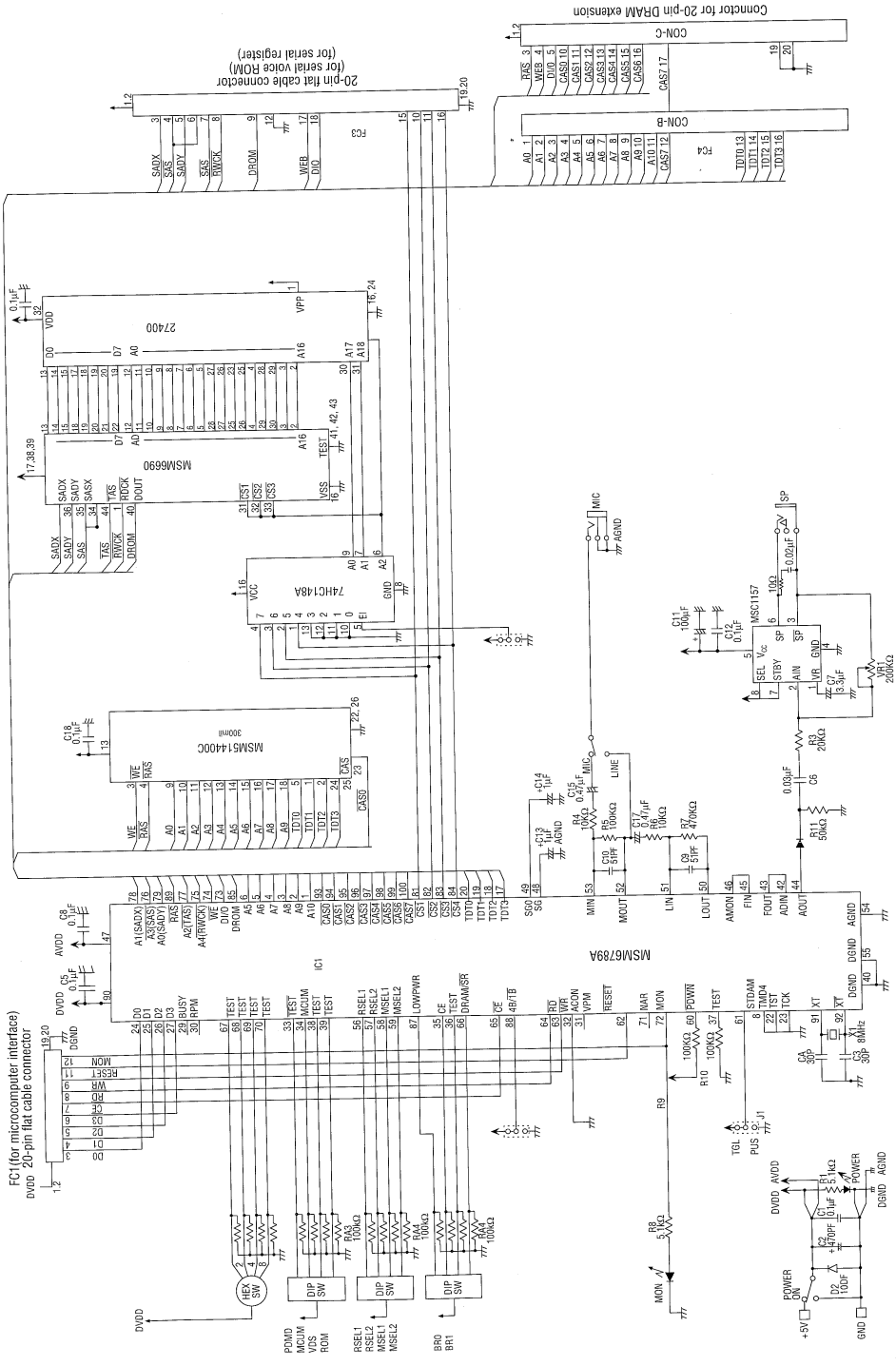


Figure 10-2. Microcomputer interface mode circuit diagram

10-3 Conditions setting procedures.

Recording conditions are set using three DIP switches and one HEX switch.

10-3-1 Set HEX switch VD0-3 to "0".

10-3-2 Set DIP switch PDMD to "ON".

10-3-3 Set DIP switch MCUM to "ON".

"OFF" Stand alone mode

"ON" Microcomputer interface mode

10-3-4 Set DIP switch VDS to "OFF".

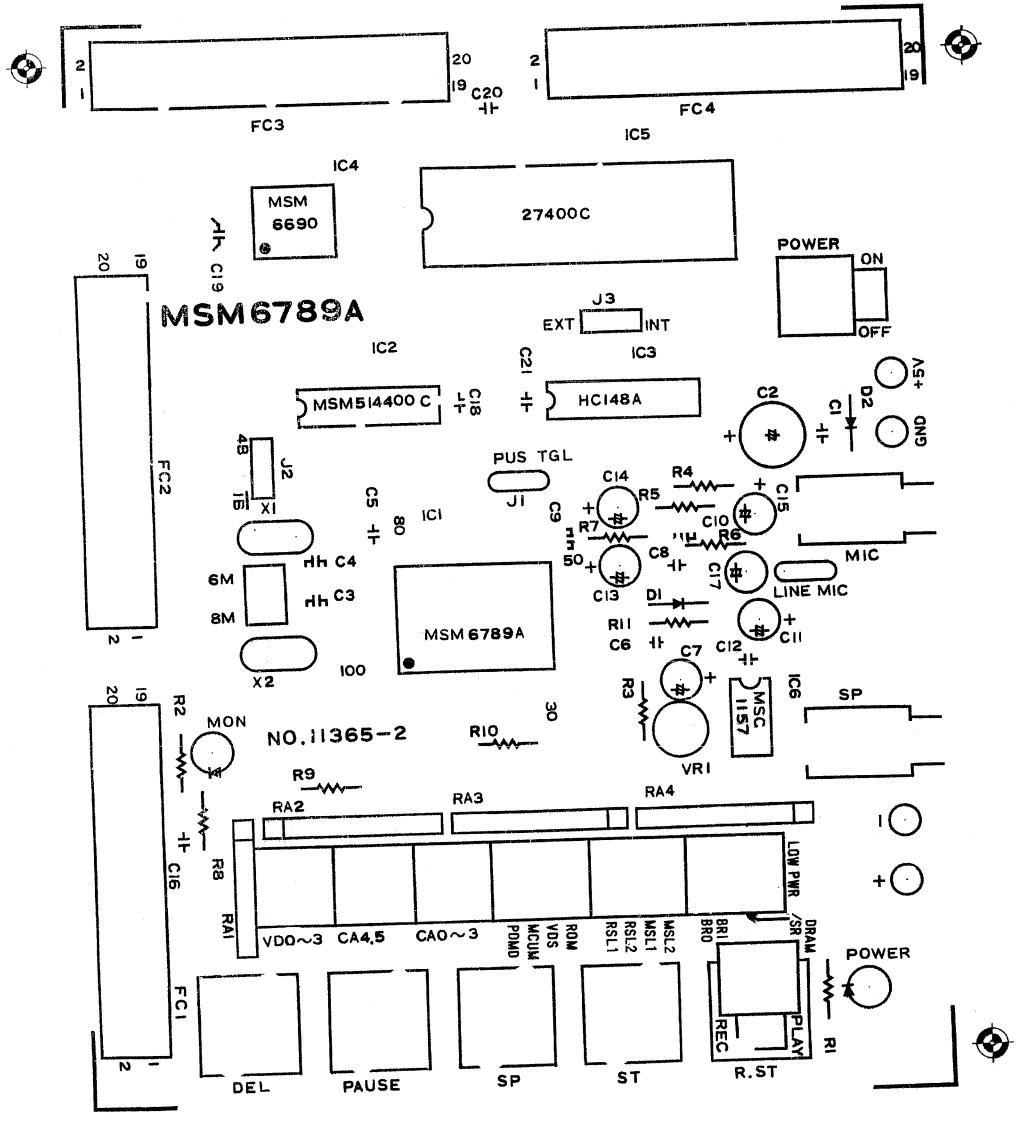
10-3-5 Set DIP switch ROM to "OFF".

10-3-6 Set DIP switch RSL1 to "ON", RSL2 to "OFF" and both MSL1 and MSL2 to "OFF".

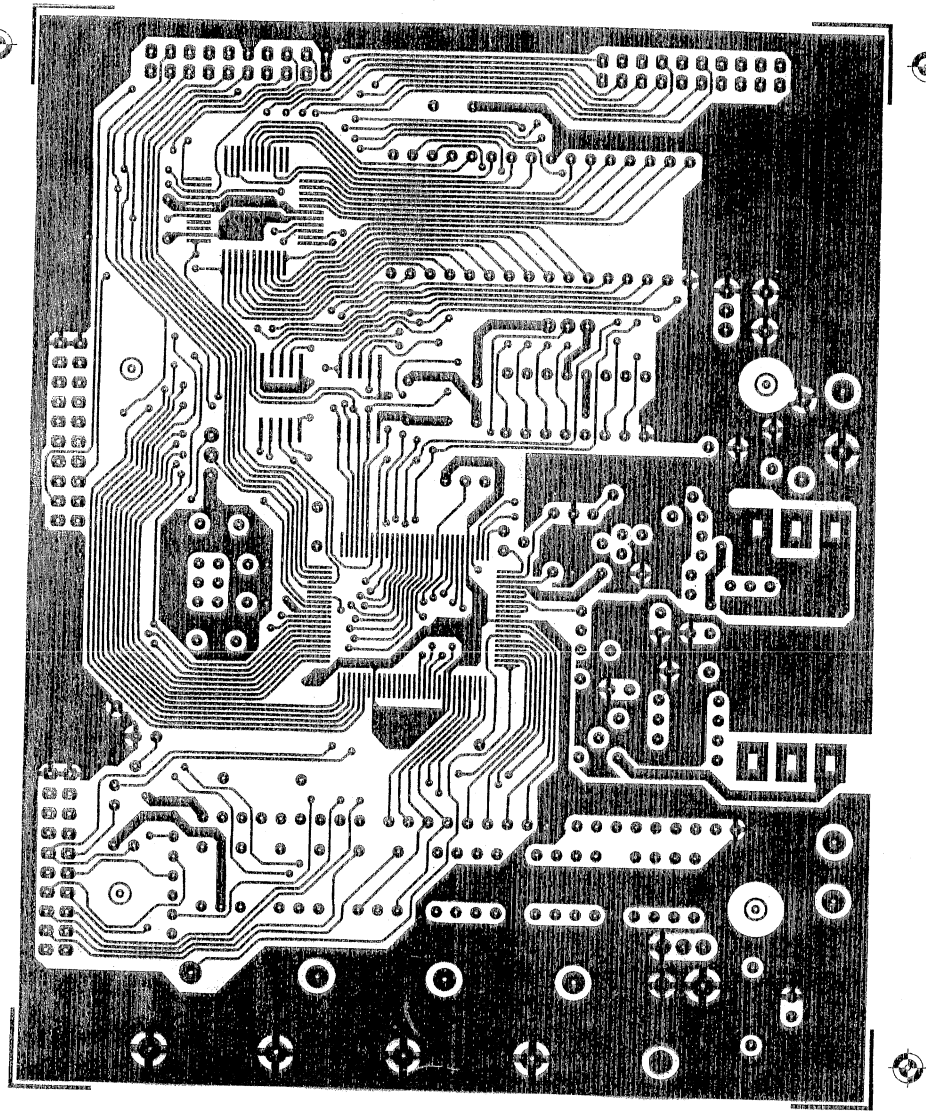
10-3-7 Set DIP switch BR0 to "ON" and BR1 to "OFF".

11. PATTERN LAYOUT

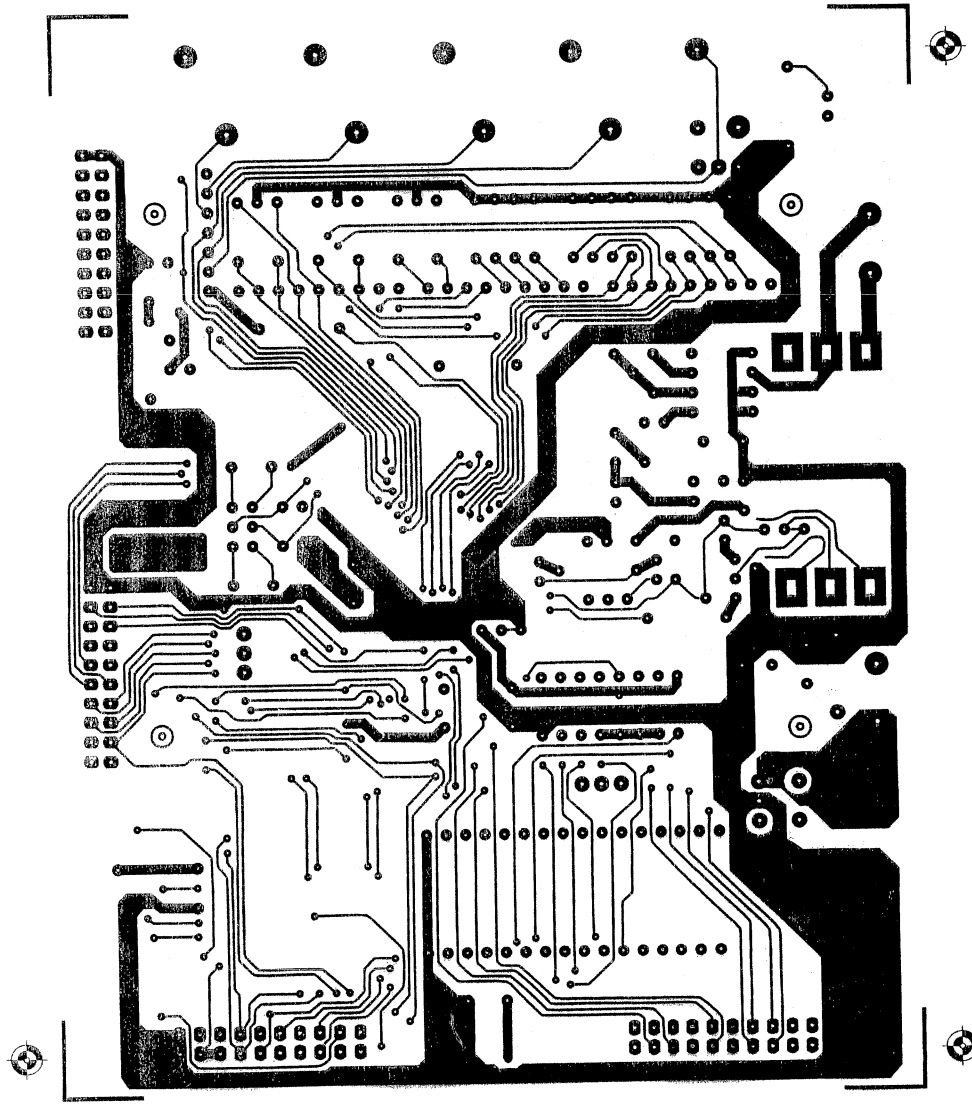
11-1 Silk Screen



11-2 Mounting Side



11-3 Solder Side

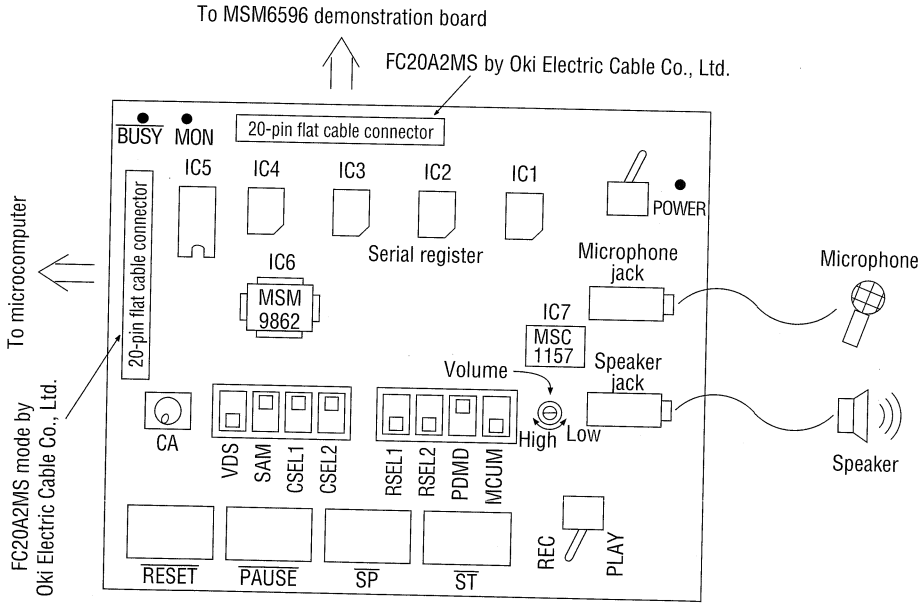


OKI Semiconductor

MSM9862 DEMO BOARD

MSM9862 Demonstration Board

1. BOARD DESIGN



2. CONDITION SETTING PROCEDURE

Set the recording conditions using two DIP switches and the rotary switch.

The setting indicated above allows 22 seconds of recording with 8 kHz sampling using internal E²PROM. (3-bit ADPCM, 8 kHz sampling)

2-1 Set DIP switch MCUM to OFF, then MSM9862 enters standalone mode. (If MCUM is set to ON, MSM9862 enters microcomputer interface mode.)

2-2 Set DIP switch RSEL1 and RSEL2 as follows according to the selection of memory for playback/recording and the number of serial registers to be mounted.

RSEL2	OFF		ON	
RSEL1	OFF	ON	OFF	ON
Memory Number of serial registers	Internal 512Kbit E²PROM	External 1Mbit Serial Register One	External 1Mbit Serial Register Two	External 1Mbit Serial Register Four

2-3 Specify recording mode and the number of channels using DIP switch CSEL1 and CSEL2.

CSEL2	OFF		ON	
CSEL1	OFF	ON	OFF	ON
Recording mode	Fix mode			Flex mode
Number of channels	8	4	2	8

Fix mode ..... Recording time of each channel is the time corresponding to each memory capacity divided by the number of channels.

The recording time of each channel is determined by the following formula.

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (Kbit)}}{\text{Sampling frequency (kHz)} \times 3\text{ (bit)} \times \text{number of channels}} \text{ (Seconds)}$$

For example, recording time per channel becomes as follows when two serial registers and two channels are used with a 8 kHz sample frequency. (RSEL1=OFF, RSEL2=ON, CSFL1=OFF, CSEL2=ON, SAM=ON)

$$\text{Recording time} = \frac{1.024 \times 2048\text{ (Kbit)}}{8\text{ (kHz)} \times 3 \times 2} \fallingdotseq 44 \text{ seconds}$$

Flex mode ..... Recording time of each channel is arbitrary within each memory capacity range. The recording sequence is ch0, ch1, - - - ch7.

2-4 Set the rotary switch (CA) to the channel used for recording/playback.

CA	Fix mode			Flex mode
	8	4	2	8
0	ch0	ch0	ch0	ch0
1	ch1			ch1
2	ch2	ch1		ch2
3	ch3			ch3
4	ch4	ch2	ch1	ch4
5	ch5			ch5
6	ch6	ch3		ch6
7	ch7			ch7

2-5 Specify the sampling frequency using DIP switch SAM.

SAM	OFF	ON
Sampling frequency	$\frac{f_{osc}}{768}$	$\frac{f_{osc}}{512}$
fsamp	(5.3kHz)	(8.0kHz)

The value inside ( ) is when original oscillaiton f_{OSC}=4.096 MHz.

2-6 Set DIP switch PDMD, normally to ON.

OFF MSM9862 enters power down status, except during recording/playback.

ON MSM9862 is always in standby status, which decreases time lag between start pulse input and recording/playback start.

2-7 Select voice detect recording start using DIP switch VDS.

OFF Normal mode without voice activation

ON Voice detect recording

Note: For voice detect recording, use a DC regulated power supply, not batteries. If batteries are used, several mV of power supply variation at recording start is amplified, which is detected as voice.

3. RECORDING PROCEDURE

3-1 Set the toggle switch at the upper right of the demonstration board to ON to turn power supply ON. The LED (POWER) at the upper right of the demonstration board lights.

3-2 Set each condition according to "2. Condition Setting Procedure".

3-3 Set the toggle switch at the lower right of the demonstration board to REC to select recording mode.

3-4 Press The $\overline{ST}$ button once to record voice from the microphone. The LED (MON) at the upper left of the demonstration board lights during recording.

3-5 When voice is recorded until the end of channel memory capacity, recording automatically ends. To quit recording, press The $\overline{SP}$ button.

4. PLAYBACK PROCEDURE

4-1 Set the toggle switch at the lower right of the demonstration board to PLAY to select playback mode.

4-2 Press The $\overline{ST}$ button once to start playback. The LED (MON) lights during playback.

4-3 Playback automatically ends when playback for an entire recording is over. To quit playback, press The $\overline{SP}$ button.

4-4 Adjust playback volume by the volume control.

5. RECORDING/PLAYBACK PAUSE PROCEDURE

5-1 Press the $\overline{PAUSE}$ button to pause during recording/playback.

5-2 To restart recording/playback, press The $\overline{ST}$ button.

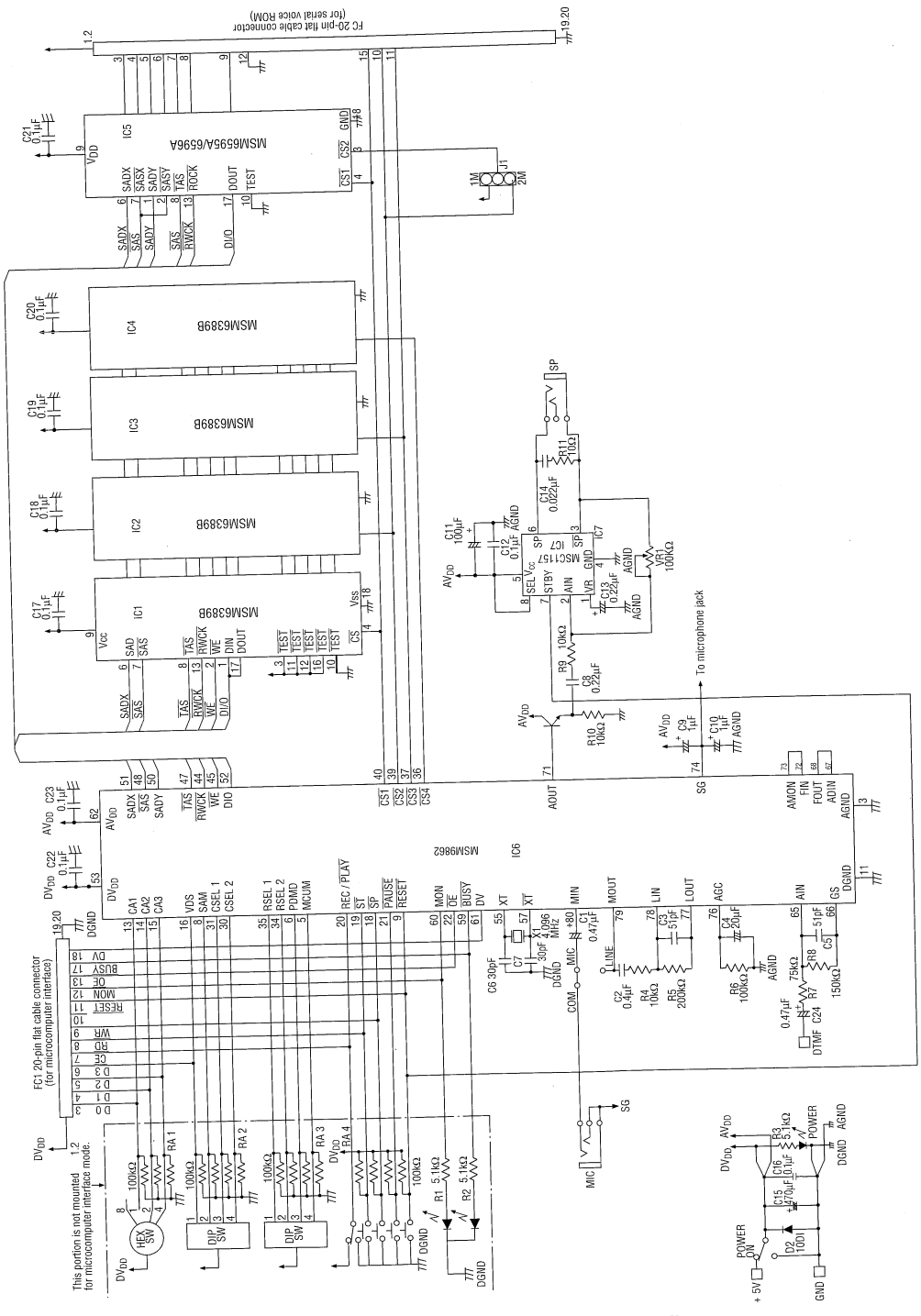


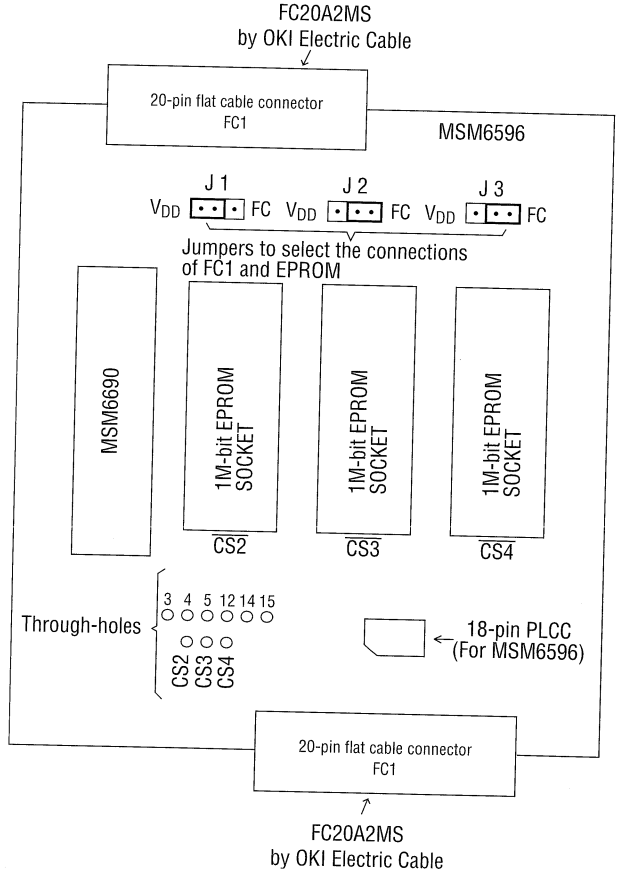
Figure. MSM9862 Demonstration Board circuit diagram

OKI Semiconductor

MSM6596 DEMO BOARD

MSM6596 Demonstration Board

BOARD DESIGN



HOW TO USE THE BOARD

1. EPROM Connection Procedure
   - Position to insert the EPROM
     When one serial register is used, set the EPROMs at the positions of $\overline{CS2}$ and $\overline{CS3}$ or the positions of $\overline{CS3}$ and $\overline{CS4}$.

   - Jumper setting
     When the EPROMs are set at the $\overline{CS2}$ and $\overline{CS3}$, set J1 and J2 of jumpers to the right side (FC side) and J3 of jumper to the left side (V_{DD} side).
     When the EPROMs are set at the $\overline{CS3}$ and $\overline{CS4}$, set J2 and J3 of jumpers to the right side (FC side) and J1 of jumper to the left side (V_{DD} side).

2. 18-pin PLCC (for MSM6596) Connection Procedure

- 18-pin PLCC
  Mount the MSM6596 of the 18-bit PLCC

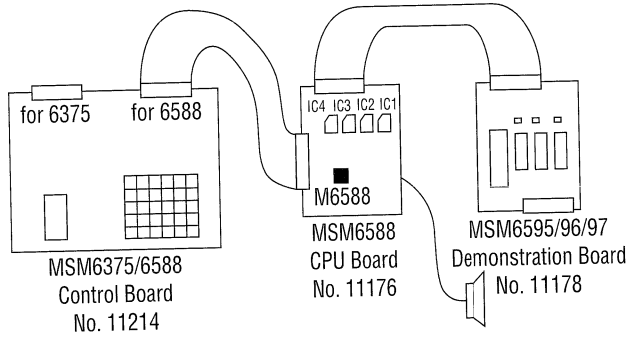
- Jumper setting
  In the evaluation of EPROM, when EPROMs are set at the positions of $\overline{CS2}$ and $\overline{CS3}$, connect the through-holes $\overline{CS2}$ and 4, and $\overline{CS3}$ and 3 with the jumper wire.
  When EPROMs are at the positions of $\overline{CS3}$ and $\overline{CS4}$, connect the through-holes $\overline{CS3}$ and 4, and $\overline{CS4}$ and 3 with jumper wire.

3. MSM6588 Demonstration Board Connection Procedure

- To play the voice of EPROM, connect the 20-pin flag cable connector FC1 to the connector for the MSM6596 of the MSM6588 demonstration board.

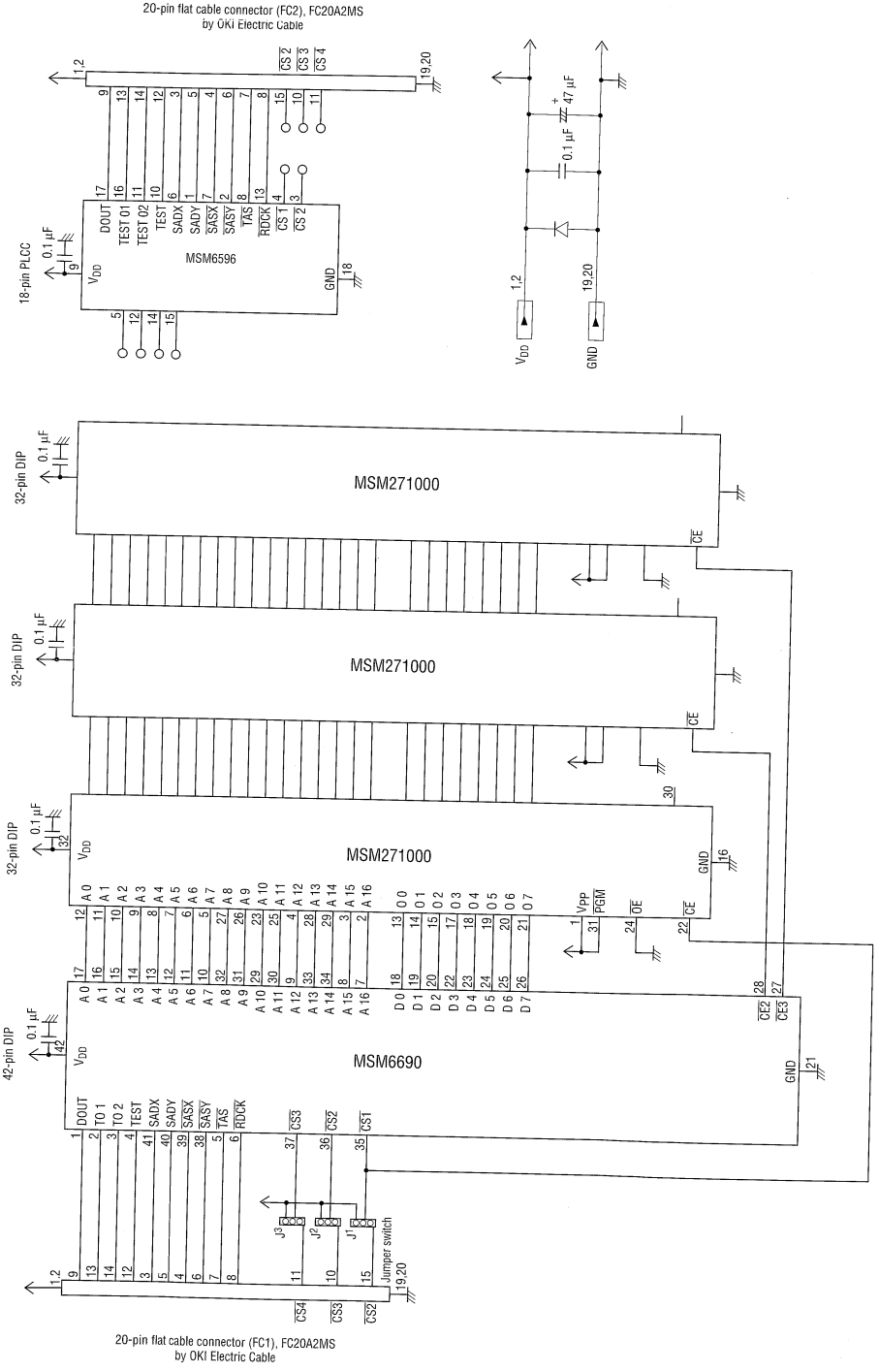
- To play the voice of 18-pin PLCC, connect the 20-pin flat cable connector FC2 to the connector for the MSM6596 of the MSM6588 demonstration board.

<Connecting Diagram>



Note: When the serial register is not mounted to IC1 on the MSM6588 CPU board (No. 11176), the circuit does not operate normally. If serial register is mounted to IC2-IC4, the normal operation is not possible either.

CIRCUIT DIAGRAM

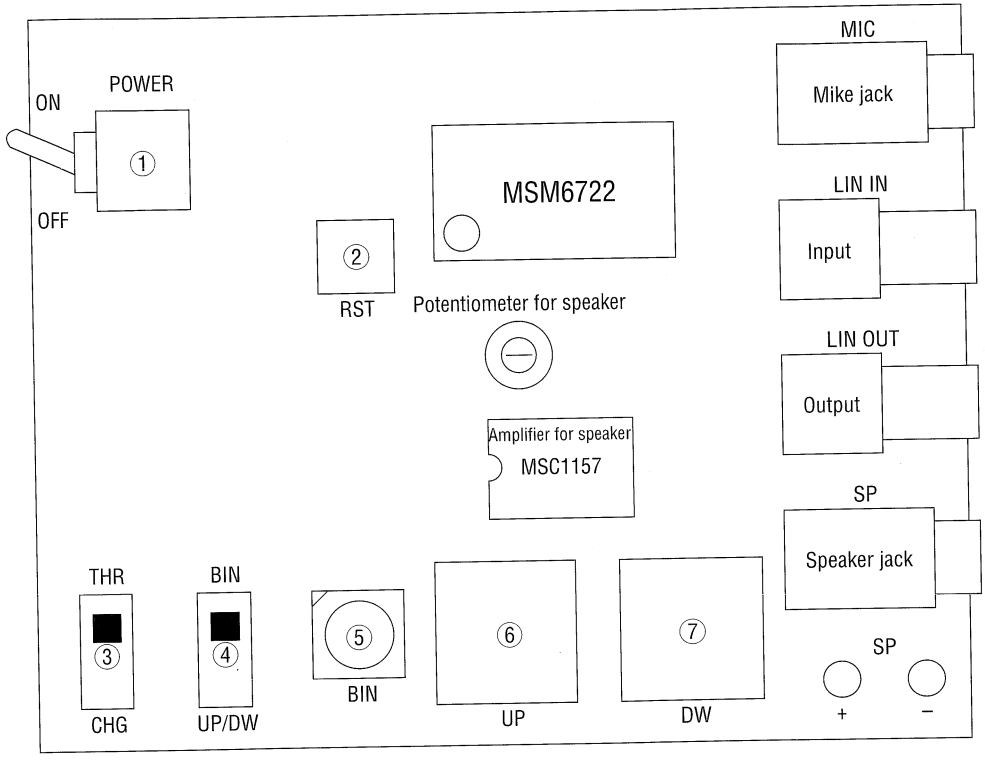


OKI Semiconductor

MSM6722 DEMO BOARD

MSM6722 Demonstration Board

BOARD DESIGN



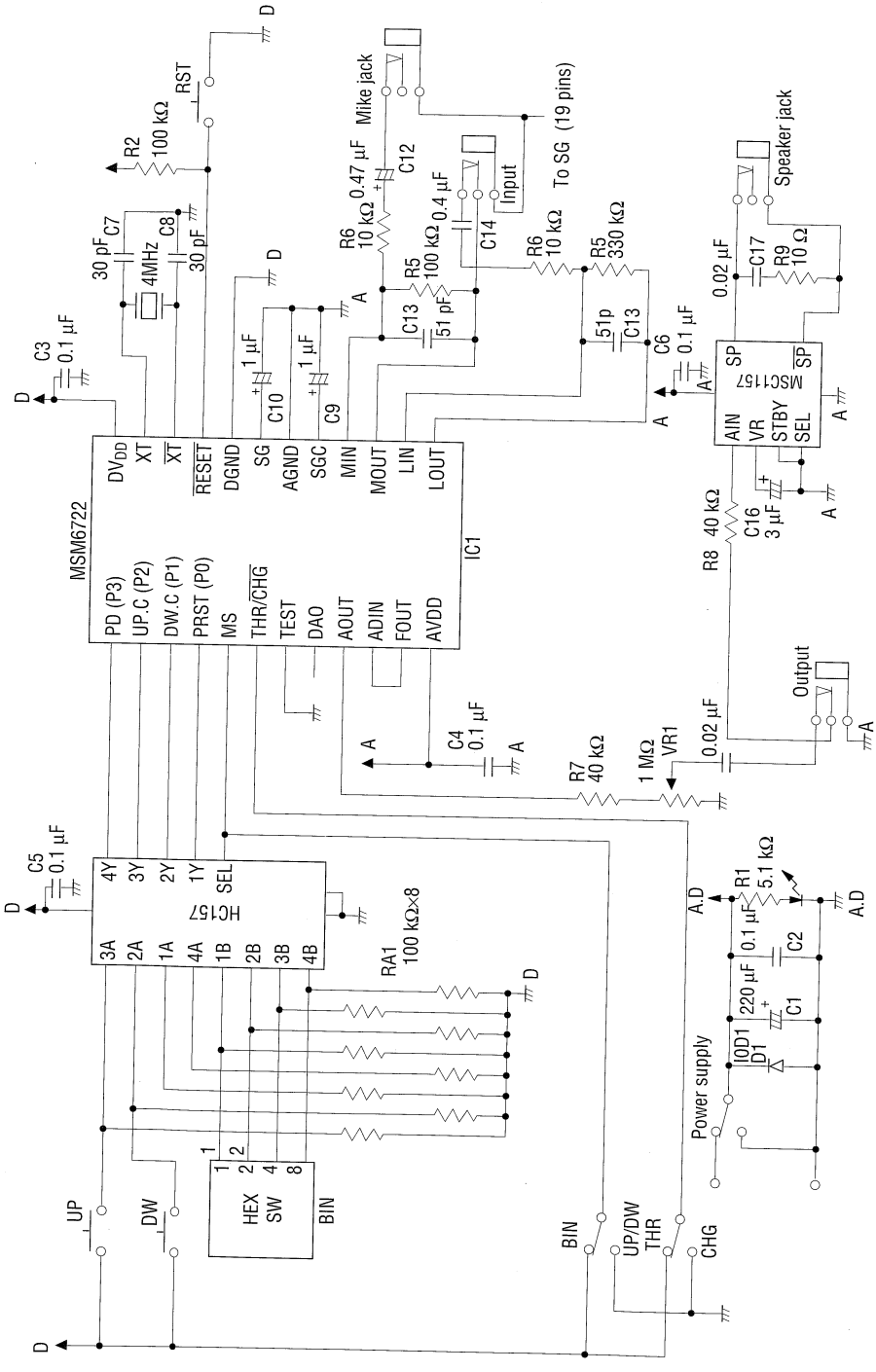
INITIALIZATION

- Insert the mike into the mike jack.
- Insert the speaker into the speaker jack.

SWITCHES

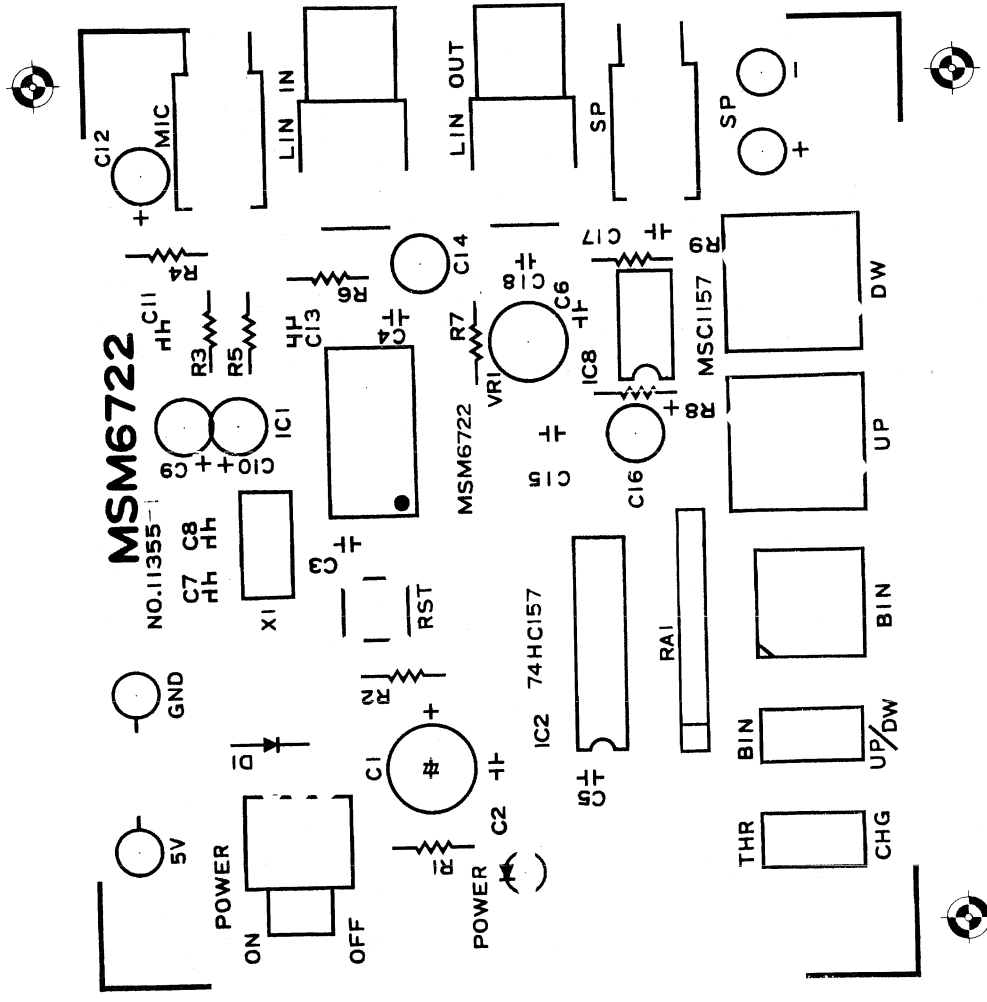
① Main power switch.
② Reset switch. Pressing the switch initializes the LSI.
③ THR/CHG switch. Placing the switch in the THR position outputs voice incurring no interval translation. Placing the switch in the CHG position outputs voice incurring interval translation.
④ Mode selection switch. Placing the switch in the BIN position sets up the binary mode. Placing the switch in the UP/DW position sets up the up/down mode.
⑤ HEX switch. Used in the binary mode to change intervals.
⑥⑦ Incremental/decremental switches. In the incremental/decremental mode, the switches allow the interval to be changed. Pressing the switches concurrently enables the interval step to be reset.

CIRCUIT DIAGRAM

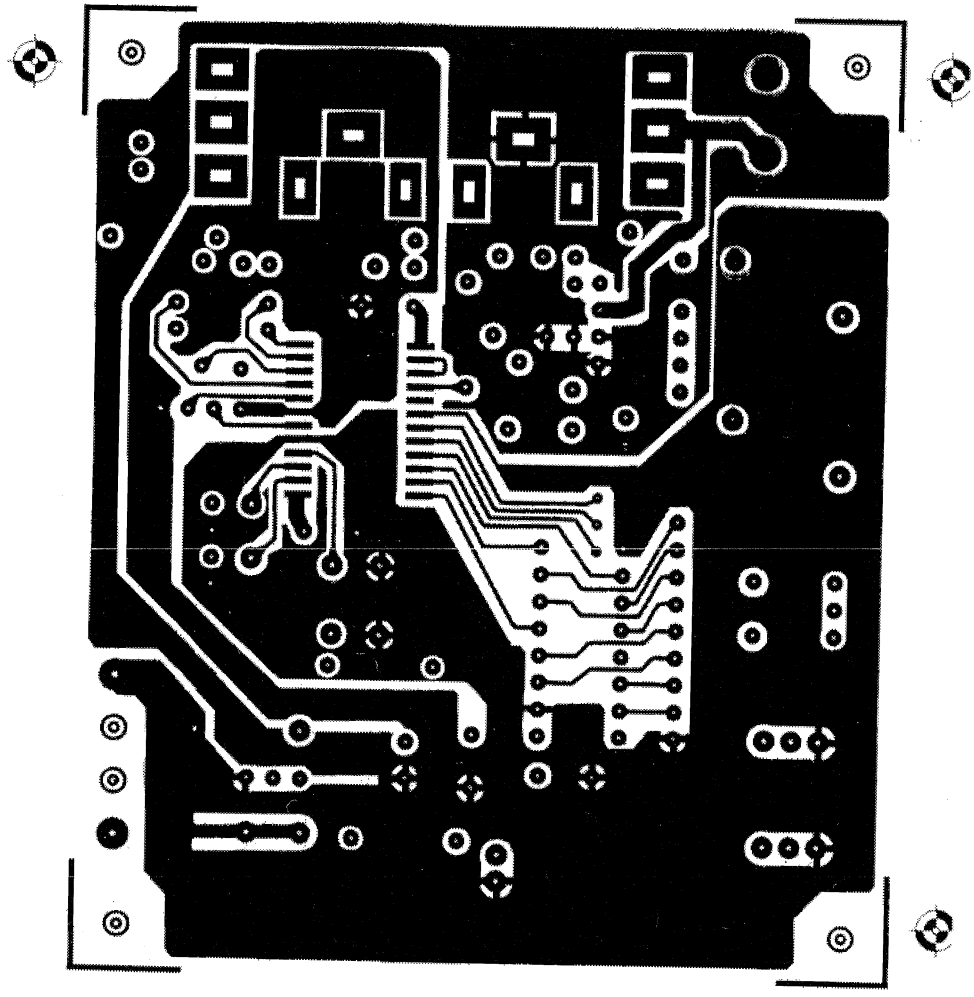


PATTERN LAYOUT

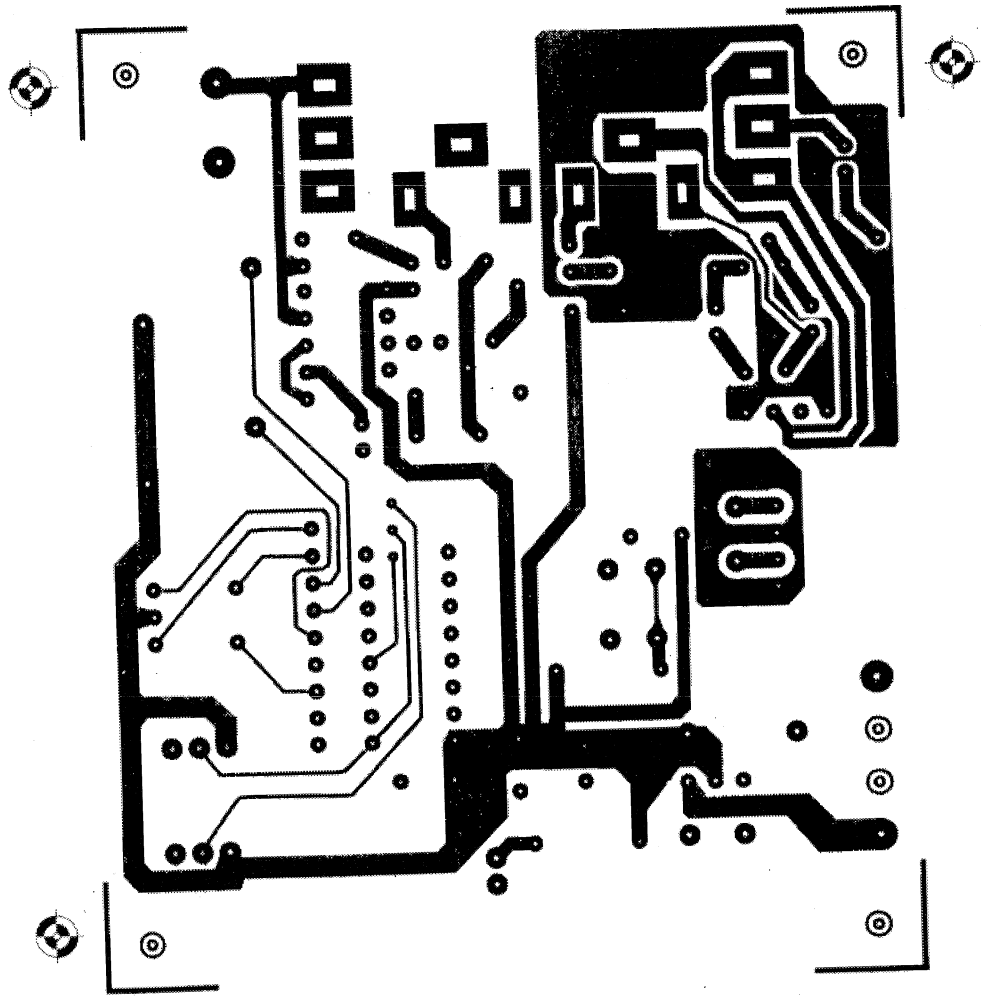
Silk Screen



Mounting Side



Solder Side



Q&A

CONTENTS

Q1: What kind of method is ADPCM?

A1 First the basic DM and ADM methods are mentioned, followed by the ADPCM method.

• DM and ADM methods

In the DM (Delta Modulation) method a certain quantity (Δ) predetermined for each cycle of sampling is added or subtracted to express a voice waveform. In other words, the addition of a Δ is encoded as 1, while the subtraction of a Δ is encoded as 0. Thus, rapid changes in voice waveform with respect to a step width Δ cannot be covered by this method. Figure 10.1 (a) illustrates this case.

For the ADM (Adaptive Delta Modulation) method, the quantized width (Δ) is adjusted according to the rapid changes to improve the response of the voice waveform. Encoding one bit is based on this means. If a value of 1 or 0 continues for a certain period, the quantized width (Δ) is enlarged for quicker response. Figure 10.1 (b) illustrates such quick response.

• ADPCM method

In the ADPCM (Adaptive Differential Pulse Code Modulation) method is such that the basic width of quantization (Δ) is adjusted adaptive to the rapid changes for each cycle of sampling to encode each signal as three to four bits of data. This provides higher response of voice waveform.

For example, in the case of four-bit ADPCM, the upper one bit stands for polarity (increase or decrease) data, while the lower three bits determine the multiplier factor to the basic width of quantization (Δ). (The Δ value depends on the correlation with the past data.) This means that about 400 pieces of data [(about 50 Δ pieces) x 8 (for 3 bits)] can be changed at a time. Therefore, approximately 400 pieces of data are available. Figure 10.2 illustrates this case.

Furthermore, in the three-bit ADPCM, the upper one bit stands for polarity (increase or decrease) data, while the lower two bits determine the multiplier factor to the basic width of quantization (Δ). This means that about 200 pieces of data [(about 50 Δ pieces) x 4 (for 2 bits)] can be changed at a time. Therefore, 200 pieces of data are available.

The ADPCM method allows the achievement of high-quality sound in a relatively simple configuration, and the easy creation of voice data.

Note, however, that there is no compatibility between ADPCM data created by different manufacturers.

Figure 10.1
DM and ADM Methods

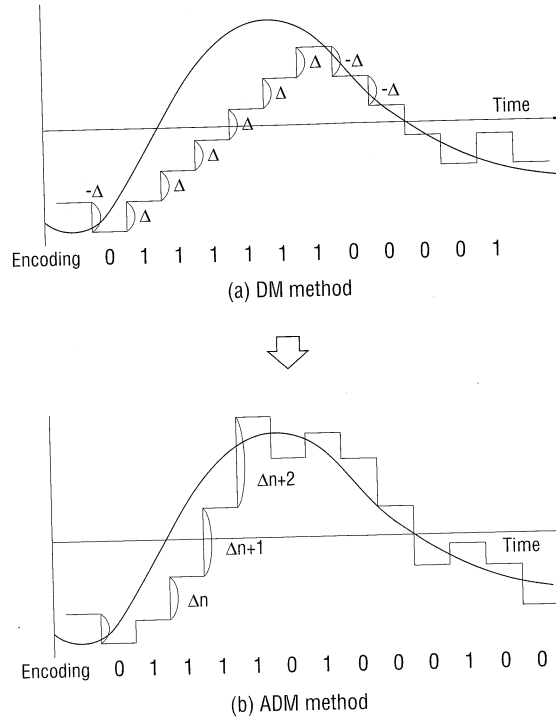
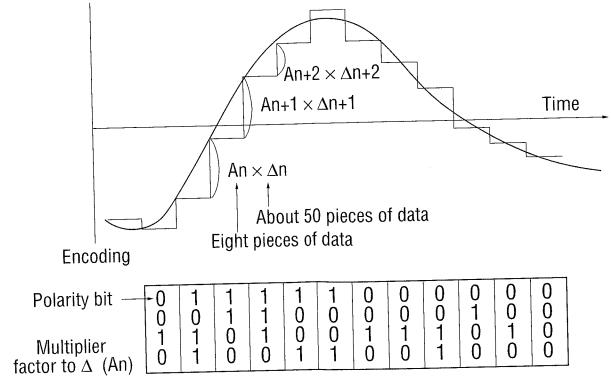


Figure 10.2
4-bit ADPCM



Q2: What is the specific value of the quantized width by ADPCM?

A2 The quantized width is an important factor in determining sound quality implemented by the ADPCM method, and is the know-how owned by individual manufacturers. Hence, detailed data of our ADPCM method (OkiADPCM) cannot be disclosed. The OkiADPCM method is not compatible with the ADPCM method conforming to ITU-T (former CCITT).

Q3: How should we perceive the relationship between bit rates and the synthesis length and between bit rates and sound quality?

A3 Bit rate and length of synthesis

A bit rate indicates the degree of information compression, and how many bits of data are required for synthesis in one second. Thus, the bit rate depends on the sampling frequency and the amount of data per sample, and is determined by the following formula:

Bit rate (kbps) = sampling frequency (kHz) x amount of data per sample (bits)

Example 1

Sampling frequency: 4 kHz, data: 4-bit ADPCM

Bit rate (kbps) = 4 (kHz) x 4 (bits) = 16 (kbps)

Example 2

Sampling frequency: 8 kHz, data: 4-bit ADPCM

Bit rate (kbps) = 8 (kHz) x 4 (bits) = 32 (kbps)

The length of synthesis depends on the memory capacity and the bit rate, as shown in the following formula:

$$\text{Synthesis length (seconds)} = \frac{1.024 \times (\text{memory capacity}) \text{ (Kbits)}}{\text{bit rate (kbps)}}$$

$$= \frac{1.024 \times (\text{memory capacity}) \text{ (Kbits)}}{\text{sampling frequency (kHz)} \times \text{data amount per sample (bits)}} \text{ (seconds)}$$

Example

Sampling frequency: 4 kHz, 4-bit ADPCM, Memory capacity: 256 Kbits

$$\text{Synthesis length (seconds)} = \frac{1.024 \times 256 \text{ Kbits}}{4 \text{ (kHz)} \times 4 \text{ (bits)}} \fallingdotseq 16.4 \text{ (seconds)}$$

Bit rate and sound quality

A lower bit rate results in a longer synthesis length. But the response to a voice waveform becomes lowered, with deteriorated sound quality.

Q4.1: How can sinusoidal waves be produced by ADPCM?

A4.1 Tables 10.1.1 to 10.1.4 show ADPCM data for 4-bit (0 to F) sinusoidal waves, and Table 10.1.5 shows ADPCM data for 3-bit (0 to 7) sinusoidal waves. There are four kinds of 4-bit data corresponding to four, six, ten and twelve samples depending on the repeated data count per period of a sinusoidal wave. Figure 10.3 shows a model of an output waveform with a supply voltage (V_{DD}) of five volts.

See Q4.3, Table 10.2 for determining the frequency of the sinusoidal wave and the frequencies.

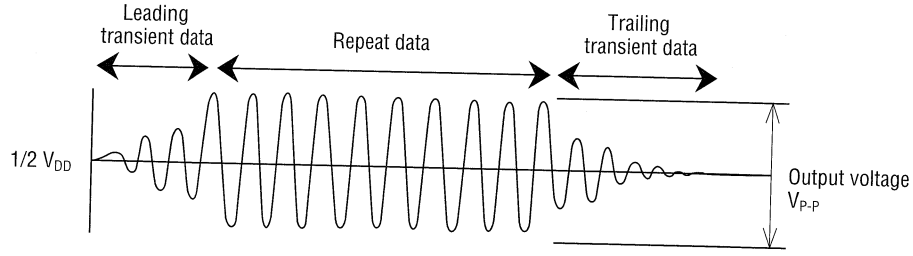


Figure 10.3 Sinusoidal Waveform Output by ADPCM

Table 10.1.1 Four-sample Output Sinusoidal Voltage and ADPCM (4-bit) Data

Output voltage	Leading transient data	Repeat data	Trailing transient data
2.0 V_{P-P}	1, 2, C, D, 4, 4, C, C, 4, 5, C, C, 4, 4, C, C, 4, 4, D, 9, 4, 0, C, 9, 4, 1, C, 8, 4, 0, C, 8, 4, 0, C, 8	4, 0, C, 8	2, 2, A, A, 2, 2, A, A, 2, 2, A, A, 2, 2, A, A, 2, 1, A, 9, 2, 1, A, 9, 2, 0, 8, 8, 0, 0, 8, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8
2.6 V_{P-P}	1, 2, C, D, 4, 4, C, C, 4, 5, C, C, 4, 4, C, C, 4, 4, D, 9, 5, 0, D, 8, 5, 0, D, 8	5, 0, D, 8	4, 0, B, 8, 3, 0, B, 8, 3, 0, A, 8, 3, 0, B, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 1, 0, 8, 8, 8, 0, 8, 0, 8, 0
3.0 V_{P-P}	1, 2, C, D, 4, 4, C, C, 4, 5, C, C, 4, 4, C, C, 4, 4, D, 9, 6, 0, E, 8	6, 0, E, 8	4, 0, B, 8, 3, 0, B, 8, 3, 0, A, 8, 3, 0, B, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, 8, 0, 8, 8, 0, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8
3.5 V_{P-P}	1, 2, C, D, 4, 4, C, C, 4, 5, C, C, 4, 4, C, C, 4, 4, D, 8, 7, 0, F, 8	7, 0, F, 8	5, 0, B, 8, 3, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 2, 0, A, 8, 1, 0, A, 9, 1, 0, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8

Table 10.1.2 Six-sample Output Sinusoidal Voltage and ADPCM (4-bit) Data

Output voltage	Leading transient data	Repeat data	Trailing transient data
0.85 V_{P-P}	0, 0, 0, B, B, B, 7, F, 7, F, 4, C, 0, 0	4, 0, 9, C, 8, 1	3, 0, 8, C, 8, 1, 1, 1, 8, A, 8, 0, 1, 0, 8, 9, 8, 1, 1, 0, 9, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8
1.0 V_{P-P}	0, 0, 0, 0, A, B, 7, F, 4, D, 2, 9	4, 0, 9, C, 8, 1	3, 0, 8, C, 8, 1, 1, 1, 8, A, 8, 0, 1, 0, 8, 9, 8, 2, 9, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0
1.5 V_{P-P}	0, 0, 0, 3, 3, 3, 7, F, 7, F, 4, C, 4, C	4, 0, 9, C, 9, 1	3, 0, 8, B, 8, 1, 2, 0, 9, B, 9, 3, 1, 1, 9, A, 8, 1, 1, 8, 0, 0, 9, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8
2.0 V_{P-P}	0, 0, 0, 0, 4, A, 7, E, 7, E, 7, F, 8, 1	4, 0, 9, C, 8, 1	2, 0, 8, A, 8, 1, 1, 0, 8, 9, 8, 0, 1, 9, 1, 8, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0
2.6 V_{P-P}	0, 0, 0, 0, 7, F, 7, F, 7, F, 4, C, 0, 0	4, 0, 9, C, 8, 1	3, 0, 8, B, 8, 1, 2, 0, 9, B, 8, 1, 2, 0, 9, A, 8, 1, 1, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0
3.5 V_{P-P}	0, 0, 0, 0, 7, F, 7, F, 7, F, 4, C, 0, 0	5, 0, A, D, 8, 2	3, 0, 8, B, 8, 1, 2, 0, 9, B, 8, 1, 2, 0, 9, A, 8, 1, 1, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0
4.25 V_{P-P}	0, 0, 0, 0, 7, F, 7, F, 7, F, 4, C, 0, 0	6, 0, B, E, 8, 3	3, 0, 8, B, 8, 1, 2, 0, 9, B, 8, 1, 2, 0, 9, A, 8, 1, 1, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0, 8, 0

Table 10.1.3 Ten-sample Output Sinusoidal Voltage and ADPCM (4-bit) Data

Output voltage	Leading transient data	Repeat data	Trailing transient data
1.0 V_{P-P}	7, 7, 7, 3, E, B, B, A, 0, 5	3, 3, 2, 8, D, B, B, A, 0, 5	3, 1, 0, 8, B, A, A, 8, 0, 3, 3, 1, 1, 8, A, 9, 9, 8, 0, 1, 2, 0, 0, 8, 8, 0, 8, 0, 8, 0
2.0 V_{P-P}	0, 5, 7, 7, 4, E, F, B, 0, 4	3, 3, 2, 8, D, B, B, A, 0, 5	3, 1, 1, 8, B, B, A, A, 0, 4, 3, 2, 1, 8, B, B, A, 9, 1, 3, 3, 2, 1, 8, B, A, A, A, 1, 2, 1, 2, 8, 8, 0, 8, 8, 0, 8, 0, 8
3.0 V_{P-P}	0, 6, 7, 7, 4, F, F, B, 0, 4	3, 3, 2, 8, D, B, B, A, 0, 5	3, 2, 0, 9, B, B, 9, 8, 2, 3, 3, 1, 0, 8, B, B, A, 8, 1, 3, 2, 1, 0, 8, A, A, 8, 8, 0, 2, 0, 0, 8, 8, 8, 0, 8, 0, 8, 0, 8, 0
4.0 V_{P-P}	0, 7, 7, 7, 7, D, E, C, 0, 3	5, 2, 1, 9, A, D, A, 9, 1, 2	3, 2, 1, 9, 9, B, 9, 9, 1, 2, 3, 0, 0, 8, 9, B, 9, 9, 1, 2, 2, 0, 0, 8, 8, A, 9, 8, 0, 2, 1, 0, 0, 8, 8, 9, 8, 0, 0, 0, 8, 0, 8, 0

Table 10.1.4 Twelve-sample Output Sinusoidal Voltage and ADPCM (4-bit) Data

Output voltage	Leading transient data	Repeat data	Trailing transient data
1.0 V_{P-P}	7, 7, 7, 3, 9, D, C, B, A, 0, 1, 4	4, 3, 2, 8, 9, C, C, B, A, 0, 1, 4	3, 2, 1, 8, 9, A, A, A, 9, 0, 1, 2, 3, 1, 8, 9, A, 8, 9, 0, 1, 1, 0, 0, 0, 8, 0, 8
2.0 V_{P-P}	7, 7, 7, 7, 1, C, C, B, B, 1, 1, 4	4, 3, 2, 8, 9, C, C, B, A, 0, 1, 4	3, 2, 0, 9, 8, A, A, A, 8, 0, 1, 2, 2, 1, 1, 0, 9, 8, A, 9, 9, 1, 1, 0, 0, 8, 0, 8, 0, 8, 8, 0, 8, 0
3.0 V_{P-P}	7, 7, 7, 7, 4, C, D, B, A, 0, 1, 4	4, 3, 2, 8, 9, C, C, B, A, 0, 1, 4	4, 1, 0, A, 8, 8, A, A, 9, 2, 2, 1, 3, 2, 2, A, A, 9, B, B, B, 3, 2, 2, 3, 2, 1, 0, B, B, B, 9, 8, 8, 1, 1, 8, 0, 8, 0, 8, 0
4.0 V_{P-P}	7, 7, 7, 7, 7, B, C, C, A, 0, 1, 4, 3, 3, 3, 8, 9, D, C, A, B, 0, 1, 4	4, 3, 2, 8, 9, C, C, B, A, 0, 1, 4	4, 2, 8, 9, A, A, 9, 9, 0, 1, 3, 3, 2, 1, 8, 9, A, B, A, 9, 0, 1, 3, 2, 2, 1, 9, 9, A, A, A, A, 0, 1, 3, 2, 0, 9, 8, 8, 0, 8, 0, 8, 0, 8

Table 10.1.5 Six-sample Output Sinusoidal Voltage and ADPCM (3-bit) Data

Output voltage	Leading transient data	Repeat data	Trailing transient data
1.0 V_{P-P}	3, 3, 3, 7, 7, 0, 3, 1, 5, 7	5, 1, 2, 1, 5, 6	5, 1, 5, 2, 1, 0, 4, 5, 4, 0, 0, 0, 4, 4, 0, 4, 0, 0, 4, 0, 4, 4, 0, 0, 4, 0, 4, 0, 4, 0, 4, 4, 0, 4, 0, 4, 0
2.0 V_{P-P}	3, 3, 3, 7, 7, 5, 3, 3, 4, 7	5, 1, 2, 1, 5, 6	5, 1, 1, 1, 1, 5, 4, 4, 0, 0, 0, 4, 4, 0, 4, 0, 0, 4, 4, 0, 4, 0, 0, 4, 4, 0, 4, 0, 0, 4, 4, 0, 4, 0, 0, 4, 4, 0, 4, 0, 4
3.0 V_{P-P}	1, 1, 1, 1, 1, 1, 3, 7, 3, 7, 3, 7, 3, 7, 3, 7	2, 0, 4, 6, 4, 0	1, 1, 4, 5, 5, 0, 1, 0, 4, 5, 5, 1, 1, 1, 4, 5, 4, 0, 1, 1, 5, 5, 5, 0, 1, 1, 4, 5, 5, 1, 1, 0, 5, 5, 4, 1, 0, 1, 5, 5, 4, 1, 0, 4, 0, 4, 0, 4

Q4.2: Can sinusoidal waves by ADPCM be used to produce an output voltage of 2.5 V_{p-p}?

A4.2 Data not covered in Tables 10.1.1 to 10.1.5 cannot be generated.

Q4.3: What are the frequencies of sinusoidal waves?

A4.3 f [kHz] stands for the frequency of a sinusoidal wave resulting from ADPCM data covered in Tables 10.1.1 to 10.1.5, while f_{SAM} [kHz] stands for the sampling frequency. If n samples of ADPCM data are repeated, the frequency of the resulting sinusoidal wave is given by the formula below.

$f = f_{SAM}/n$ (Common to four-bit and three-bit data.)

For actual values, see Table 10.2.

Table 10.2 Frequency of Synthesized Sinusoidal Wave

Sampling frequency (Hz) \ Repeated data samples	Frequency (Hz) of synthesized sinusoidal wave			
	4 samples	6 samples	10 samples	12 samples
32. 0 k	8. 0 k	5. 33 k	3. 2 k	2. 67 k
25. 6 k	6. 4 k	4. 27 k	2. 56 k	2. 13 k
24. 0 k	6. 0 k	4. 0 k	2. 4 k	2. 0 k
21. 2 k	5. 3 k	3. 53 k	2. 12 k	1. 77 k
16. 0 k	4. 0 k	2. 67 k	1. 6 k	1. 33 k
14. 0 k	3. 5 k	2. 33 k	1. 4 k	1. 17 k
12. 8 k	3. 2 k	2. 13 k	1. 28 k	1. 07 k
12. 0 k	3. 0 k	2. 0 k	1. 2 k	1. 0 k
10. 6 k	2. 65 k	1. 77 k	1. 06 k	883
10. 0 k	2. 5 k	1. 67 k	1. 0 k	833
8. 0 k	2. 0 k	1. 33 k	800	667
6. 4 k	1. 6 k	1. 07 k	640	533
6. 0 k	1. 5 k	1. 0 k	600	500
5. 3 k	1. 33 k	833	530	442
4. 0 k	1. 0 k	667	400	333

Q5: Why does voice synthesis require a low-pass filter?

A5 A low-pass filter (LPF) only passes the frequency components below a certain frequency in an input signal.

Synthesized voice output is issued by a DA converter. Therefore, a stepwise waveform is output, as shown below.

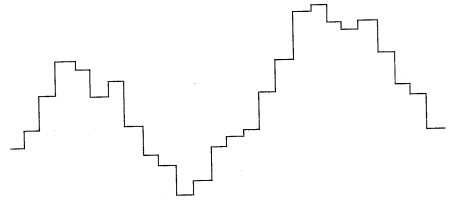


Figure 10.4 Voice Output Waveform from DA Converter

The waveform contains high-frequency noise components (metal-like sound). Moreover, the sampling theorem indicates that only the frequency components below half the sampling frequency are valid as the output. If high-frequency noise components are removed by an LPF, the following output waveform is obtained. (Smooth sound)

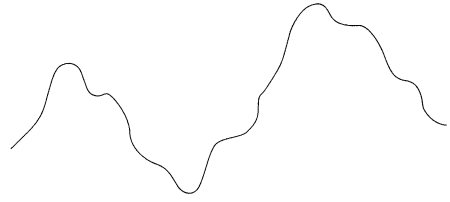


Figure 10.5 LPF Output Waveform

Q6: How should a cut-off frequency for a low-pass filter be determined?

A6 An ideal low-pass filter completely cuts off the frequency components above a certain frequency. In reality however, the output of frequency components above a certain frequency is attenuated in a slope.

Conventionally, such a slope is expressed as "dB/oct". For example, a slope of –12 dB/oct indicates that, when the frequency is doubled (an octave), the output becomes –12 dB (1/4).

The frequency at which attenuation is started is referred as a cut-off frequency (*1). The optimum cut-off frequency depends on the sampling frequency, attenuation characteristics, and frequency components of source voice. The conventional measure of design is the degree of attenuation at half the sampling frequency (f_{SAM}).

Table 10.3 lists reference values. As optimum value varies significantly with the frequency components of source voice, it is recommended that the cut-off frequency be determined in an auditory way.

Table 10.3 Relationship between Filter's Attenuation Characteristics, Cut-off Frequency and Sampling Frequency

Filter's attenuation characteristics (dB/oct)	Cut-off frequency	Gain at 0.5 f_{SAM} (dB)	Figure number
–12	0.3 f_{SAM}	–8.7	①
–18	0.33 f_{SAM}	–11	—
–24	0.35 f_{SAM}	–12.5	②
–48	0.38 f_{SAM}	–19	—

The more abrupt attenuation characteristics, the further efficient high-frequency noise removal and effective signal component output. But an increase in the number of component devices results in less cost effective performance.

Figure 10.6 shows filter's frequency characteristics at 8 kHz (f_{SAM}).

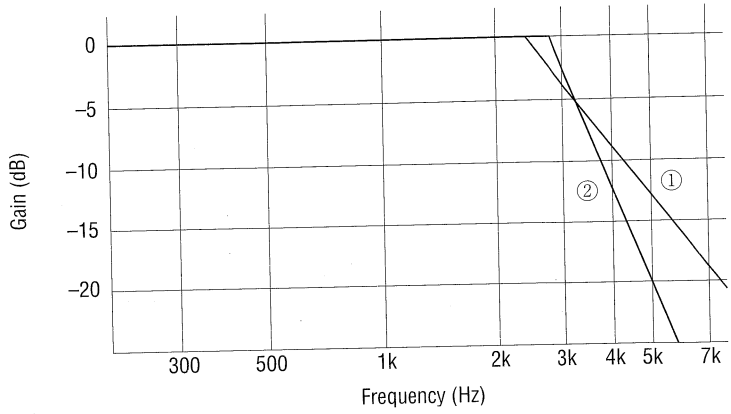


Figure 10.6 Filter's Frequency Characteristics at 8 kHz (f_{SAM})

*1 The cut-off frequency is not strictly defined as the frequency at which attenuation begins. In Butterworth type low-pass filter, the cut-off frequency is defined as the "–3 dB point of total characteristics". In a Chebyshev type low-pass filter, the cut-off frequency is defined as the "first point beyond the maximum ripple amplitude of a passband". Roughly, however, the cut-off frequency can be defined as the frequency at which attenuation begins.

Q7: Is there an inexpensive external filter configuration for voice synthesis?

A7 The active filters (filters using active devices) are classified as Butterworth, Bessel and Chebyshev type filters. These filters can be selected according to the purposes of applications.

The Butterworth type active filter focuses on the flatness of a passband. But characteristics of attenuation and response are inferior to those of the Bessel and Chebyshev type active filters.

For applications where severe flatness of a passband is not required as is the case with LPF used for voice synthesis, the Chebyshev type active filter is recommended where by allowing ripples, abrupt attenuation characteristics can be attained and active filter can be composed by smaller number of parts.

The Chebyshev type active filter can be designed by selecting appropriate ripple amplitude and attenuation characteristics.

If the frequency characteristics of a speaker itself does not reach the desired cut-off frequency, no filter is required.

Configuration

An LPF, consisting of one RC stage, containing no active device is as shown in Figure 10.7, and its transfer characteristics are given by the formula below.

$$F(j\omega) = \frac{\ell_o}{\ell_i} = \frac{1}{1 + j\left(\frac{\omega}{\omega 0}\right)} \quad \cdots\cdots\cdots\cdots (1)$$

where

$$\omega_0 = \frac{1}{CR} \quad (\omega_0 = 2\pi f_0)$$

f_0 : Cut-off frequency

Figure 10.7 LPF Consisting of One RC Stage

Figure 10.8 plots F (jw).

As shown in Figure 10.8, frequency characteristics shows attenuation at –6 dB/oct above ωo. At ωo, a value of –3 dB is observed.

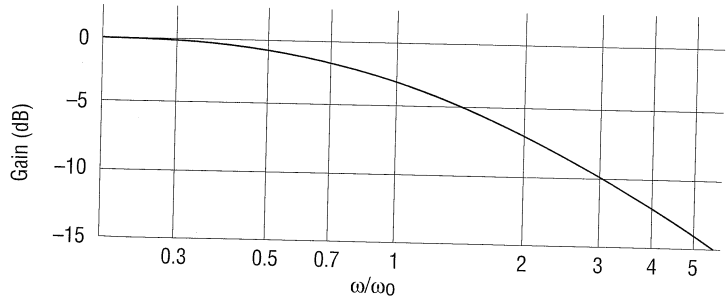


FIgure 10.8 Frequency Characteristics of LPF Consisting of One RC Stage

Figure 10.9 illustrates the circuit configuration of a second-order Chebyshev type filter.

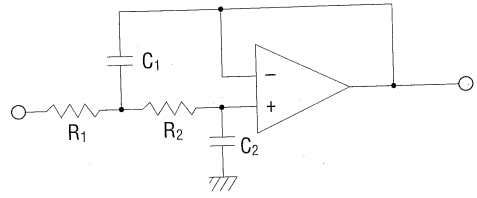


Figure 10.9 Second-order Chebyshev Type Filter

The following gives transfer characteristics of the circuit.

$$F(j\omega) = \frac{\ell_o}{\ell_i} = \frac{1}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{1}{Q} \cdot \frac{\omega}{\omega_0}}$$

$$Q = \frac{\sqrt{R_1 C_1 R_2 C_2}}{C_2 (R_1 + R_2)} \qquad \omega_0 = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

The gain is one because the voltage follower consisting of an operational amplifier is used. Assuming that R_1 and R_2 are equal to R, the following expressions are obtained:

$$C_1 = \frac{2Q}{\omega_0 R} \qquad C_2 = \frac{1}{2Q\omega_0 R}$$

Design of high-order Chebyshev type filter

Such even-order filters as the fourth- and sixth-ones can be resolved into second-order elements. Such odd-order filters as third- and fifth-ones can be resolved into second- and first-order (passive filter consisting of one RC stage) elements.

For example, a fourth-order filter can be resolved into two second-order elements as shown in Figure 10.10. Determining fn and qn allows a fourth-order filter to be readily built.

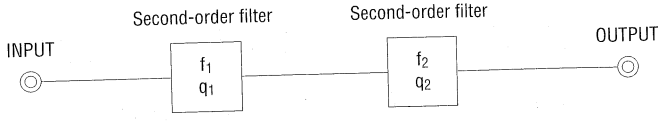


Figure 10.10 Implementation of Fourth-order LPF

The Chebyshev type filter incurs a ripple in the passband. Attenuation characteristics vary with permissible ripples, as fn and qn settings in each stage is changed.

Table 10.4 lists fn and qn values for the Chebyshev type LPF.

Table 10.4 fn and qn Values for Chebyshev Type LPF

	Ripple=0.1dB		Ripple=0.2dB		Ripple=0.25dB		Ripple=0.3dB		Ripple=0.5dB	
	fn	qn	fn	qn	fn	qn	fn	qn	fn	qn
Second order	1.8204497	0.7673593	1.5351966	0.7966418	1.4539722	0.8092536	1.3911667	0.8210811	1.231418	0.8637210
Third order	1.2999029	1.3409276	1.1889612	1.4595033	1.1569921	1.5080264	1.1321861	1.5524768	1.0688535	1.7061895
	0.9694057	0.5*	0.8146341	0.5*	0.7672227	0.5*	0.7292773	0.5*	0.6254565	0.5*
Fourth order	1.1532699	2.1829303	1.0948338	2.4350125	1.0779389	2.5361100	1.0648159	2.6279020	1.0312704	2.9405542
	0.7892557	0.6188010	0.7011094	0.6458968	0.6744223	0.6572494	0.6532428	0.6677803	0.5970024	0.7051102
Fifth order	1.0931318	3.2820141	1.0570753	3.7068586	1.0466301	3.8756825	1.0385110	4.0283601	1.0177347	4.5449633
	0.7974460	0.9145215	0.7472558	1.0009079	0.7324054	1.0359319	0.7207553	1.0678979	0.6904832	1.1778056
	0.5389143	0.5*	0.4614106	0.5*	0.4369509	0.5*	0.4171291	0.5*	0.3623196	0.5*
Sixth order	1.0627261	4.6329012	1.0382299	5.2689021	1.0311242	5.5204164	1.02555981	5.7474076	1.0114459	6.5128456
	0.8344903	1.3315707	0.8030621	1.4917187	0.7938542	1.5556533	0.7866630	1.6135959	0.7681212	1.8103772
	0.5131875	0.5994600	0.4603216	0.6259511	0.4440628	0.6370268	0.4310754	0.6472924	0.3962290	0.6836390

A value of 0.5* for qn indicates the first-order CR stage.

Example of design

The following gives an example of designing the fifth-order Chebyshev type LPF. A permissible ripple is 0.5 dB. Figure 10.11 provides the circuit.

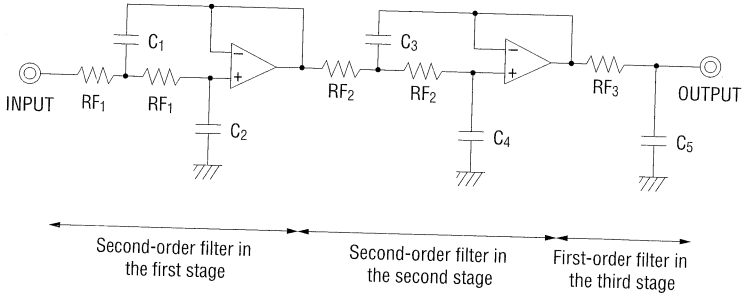


Figure 10.11 Fifth-order Chebyshev Type LPF

The fn and qn values are covered in Table 10.4. Data for the fifth order and a ripple of 0.5 dB provides the following fn and qn values.

For the second-order filter in the first stage fn = 1.0177347 and qn = 4.5449633
For the second-order filter in the second stage fn = 0.6904832 and qn = 1.1778056
For the first-order filter in the third stage fn = 0.3623196 and qn = 0.5

The values above can be used to calculate constants.

When the cut-off frequency is 2.8 kHz, the constants are determined as follows.

Second-order filter in the first stage

R_{F1}=51 kΩ

$f_0 = 2800 \times 1.0177347 \fallingdotseq 2850$ (Hz)

$$C_1 = \frac{2Q}{\omega_0 R_F} = \frac{2qn}{2\pi f_0 R_F} = \frac{2 \times 4.5449633}{2p \times 2850 \times 51 \times 10^3} = 9953 \text{ (pF)}$$

$$C_2 = \frac{1}{2Q\omega_0 R_F} = \frac{1}{2qn2\pi f_0 R_F} = \frac{1}{2 \times 4.5449633 \times 2\pi \times 2850 \times 51 \times 10^3}$$

$$= 120 \text{ (pF)}$$

Second-order filter in the second stage

R_{F2} = 56 kΩ

$f_0 = 2800 \times 0.6904832 \fallingdotseq 1933$ (Hz)

$$C_3 = \frac{2Q}{\omega_0 R_F} = \frac{2 \times 1.1778056}{2\pi \times 1933 \times 56 \times 10^3} = 3463 \text{ (pF)}$$

$$C_4 = \frac{1}{2\pi\omega_0 R_F} = \frac{1}{2 \times 1.1778056 \times 2\pi \times 1933 \times 56 \times 10^3} = 624 \text{ (pF)}$$

First-order filter in the third stage

R_{F3}=68 kΩ

$f_0 = 2800 \times 0.3623196 \fallingdotseq 1014$ (Hz)

$$C_5 = \frac{1}{\omega_0 R_F} = \frac{1}{2\pi f_0 R_{F3}} = \frac{1}{2\pi \times 1014 \times 68 \times 10^3} = 2308 \text{ (pF)}$$

The R_F value can be changed to reflect the actual capacitor value. If C_1 and C_2 values have been multiplied by 1.5, the R_{F1} value should be divided by 1.5.

Selecting appropriate capacitor values leads to the final determination of the filter constants. See Figure 10.12.

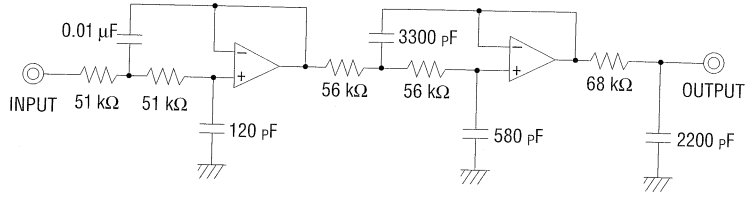


Figure 10.12 Designed Filter (Fifth Order)

Then, filter characteristics in Figure 10.12 are plotted.

Transfer characteristics for the second-order filters in the first and second stages are expressed by the formula below.

$$F(j\omega) = \frac{1}{1-\left(\frac{\omega}{\omega_0}\right)^2 + j\frac{1}{Q}\cdot\frac{\omega}{\omega_0}}$$

Transfer characteristics of the first-order filter in the third stage are expressed by the formula below.

$$F(j\omega) = \frac{1}{1 + j\left(\frac{\omega}{\omega_0}\right)}$$

For example, if ω is equal to ωo for the filter in the first stage, we get the following expression.

$$F(j\omega_0) = \frac{1}{1-(1)^2 + j\frac{1}{Q}\times 1} = -jQ = -4.5449633j$$

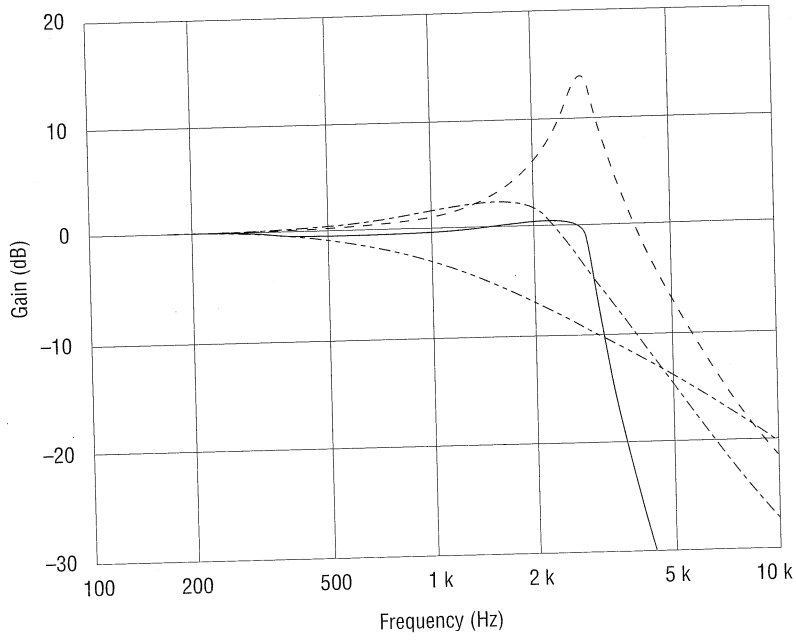
The following gives the absolute dB value of the I/O output voltage ratio.

$$20 \log 4.545 = 13.15 \text{ (dB)}$$

The absolute value is 13.15 dB for a frequency of 2850 Hz.

Figure 10.13 provides the plotted dashed curve. The alternate dot-dash line and the alternate two dot-dash line cover the second and third stages, respectively. The solid line provides total characteristics.

As the capacitor values have been approximated, total characteristics indicate that the maximum ripple is 0.6 dB and the cut-off frequency is about 2.9 kHz.



Figures 10.13 Frequency Characteristics of Designed Filter

Figures 10.14 and 10.15 provide constants and frequency characteristics of a designed third-order Chebyshev type LPF.

The solid line in Figure 10.15 provides total characteristics.

As the capacitor values have been approximated, the characteristics indicate that the maximum ripple is 3 dB and the cut-off frequency is 2.56 kHz.

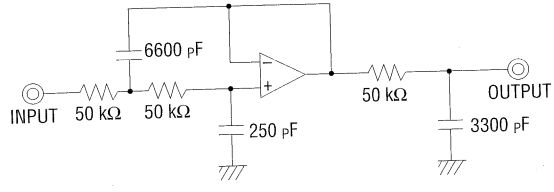


Figure 10.14 Designed Filter (Third Order)

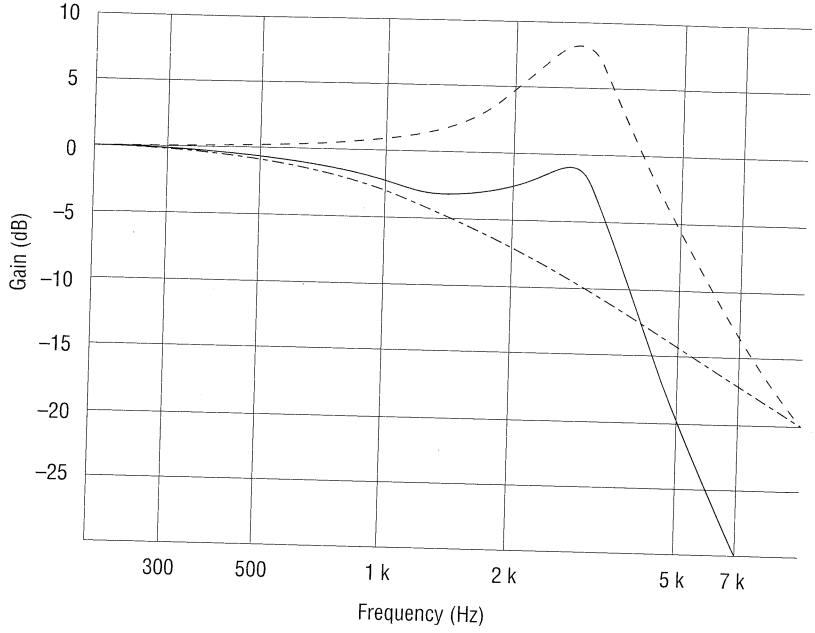


Figure 10.15 Frequency Characteristics of Designed Filter (Third Order)

Q8: Which is the chip's substrate electric potential, the V_{DD} or the GND level?

A8 Table 10.5 lists voice LSI chip products available from OKI and their substrate potential.

Table 10.5 Chip products and their substrate potential

LSI chip product model	Chip's substrate pontential
MSM6658A-XXX	GND
MSM6656A-XXX	GND
MSM6655A-XXX	GND
MSM6654A-XXX	GND
MSM6653A-XXX	GND
MSM6652A-XXX	GND
MSM9805-XXX	GND
MSM9803-XXX	GND
MSM9802-XXX	GND
MSM6376	GND
MSM6375-XXX	GND
MSM6374-XXX	GND
MSM6373-XXX	GND
MSM6372-XXX	GND
MSM6379	GND
MSM6378A	GND
MSM6588	V_{DD}
MSM6388	V_{DD}
MSM6722	V_{DD}
MSM6322	V_{DD}
MSA180	GND
MSC1157	GND
MSC1192	GND
MSC1191	GND

Q9: How should multiple power supply pins (AV_{DD}, DV_{DD} and so forth) be connected?

A9 For ICs such as MSM6388 having multiple supply and GND pins including AV_{DD}, DV_{DD}, AGND and DGND. The same power supply should be used as shown in Figure 10.16. Connect AV_{DD}, DV_{DD}, AGND, and DGND separately to each V_{DD} and GND on the printed board wiring pattern.

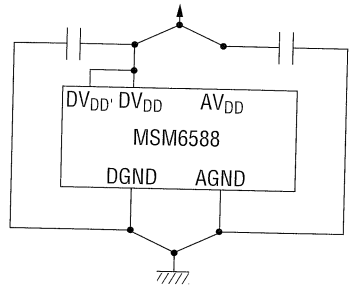
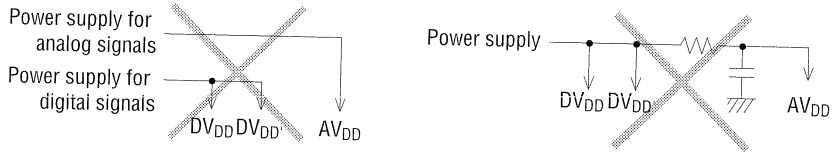


Figure 10.16 Typical GND Connection for MSM6588 Power Supply

The following connection should not be made.



The separation of supply and GND pins for AV_{DD} (analog system) and DV_{DD} (digital logic system) contributes to sound quality enhancement. Ideally a stable potential from separate power sources should be supplied. But in reality supply from separate power sources results in potential differences in the analog and digital systems. Since latching may damage the IC, the same power supply must be used.

Q10: Which EPROM can be used for the MSM6650 and MSM6376 evaluation boards?

A10 Table 10.6 lists the EPROMs (including OTP ROMs) that can be applied to evaluation boards.

Table 10.6 EPROMs Applicable to Evaluation Boards

MSM6650 Evaluation Board	4 Mbits	M5M27C401, MBM27C4001, MSM27C401 (OTP), TC574000, µPD27C4001, and devices with the same pin layout
MSM6650 Evaluation Board MSM6376 Evaluation Board	1 Mbit	M5M27C101, MBM27C1001, MSM271000, TC571000, µPD27C1001, and devices with the same pin layout

Q11: Can voice be output over lines?

A11 Figure 10.17 covers the MSM6650 family (LPF output).

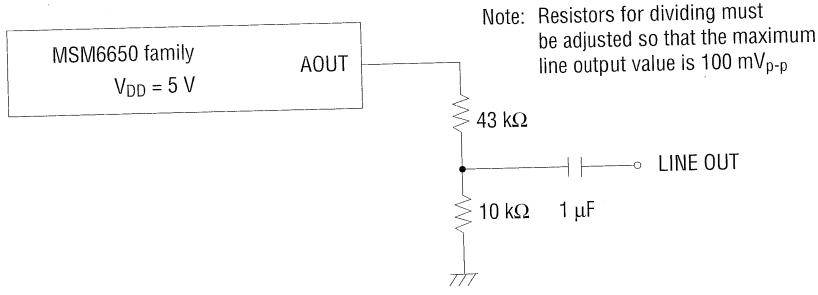


Figure 10.17 Typical Connection for Line Output in MSM6650 Family

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